SPEAr600

SPEAr® embedded MPU with dual ARM926EJ-S™ core

The SPEAr600 is a highly integrated eMPU with flexible memory support, powerful connectivity features and programmable LCD interface.
High-performance dual 32-bit ARM926EJ-S CPU cores make this part the right choice for cost-sensitive applications that require extra computational power. The SPEAr600 is a versatile device which supports a wide range of embedded applications.
Learn more about this and other SPEAr® products, development kits, reference designs and our regional design-in support centers by visiting www.st.com/spear.

Key features

- Dual ARM926EJ-S cores run up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Up to 733 DMIPS
- Memory:
  - 32 Kbytes ROM and up to 8 Kbytes internal SRAM
  - External DRAM interface: 8/16-bit DDR1-400/ DDR2-666
  - Flexible Static Memory Controller (FSMC) supporting parallel NAND Flash memory interface
  - Serial NOR Flash memory interface

- Connectivity:
  - USB 2.0 (2 hosts, 1 device)
  - 1 Giga Ethernet (GMII port)
  - I²C and fast IrDA interfaces
  - 3 SPI ports
  - 3 I²S interfaces (1 stereo input, 2 stereo outputs)
  - 2 UART interfaces
- Peripherals supported:
  - LCD controller (resolutions up to 1024 x 768 and up to 24 bpp)
  - Touchscreen support
- Miscellaneous functions:
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 MSPS
  - JPEG codec accelerator
  - 10 general-purpose 16-bit timers with capture mode and programmable prescalers
  - 10 GPIO bidirectional signals with interrupt capabilities
  - External 32-bit local bus
- Package: PBGA420 (23 x 23 mm, pitch 1 mm)

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SPEAr®: Flexible, powerful eMPUs with high connectivity

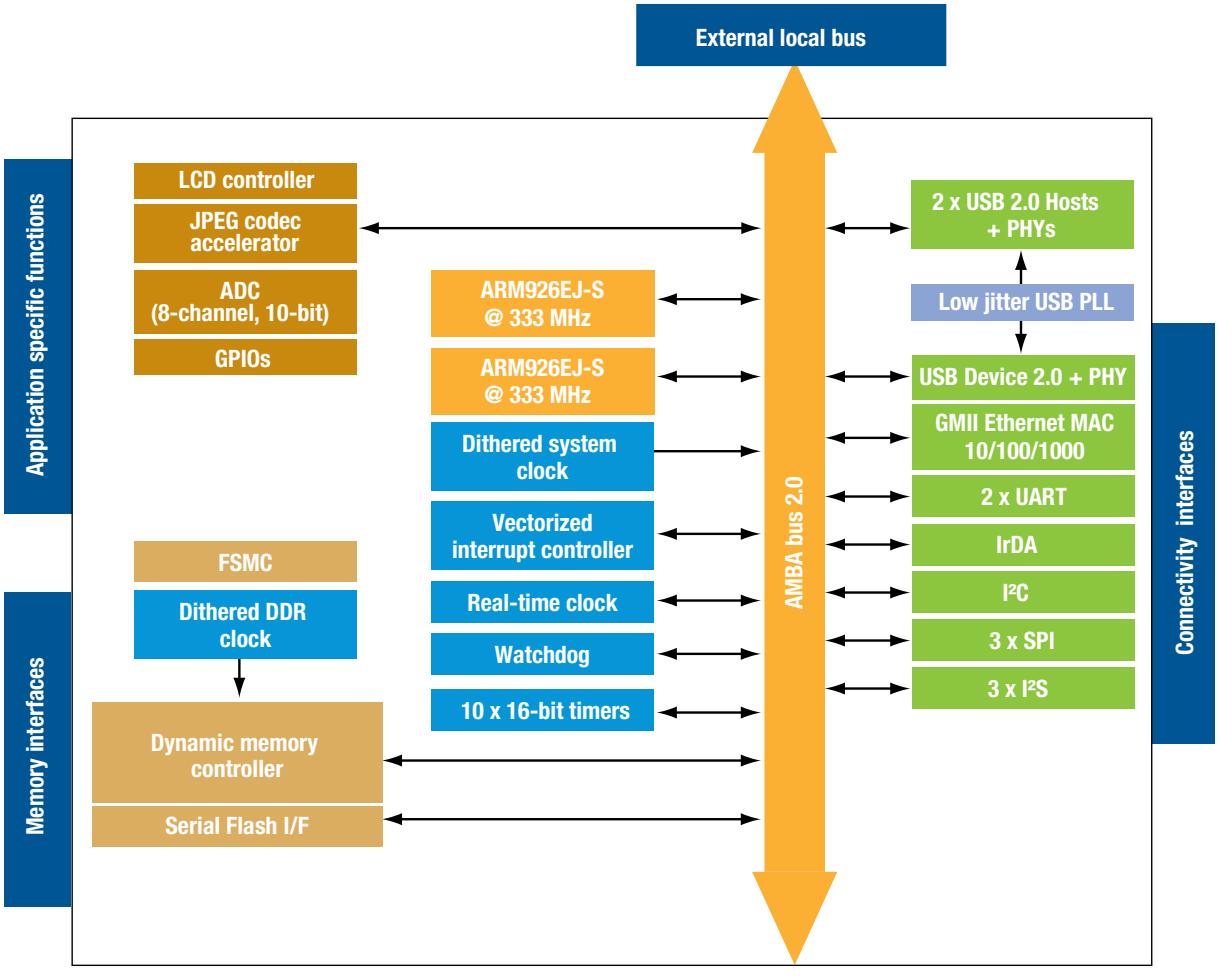
Embedded applications today demand increasingly higher levels of performance and power efficiency for computing, communication, control, security and multimedia.

ST's SPEAr® family of embedded MPUs meet these challenges head-on with state-of-the-art architecture, silicon technology and intellectual property, targeting networked devices used for communication, display and control.

The new SPEAr600 offers dual 333 MHz ARM926EJ-S cores that can support robust general-purpose processing and dedicated real-time processing together. The device supports complex operating systems like Linux, sophisticated user interfaces and microbrowsers. Both processors offer 16 Kbytes of data cache, 16 Kbytes of instruction cache, JTAG and ETM (embedded trace macrocell) for debug operations.

Furthermore, the SPEAr600 offers unique flexibility by externalizing its local bus so that external peripherals can be added.

SPEAr600 block diagram



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