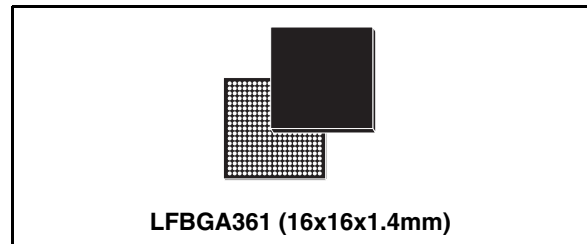




Features

- High performance ARM926 MCU (up to 333 MHz)
- MCU memory organization
 - Cache: 16 KByte instruction, 16 KByte data
 - 8 KByte instruction TCM (tightly coupled memory)
 - 8 KByte data TCM
 - 32 KByte embedded ROM for boot
 - Two banks of 64 KByte embedded SRAM
 - 512 Byte embedded SRAM for back-up
 - 4 GByte total linear address space
 - Memory extension through:
Flexible static memory controller-FSMC (NOR/NAND Flash, CF/CF+, ROM, SRAM support)
Mobile DDR/SDRAM controller:
16 bit data @166 MHz, 2 Chip Select, 512 Kbit each
- Interrupt
 - 64-channel interrupt controller (VIC)
 - 16-vectorized interrupts with 16 programmable priority Level
- DMA
 - Two 8-channel double port system DMA controllers
 - 32 DMA request for each controller
 - Two external DMA requests are supported
- 32 channel high performance GPS correlation embedded subsystem
- Eight 32-bit free running timers/counters
- Four 16-bit extended function timer (EFT) with input capture/output compare and PWM
- Real time clock (RTC)
- Pulse width light modulator (PWL)
- 32-bit watchdog timer
- Four autobaud UART with 64x8 transmit and 64x12 receive FIFO with DMA and hardware flow control
- One IrDA(SIR/MIR/FIR) interface
- Three I²C multi-master/slave interfaces
- Two synchronous serial port (SSP) with 32x32 separate transmit and receive FIFO with



- Motorola-SPI, National-MicroWire and Texas-SSI support modes
- Four multichannel serial ports (MSP) with 32x8 separate transmit and receive FIFO
- Color LCD controller for STN, TFT or HR-TFT panels
- USB 2.0 OTG high speed dual role controller (ULPI interface)
- USB full speed dual role controller with integrated 1.1 physical layer transceiver
- Two secure-digital multimedia memory card Interface (SD/SDIO/MMC) up to 8 bit data
- SPDIF input interface
- C3 hardware Reed-Solomon decoder
- Hardware sample rate converter (SaRaC)
- Four 32-bit GPIO ports
- JTAG based in-circuit emulator (ICE) with embedded medium trace module
- Typical working condition: V_{dd} : 1.2 \pm 10% V, V_{IO} : 1.8 V
- Overdrive: V_{dd} : 1.4 V \pm 5 %, V_{IO} : 1.8 V \pm 10 %, 2.5 V \pm 10 %
- Bus frequency: 166 MHz (overdrive)
- Bus/DDR frequency: 166 MHz
- HCMOS 0.90 μ m process
- Package:
 - LFBGA16x16x1.4 mm (19x19balls)
 - 0.8 mm ball pitch, (0.4 mm ball)
 - Full array
- Ambient temperature range: -40 / +85 °C

Table 1. Device summary

Order code	Package	Packing
STA2062	LFBGA361	Tray

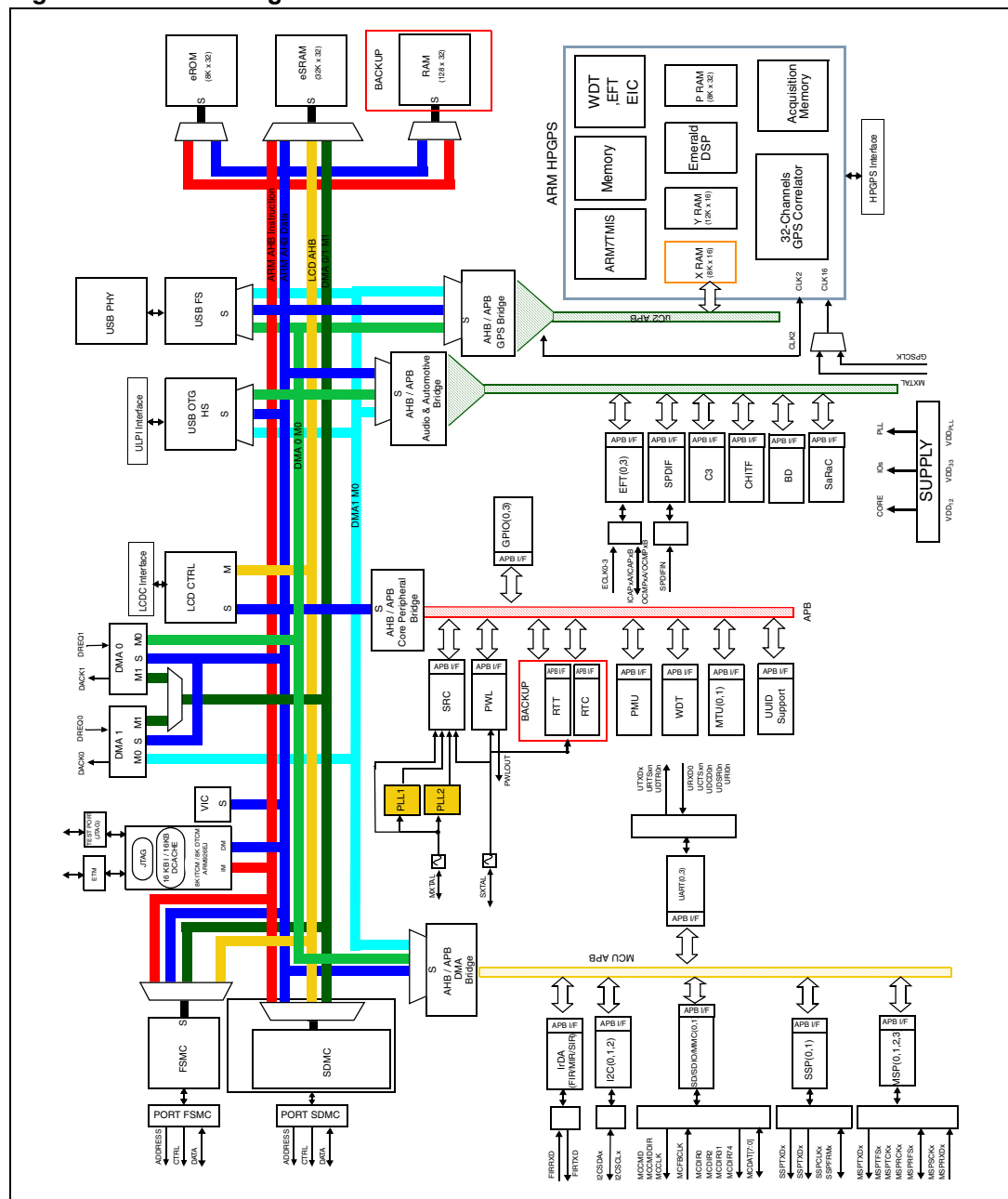
1 Description

The STA2062 is an highly integrated SOC application processor combining host capability with embedded GPS.

STA2062 targets in vehicle and mobile navigation (PND), telematics, advance audio and connectivity systems.

Figure 1: Block diagram gives an overview of the complete processor, showing how the ARM926 microcontroller and its peripherals are interfaced.

Figure 1. Block diagram

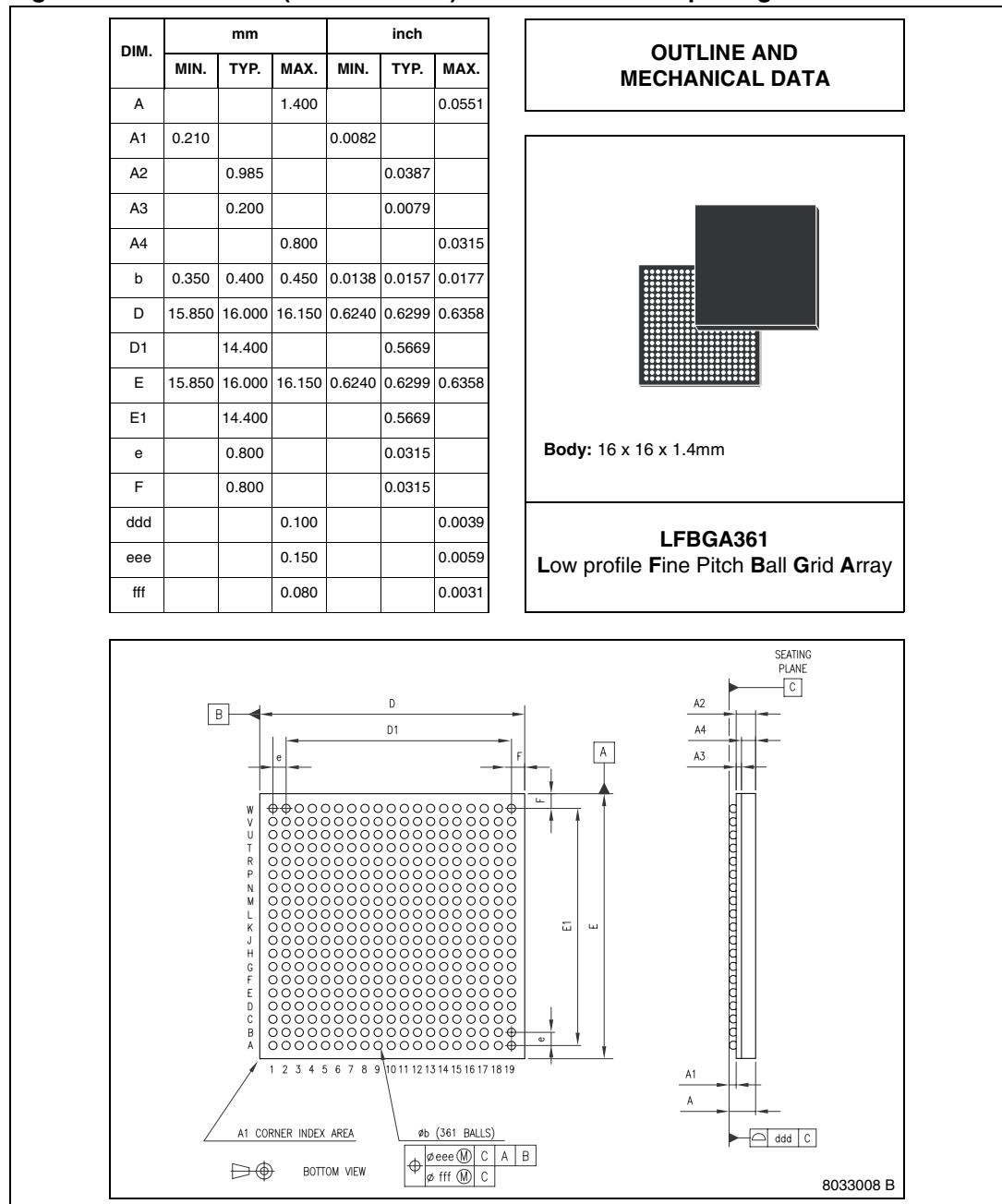


2 Package information

In order to meet environmental requirements, ST offers this device in ECOPACK[®] packages. This package has a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. LFBGA361 (16x16x1.4mm) mechanical data & package dimensions



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
3-Oct-2007	1	Initial release.
12-Oct-2007	2	Minor changes.
11-Apr-2008	3	Typo and graphic errors correction.

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