

TN0864 Technical note

Detailed revision history of the M95160-x M95080-x datasheet

This technical note supplements the M95160-x M95080-x datasheet and is reserved for engineers working on the device. It shows the datasheet's detailed revision history, which tracks all the changes implemented during the design phase of the device development.

All the references in this document are directly related to Revision 11 (dated 21-July-2011) of the M95160-x M95080-x datasheet.

The products covered by the M95160-x M95080-x datasheet are listed in *Table 1*.

Table 1. Device summary

Reference	Part number
	M95160
M95160-x	M95160-W
IVI95100-X	M95160-R
	M95160-F
	M95080
M95080-x	M95080-W
	M95080-R

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1 M95160-x M95080-x datasheet changes

Table 2. Document revision history

Date	Revision	Changes
19-Jul-2001	1.0	Document written from previous M95640/320/160/080 datasheet
06-Feb-2002	1.1	Announcement made of planned upgrade to 10MHz clock for the 5V, -40 to 85°C, range
18-Oct-2002	1.2	TSSOP8 (3x3mm body size, MSOP8) package added
04-Nov-2002	1.3	New products, identified by the process letter W, added
13-Nov-2002	1.4	Correction to footnote in Ordering Information table
21-Nov-2003	2.0	Table of contents, and Pb-free options added. V _{IL} (min) improved to – 0.45V
08-Jun-2004	3.0	MLP8 package added. Absolute Maximum Ratings for $V_{IO}(min)$ and $V_{CC}(min)$ improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. Process identification letter "G" information added. SO8 narrow and TSSOP8 Package mechanical specifications updated.
07-Oct-2004	4.0	Product List summary table added. AEC-Q100-002 compliance. tHHQX corrected to tHHQV. 10MHz, 5ms Write is now the present product. tCH+tCL<1/fC constraint clarified
21-Sep-2005	5.0	Added 20MHz and -S product information. Removed DIP package. Info on Pull-up resistors, VCC lines and Note 2. added to Figure 4.: Bus master and memory devices on the SPI bus. Device internal reset paragraph clarified. Packages compliant with the JEDEC Std J-STD-020C. Process info updated in DC and AC parameters and Table 32.: Ordering information scheme.

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Table 2. Document revision history (continued)

Date	Revision	Changes
24-May-2007	6	Document reformatted. Small text changes. TSSOP8 3 x 3 mm (DS) package removed, 1.65 V to 5.5 V operating
		voltage range removed (M95080-S and M95160-S removed). Figure 4: Bus master and memory devices on the SPI bus updated, note 2 removed and explanatory paragraph added (see Section 3: Connecting to the SPI bus).
		Section 2.7: V _{CC} supply voltage and Section 2.8: V _{SS} ground added. Power-up, Device Internal Reset and Power-down replaced by
		Section 4.1: Supply voltage (V _{CC}). Command termination specified in Section 6.4: Write Status Register
		(WRSR). Blank process no longer available for Root part number 1, M95080, Root
		part number 2 and M95080-W in the device grade 3 range. L, GB and SB processes no longer available for Root part number 1 and M95080, in the device grade 6 range.
		L process no longer available for Root part number 2 and M95080-W in the device grade 6 range.
		I _{CC1} value and test conditions modified in <i>Table 19: DC characteristics</i> (M95160-R and M95080-R).
		End timing line of t _{SHQZ} modified in <i>Figure 17: Serial output timing</i> . SO8N and UFDFPN8 package specifications updated. All packages are ECOPACK® compliant.
		Blank option removed below Plating technology and Note 2 modified in <i>Table 32: Ordering information scheme</i> .
		Table 33: Available M95160 products (package, voltage range, temperature grade) and Table 34: Available M95080 products (package, voltage range, temperature grade) added.
	7	Endurance modified <i>on page 1</i> . Small text changes.
		Section 4.1: Supply voltage (V _{CC}) on page 12 modified. Section 6.6: Write to Memory Array (WRITE) on page 23 modified.
06-Mar-2008		Table 19: DC characteristics (M95160-R and M95080-R) updated.
		Note removed below <i>Table 24: AC characteristics (M95160-W and M95080-W, device grade 6) on page 35.</i>
		Inch values are calculated from millimeters and rounded to 4 decimal digits and UFDFPN package specifications updated (see Section 10: Package mechanical data on page 41).
26-Jan-2009	8	WLCSP (CS) package added (see Figure 20 and Table 30: WLCSP-R 1.350 x 1.365 mm 0.4 mm pitch 8 bumps, package mechanical data).
		M95160-F part number added (delivered in WLCSP package and device grade 6 only).
		Section 2.7: V _{CC} supply voltage and Section 6.4: Write Status Register (WRSR) updated.
		Table 27: AC characteristics (M95160-F) added. Figure 15: Serial input timing, Figure 16: Hold timing and Figure 17: Serial output timing updated.

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Table 2. Document revision history (continued)

Date	Revision	Changes
12-May-2009	9	Section 4.1.2: Device reset updated. V _{RES} added to DC characteristics tables 15, 16, 17, 18, 19 and 20. Note added to Section 6.6: Write to Memory Array (WRITE). Note 1 added to Table 19: DC characteristics (M95160-R and M95080-R). VIL and VOL modified in Table 20: DC characteristics (M95160-F). Table 24: AC characteristics (M95160-W and M95080-W, device grade 6) split into two tables: Table 24 for process GB or SB and Table 25 for process SA. M95160-F is now available in device grade 6 (Table 33: Available M95160 products (package, voltage range, temperature grade) updated.
09-Oct-2009	10	Revision number of 12-May-2009 corrected in <i>Table 1: Document revision history.</i> V _{RES} corrected in <i>Table 15: DC characteristics (M95160 and M95080, device grade 3)</i> and <i>Table 16: DC characteristics (M95160 and M95080, device grade 6).</i>
21-Jul-2011	11	MC package added (UFDFPN8) Two tables removed in Section 11: Part numbering.

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Table 3. Document revision history

Date	Revision	Changes
09-Jan-2012	1	Initial release.

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