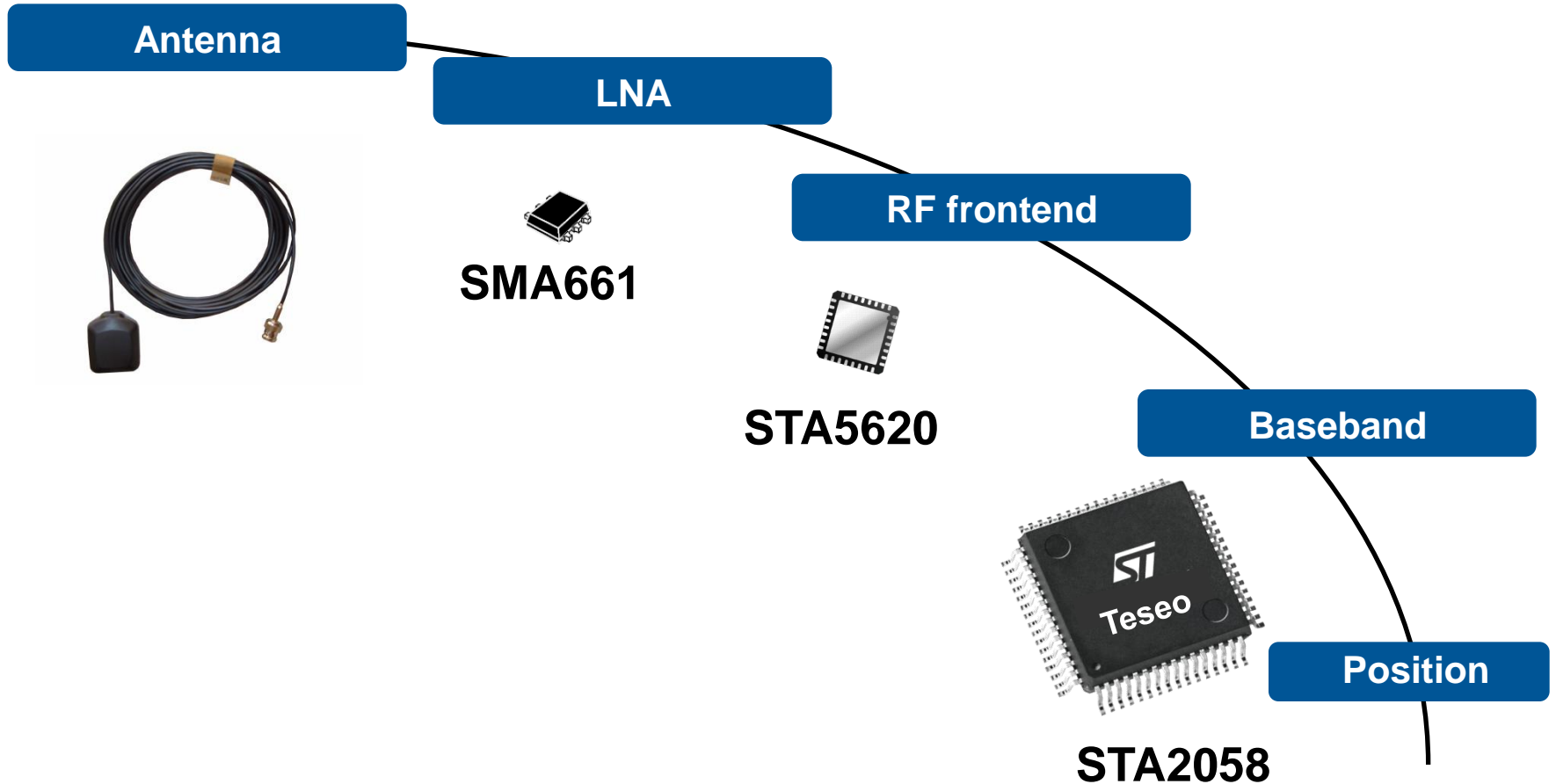


Telematics – Navigation – Multimedia

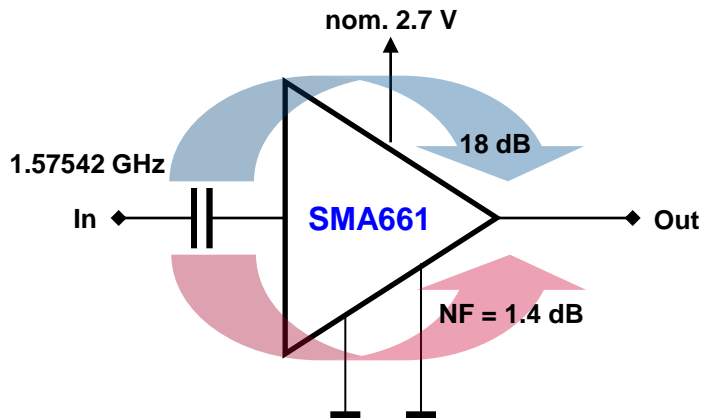


July 2010

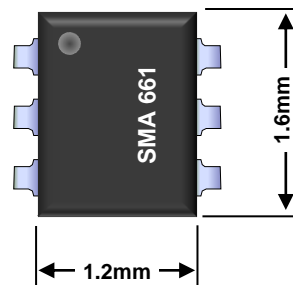
Basic GPS system



SMA661 – low-noise amplifier



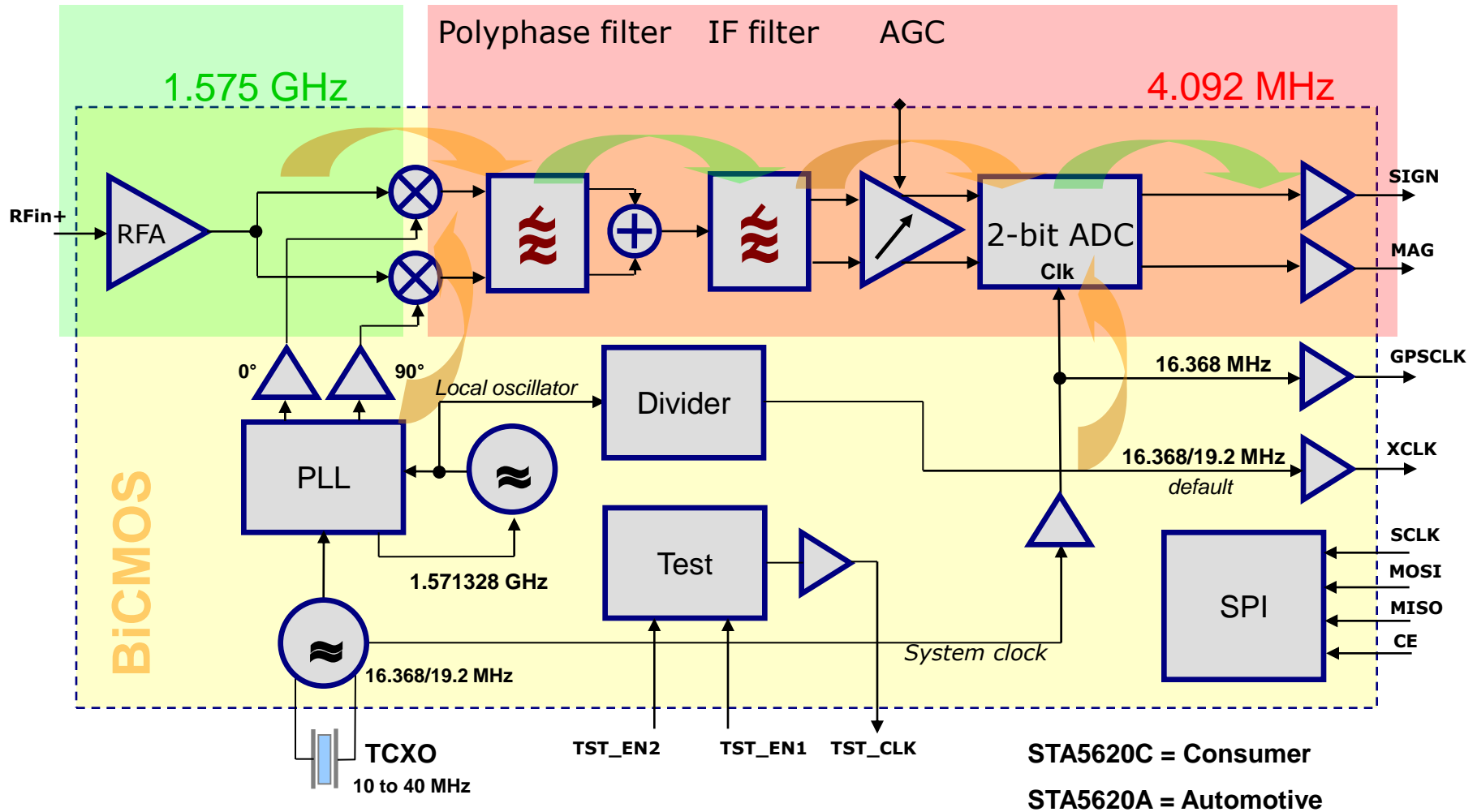
SOT666 package



- Gain 18 dB
- Noise figure 1.4 dB (1.15 typ.)
- 1 external component
- 1.2 x 1.6 mm footprint

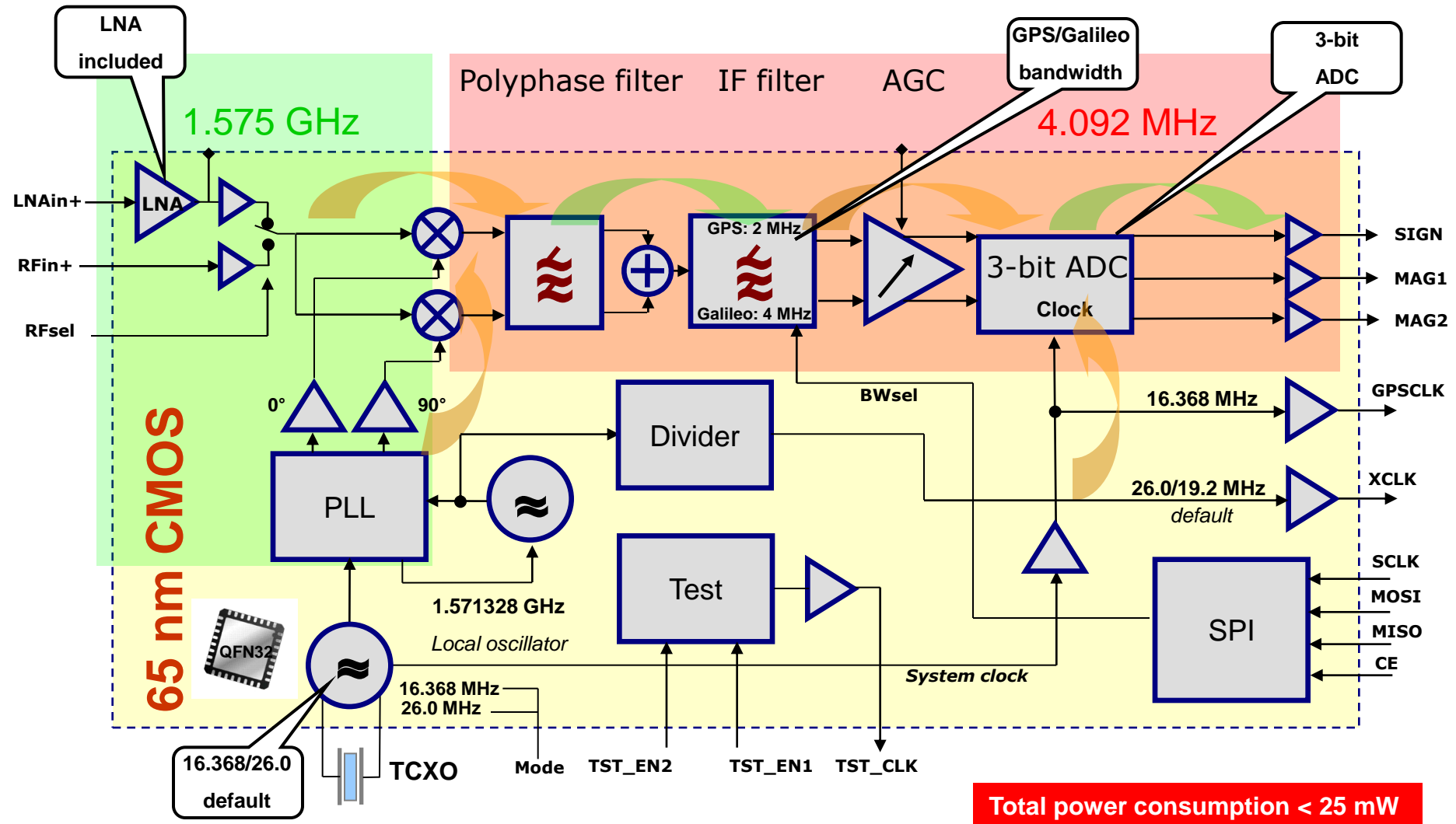
This device is qualified according to AEC-Q100 but cannot be tested in automotive grade (waiver needed).

STA5620 HP-GPS frontend

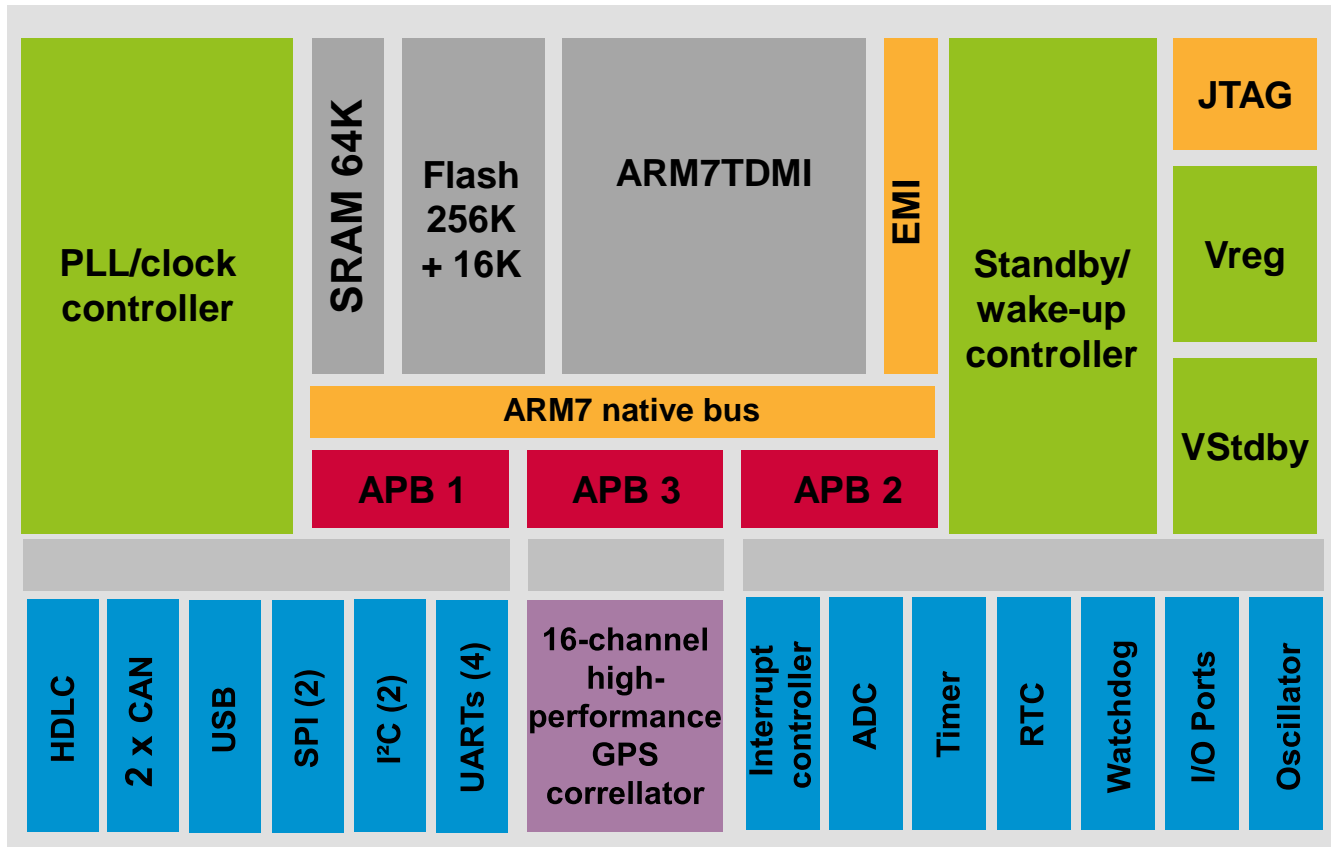


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STA5630 – Galileo GPS frontend



STA2058 Teseo



Highly-integrated solution: embedded memories, CAN, GPS

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STA2058 Teseo

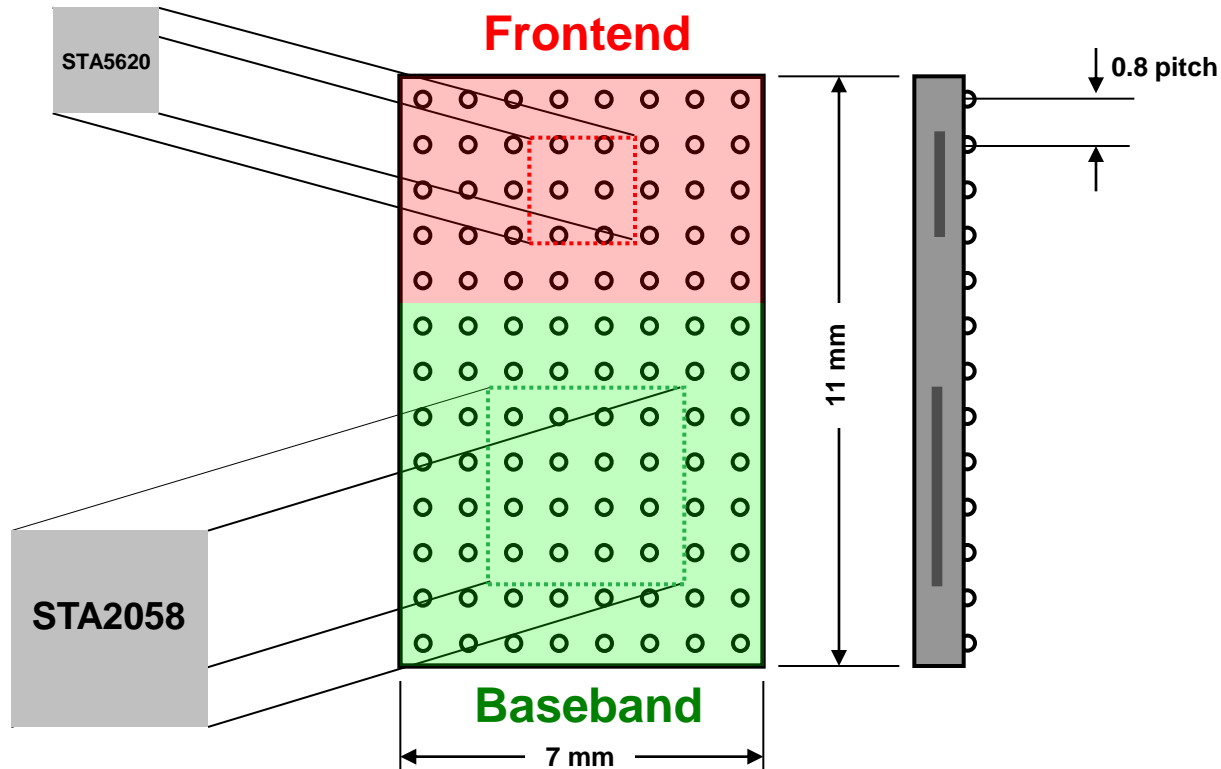


- 0.18 μm technology, 3.3 V single supply, low power, -40 to +85 $^{\circ}\text{C}$
- ARM7TDMI, 32-bit RISC engine, JTAG
- Embedded 256 Kbyte + 16 Kbyte Flash, 64 Kbyte SRAM
- External memory interface: 4 banks and up to 64 Mbytes
- 16-channel, high-performance GPS correlator and DSP (*STMicroelectronics IP*)
- Electrically isolated real-time clock with wake-up capability
- Two CAN controllers (CAN protocol rev. 2.0 part A and B) up to 1 Mbit/s
- Four 16-bit multipurpose timers (capture, compare, count, PWM)
- Four UARTs, two SPI, two I²C and USB for serial communications
- Smartcard interface capability (ISO 7816-3 including clock generation)
- Watchdog and wake-up controller (RTC or/and external event)
- HDLC controller (including NRZI, FM0 and Manchester encoder)
- 4-channel 12-bit analog-digital converter (sigma-delta)
- On-chip voltage regulators for CPU and core logic

Multi-chip solutions



STA2058 Teseo – two chips – one package – no stacked die

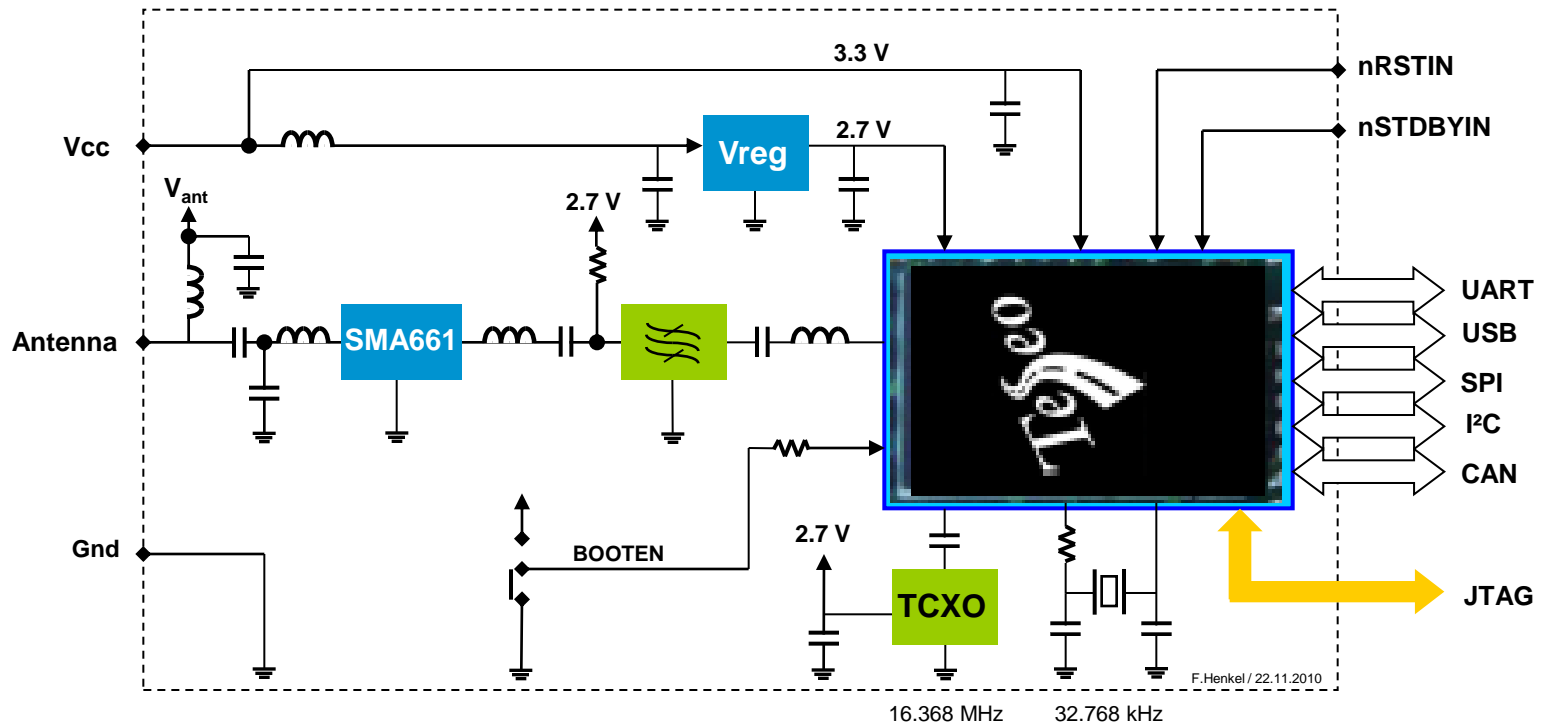


Automotive qualification according to AEC-Q100

STA2058 Teseo multi-chip module

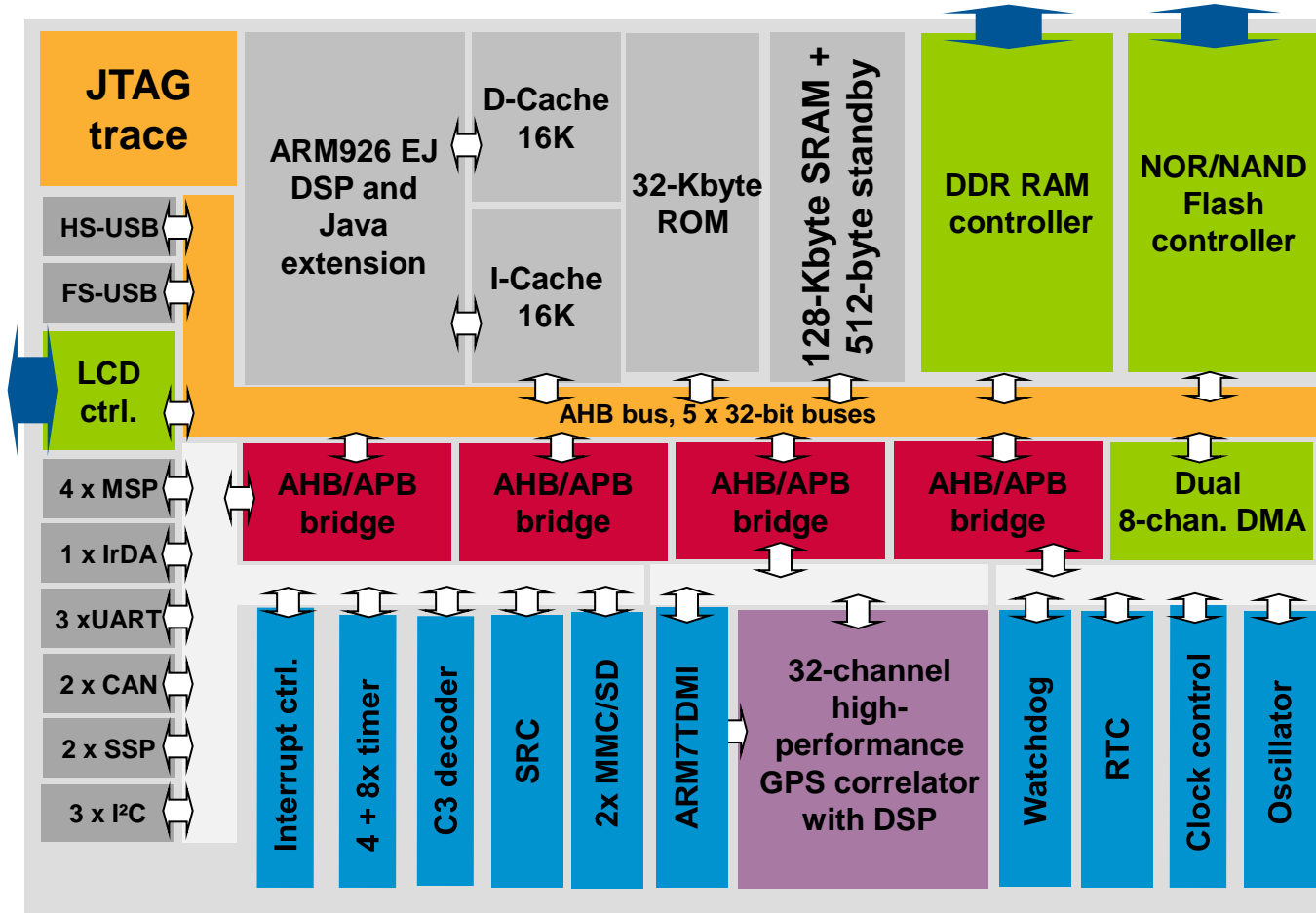


Basic circuit diagram



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STA2062 Cartesio



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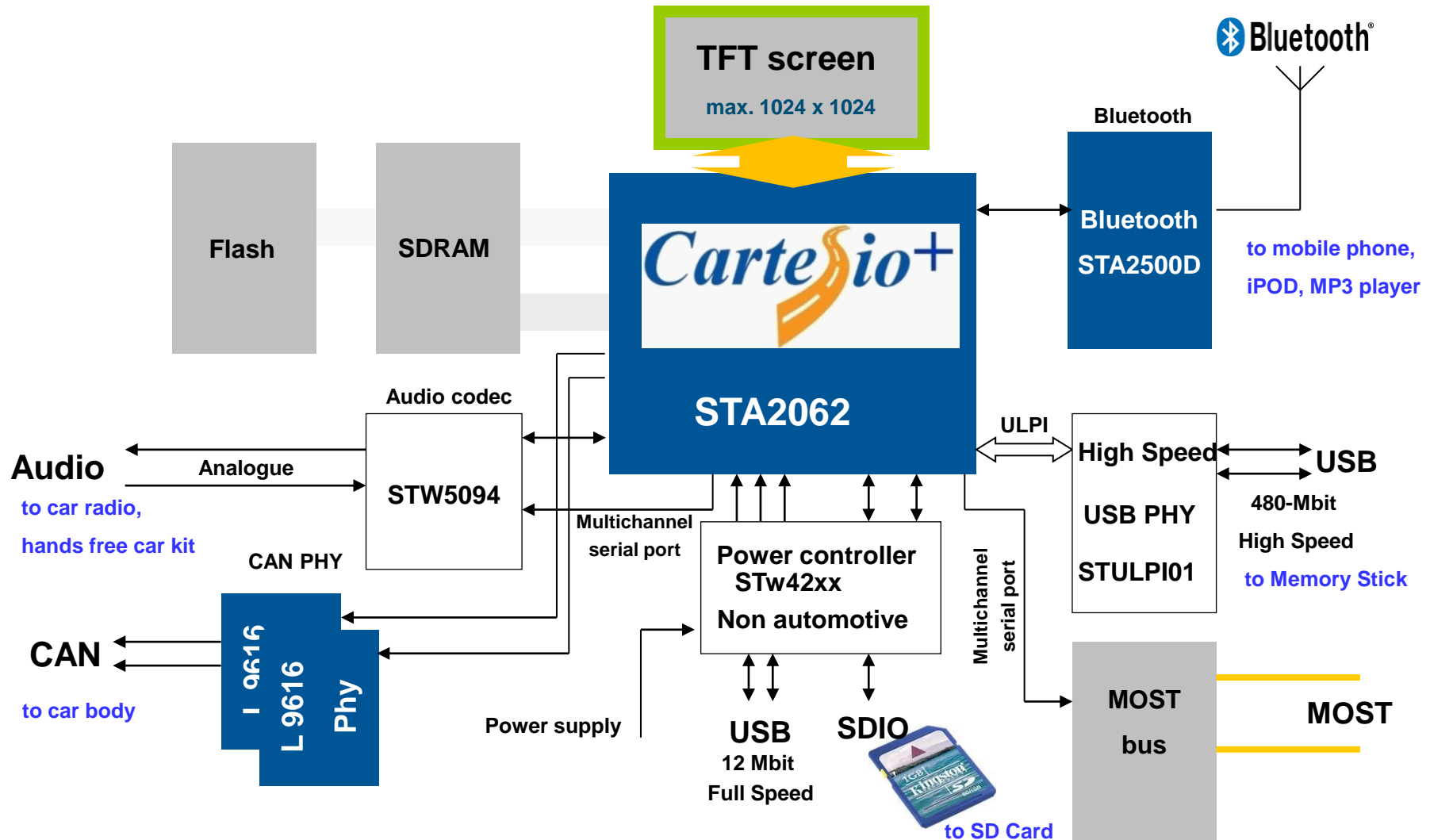
STA2062 Cartesio



- ARM926 EJ-S CPU @ 260/351 MHz
- 90 nm HCMOS process
- *ARM DSP* (single-cycle MAC) and *Jazelle* Java extension for fast processing
- SDRAM/mDDR-DRAM, NAND/NOR Flash support
- High-performance, 32-channel GPS correlator with DSP + ARM7TDMI
- Rich offer of serial communication channels (UART, SSP, I²C)
- Two CAN controller (CAN 2.0 B)
- Two USB dual-mode controller (On-The-Go and device mode, 1xFS,1xHS)
- Hardware sample rate converter (44.1 kHz < > 48 kHz, etc.)
- Multi serial ports (for I²S, PCM, T1/D1, SPI, AC97 programmable)
- Two Secure Digital and MultiMediaCard interfaces
- C3/block decoder for CD drive
- LFBGA 361 package (0.8 pitch)



Communication gateway

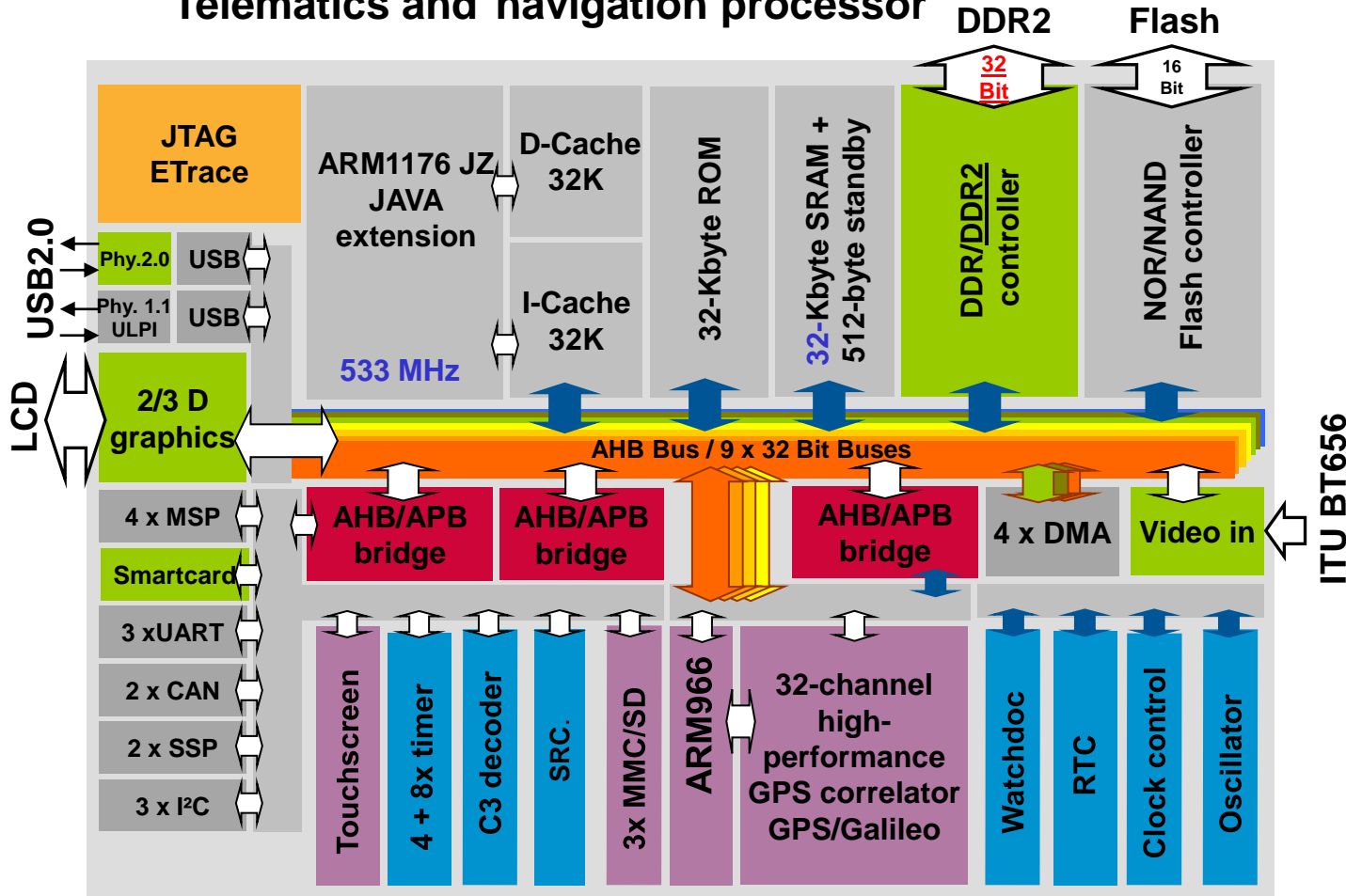


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STA2064/65 Cartesio+



STA 2064/65 Cartesio+ Telematics and navigation processor



■ Blocks in green are new to Cartesio+

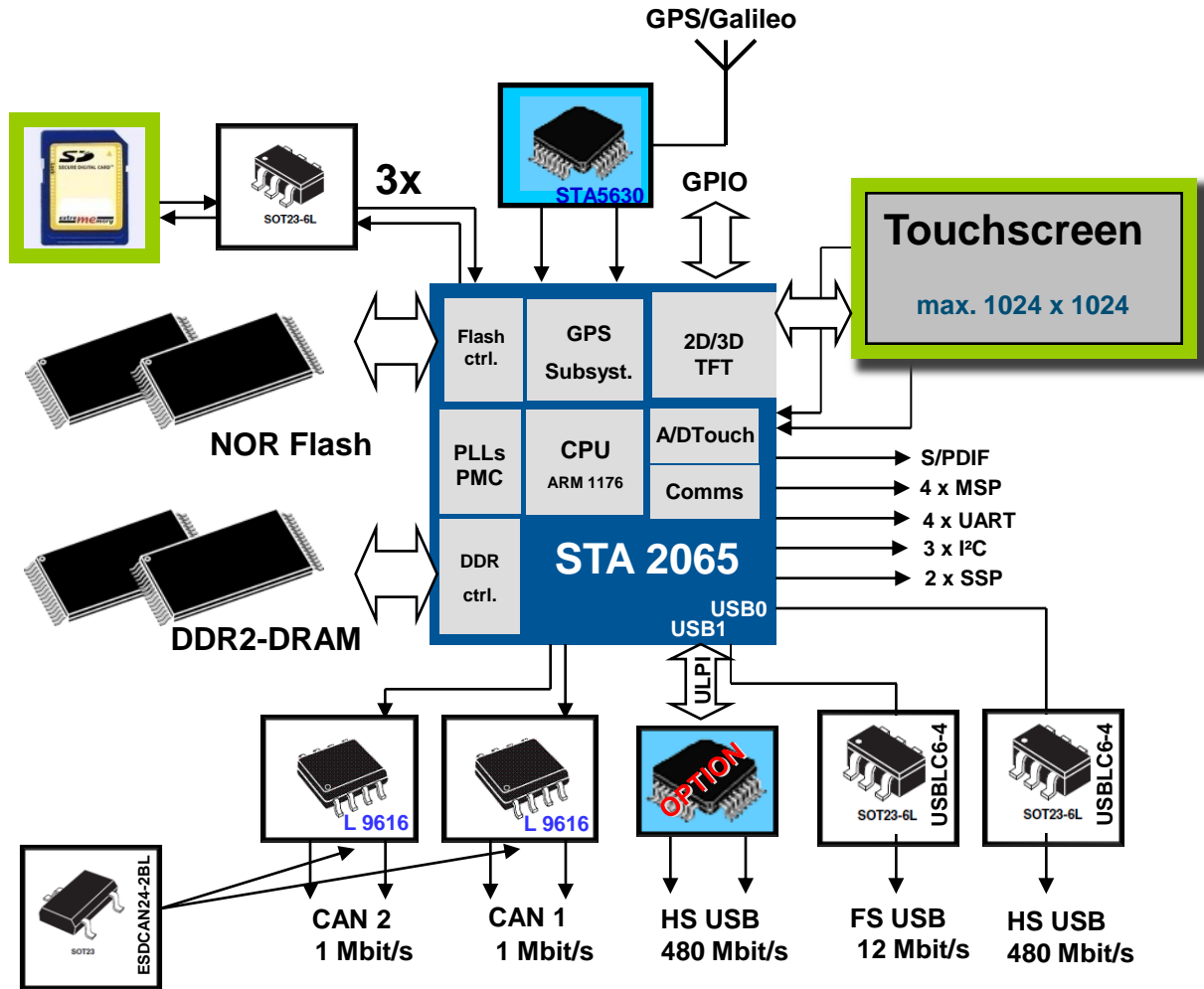
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STA 2064/65 Cartesio+



- ARM1176 JZF CPU @ 533 MHz (automotive)
- 55 nm HCMOS process
- *Jazelle* extension for fast Java processing and floating point unit
- Mobile DDR and DDR2-DRAM (2xCS, 1 Gbit each), NAND/NOR Flash support
- High-performance, 32-channel GPS correlator with DSP + ARM966
- Video input port, JPEG and 2D/3D graphics accelerator and LCD controller
- Rich offer of serial communication channels (UART, SSP, I²C)
- Two CAN controllers (CAN 2.0 B)
- Two USB 2.0 dual-mode controllers (2xHS, 1x 2.0 Phy, 1 x 1.1 Phy)
- Hardware sample rate converter (44.1 kHz < > 48 kHz, etc.)
- Multi serial ports (for I²S, PCM, T1/D1, SPI, AC97 programmable) and S/PDIF
- Three Secure Digital and MultiMediaCard interfaces
- 10-bit ADC with 8 inputs (touchscreen support)
- C3/block decoder for CD drive
- STA2064: TFBGA 289 package (0.8 pitch), limited functions
- STA2065: LFBGA 372 + 100 package (0.65 pitch), full functionality

Basic Cartesio+ system



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Cartesio versus Cartesio+



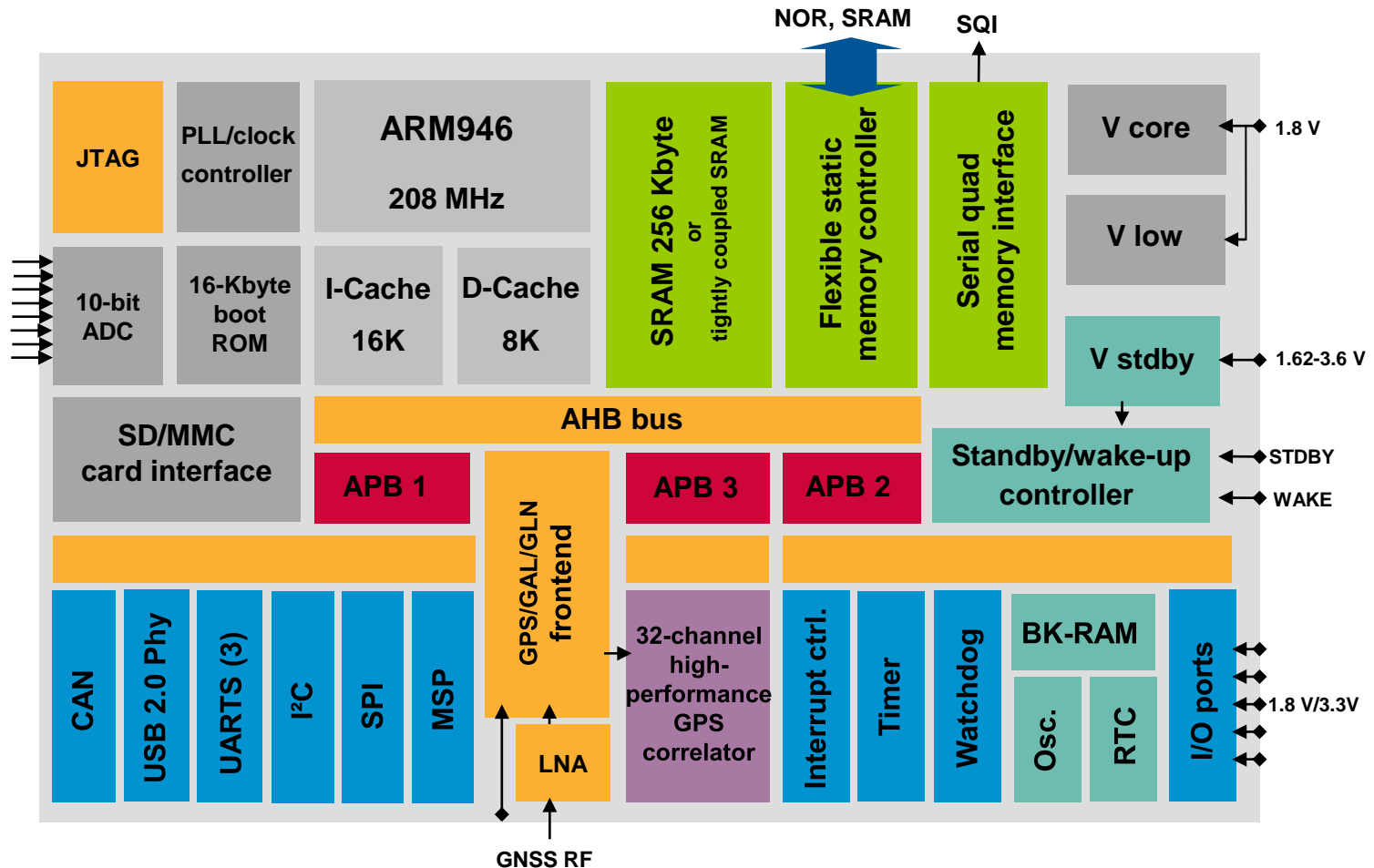
Feature	STA2062 Cartesio	STA2064/5 Cartesio+
Main processor	ARM946	ARM1176
Main processor speed/automotive	325 MHz/351 MHz	533 MHz/624 MHz
Caches	16k + 16k	32k + 32k
Floating point unit	no	yes
SRAM embedded	64 Kbyte	32 Kbyte
Number of system buses	5 x 32 bits	9 x 32 bits
System bus speed	166 MHz	208 MHz
DRAM support	SDRAM/mobile DDR	Mobile DDR/DDR II
DRAM bus width	16 bit	16/32 bit
2D/3D graphics accellerator	none	yes
JPEG H/W accellerator	none	yes
Video input port	none	CCIR 656
USB controller (dual role)	1 x USB1.1 ,1 x USB2.0	2 x USB 2.0
USB physical layer device	1 x USB 1.1	1 x USB 2.0, 1 x USB 1.1
SD/MMC card interfaces	2 x	3 x
A/D converter and touchscreen control	none	10 bit, 8 channel
Smart card interface	none	yes
GPS processor	ARM7TDMI	ARM946
GPS correlator	GPS	GPS and Galileo
GPIO domain voltages	1.8 V and 2.5 V	1.8 V, 2.5 V and 3.3 V

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STA8088 Teseo II



3GNSS systems and telematics controller



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STA8088 Teseo II

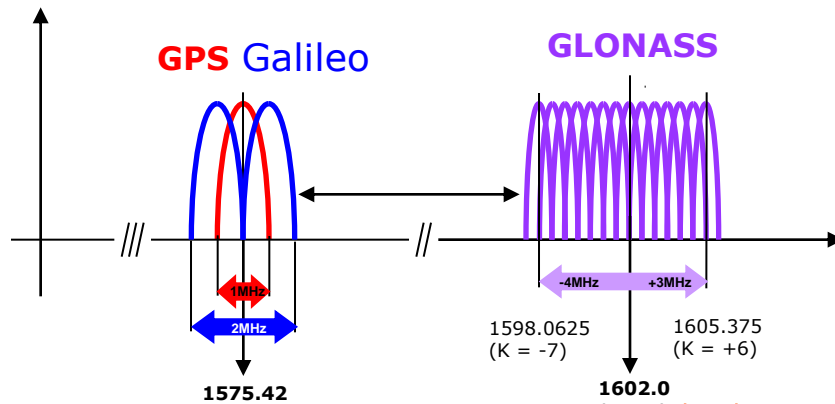
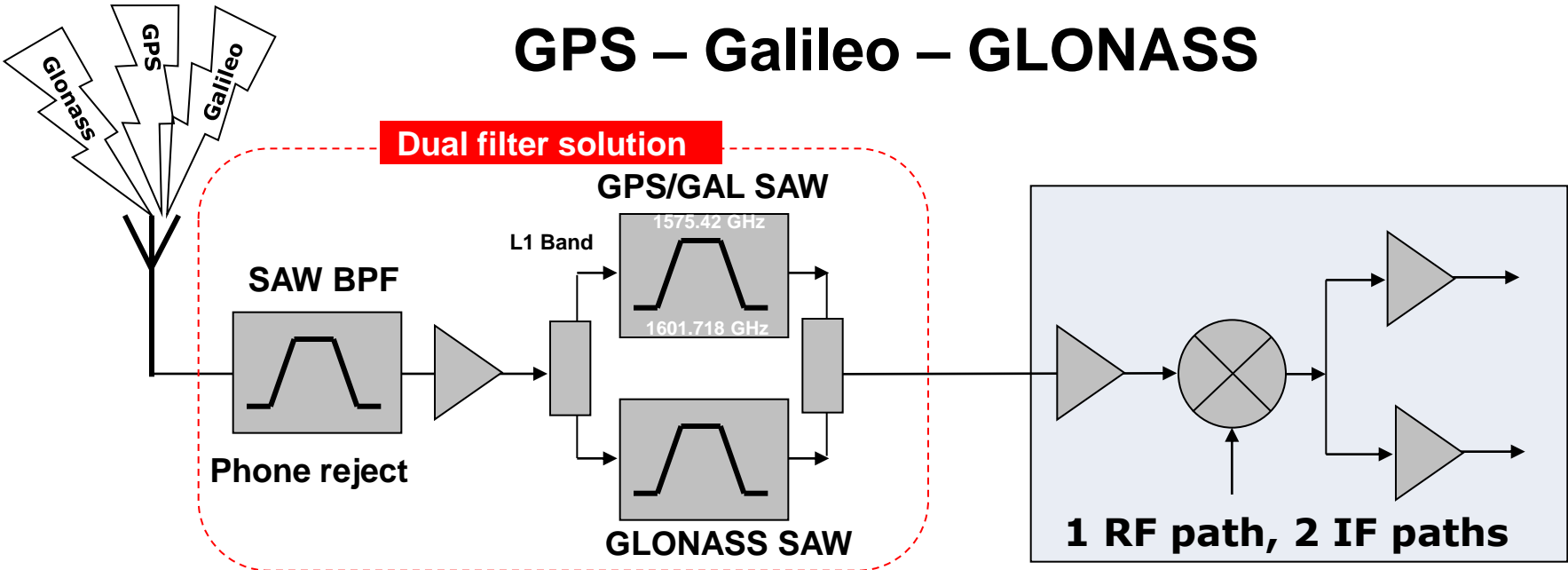


- 55 nm technology, 1.8 V single supply, -40 to +85 °C, AEC-Q100
- ARM946, 32-bit RISC engine with 16K I-Cache + 8K D-Cache (opt. TCM)
- Embedded 256 Kbyte SRAM and 16 Kbyte boot-ROM
- FSMC for static memories (NOR-Flash, SRAM) and SQI (serial SQI-Flash)
- 32+2-channel, high-performance G3 correlator (GPS, Galileo, GLONASS)
- Embedded *GPS/Galileo/GLONASS* radio frontend
- Isolated real-time clock with wake-up capability
- CAN controller (CAN protocol rev. 2.0 part A and B) up to 1 Mbit/s
- 10-bit successive approximation A/D with up to 500 ksps, 8 inputs
- Four 16-bit multipurpose timers (capture, compare, count, PWM)
- Three UARTs, SPI, I²C, MSP (I²S) and USB 2.0 OTG for serial communications
- SD/MMC card interface
- Watchdog and wake-up controller (RTC or/and external event)
- LFBGA 153 package, 9 x 9 mm, 0.65 mm pitch

STA8088 Teseo II



GPS – Galileo – GLONASS



Target specification

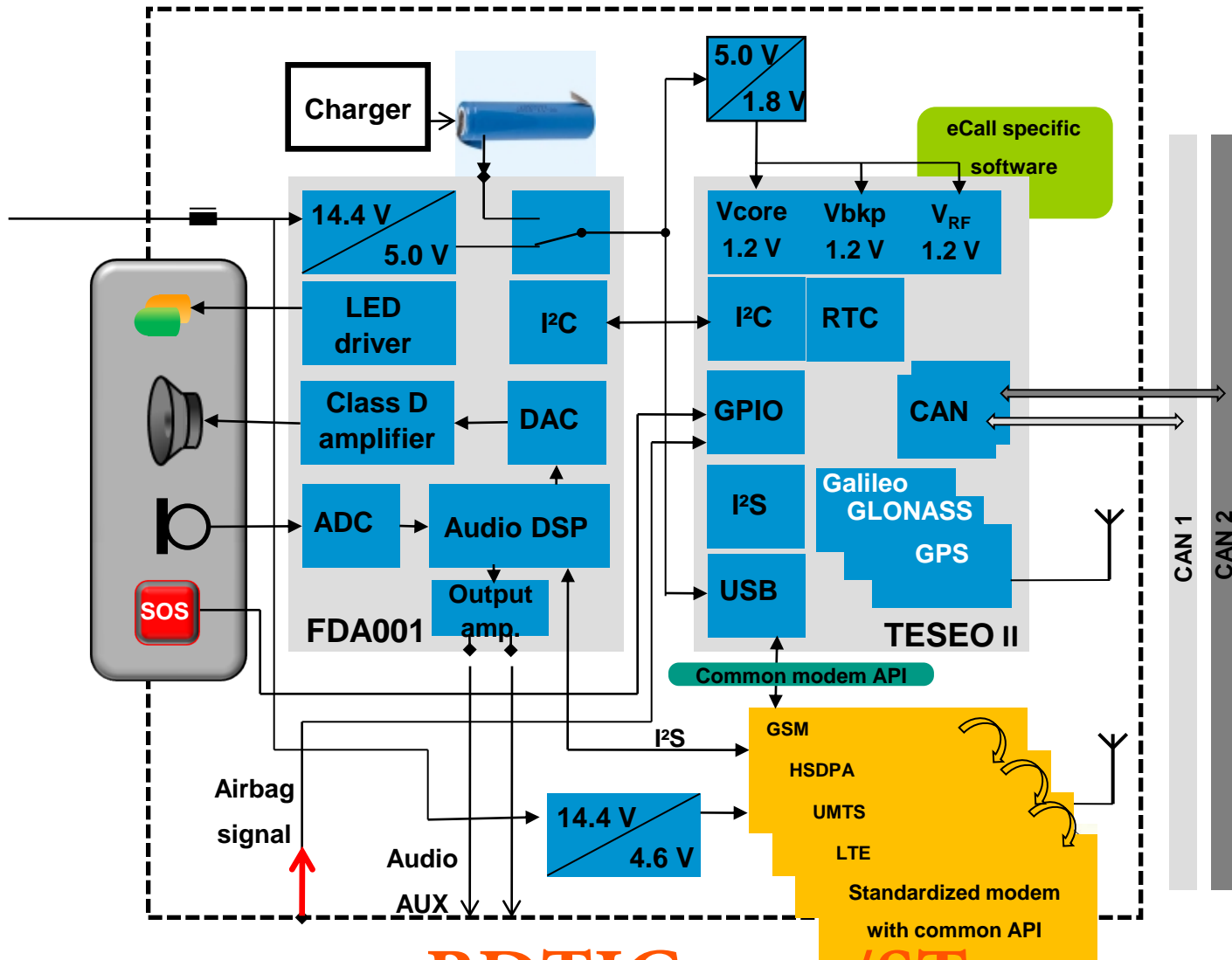
Sensitivity: -161 dBm

TTFF hot: 1 sec.

TTFF cold: 35 sec.

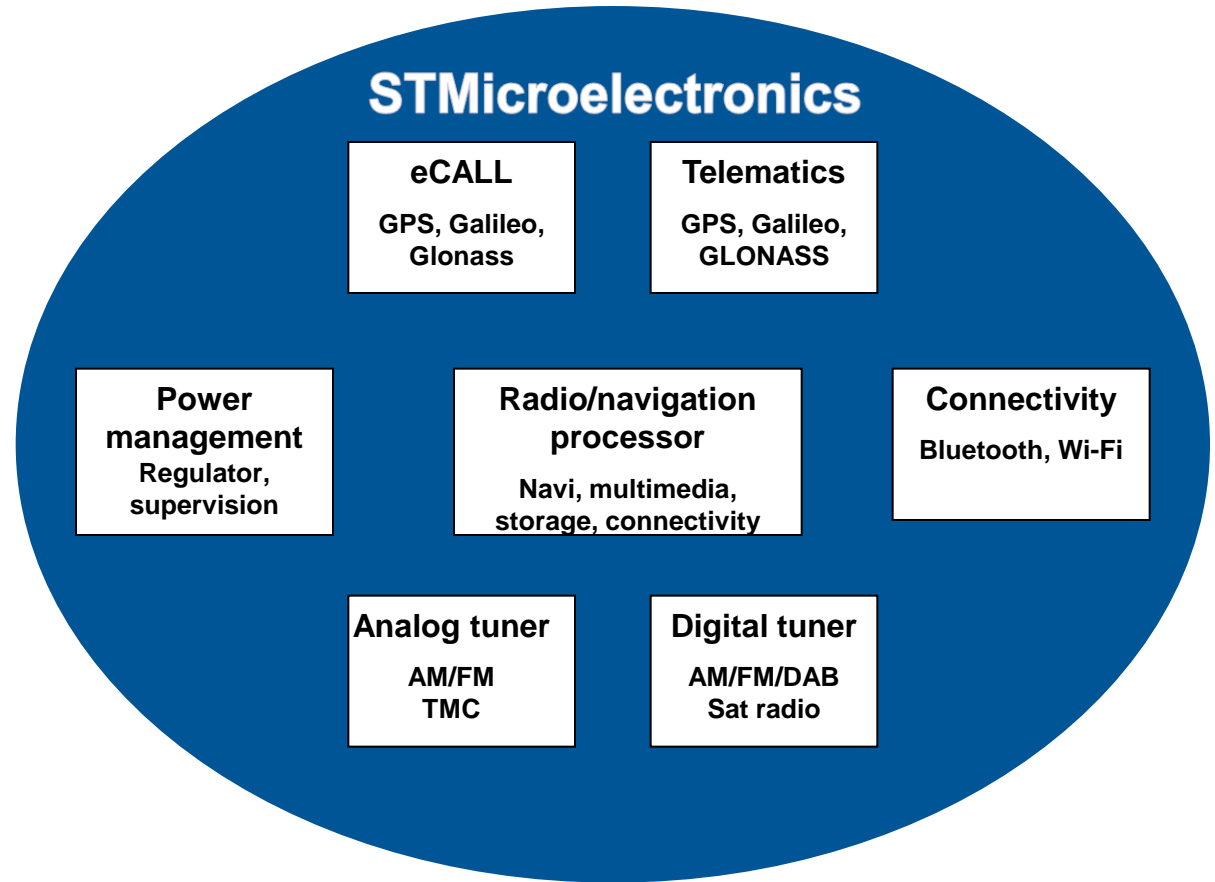
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eCall/Telematics system



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Telematics/navigation systems



More information



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