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TI is developing a new arsenal of digital input/output buffer information specification (IBIS) simulation models to meet a variety of customer needs. This article, the second of a three-part series, investigates IBIS-model validation. Since it is important to know the quality of an IBIS model, this article covers the four stages of the IBIS Open Forum's QC process that help insure that the IBIS model provides reliable simulations with signal integrity.

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Inductive coupling is the method by which efficient and versatile wireless power can be achieved. This article provides an overview of the Wireless Power Consortium (WPC) standard and the design considerations for the power transmitted, the power received, and the communications protocol. Also included is an introduction to TI's WPC-compliant solutions in the form of three newly developed ICs.

Fine-tuning TI's Impedance Track™ battery fuel gauge with $LiFePO_4$ cells in shallow-discharge applications 13

Impedance Track technology has been established as an accurate tool for determining a battery pack's state of charge (SOC). In applications where full discharge of the battery with a long rest period is not possible, it is necessary to explore a shallow-discharge option to determine the SOC. As demonstrated in this article, new battery chemistries like $LiFePO_4$ require the Impedance Track algorithm to be customized to achieve accurate SOC measurements when shallow-discharge cycles are necessary. Included are calculations and examples for adjusting the algorithm parameters for a specific battery pack.

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

The IBIS model, Part 2: Determining the total quality of an IBIS model

By Bonnie C. Baker
Senior Applications Engineer

This article is Part 2 of a three-part series. Part 1 (see Reference 1) discussed the fundamental elements of digital input/output buffer information specification (IBIS) simulation models and how they are generated in the SPICE environment. This article, Part 2, investigates IBIS-model validation. Part 3, which will appear in a future issue of the *Analog Applications Journal*, will show how IBIS users investigate signal-integrity issues and problems during the development phase of a printed circuit board (PCB).

IBIS models can be generated from the SPICE deck of an integrated circuit (IC) or in the lab. In both cases, the modeling engineer collects DC data to generate the power-clamp, ground-clamp, pull-up, and/or pull-down data for the various digital buffers on the chip. Following this, data is collected on the output buffer's transient or on the AC rise and fall times. See Reference 1 for more information on these data-collection processes. The IBIS model's transient data replicates the time behavior of output buffers. The modeling engineer acquires the model data with an array of power-supply conditions and junction temperatures. Further enhancements include the addition of the IC's package characteristics, buffer-input chip capacitance, and surrounding documentation. Once the IBIS model exists, the engineer reviews it to verify several quality stages and then produces a validation report that correlates the IBIS model to SPICE simulations or bench data.

Historically, IBIS models have had a reputation of poor quality because many IBIS users have received incorrect models from vendors. The errors range from simple format errors to the model not really portraying the behavior of the buffers in the IC at all. Texas Instruments (TI) is committed to generating quality, reliable IBIS models for customers' signal-integrity investigations.

The IBIS Open Forum's Quality Task Group and Model Review Task Group have formulated a quality-control (QC) process using four QC stages, which are described in the "IBIS Quality Specification," Version 2.0 (Reference 2).

The IBIS task groups are subcommittees of TechAmerica's Systems, Standards & Technology Council. Other model users and model makers across the industry have also contributed to this QC process. The four QC stages are:

- Stage 0: An automated quality check using an IBIS parser
- Stage 1: A manual and visual quality check of the model
- Stage 2: Correlation to SPICE or hardware test data
- Stage 3: Correlation to both SPICE and hardware test data

TI performs stages 0, 1, and 2 for its IBIS models, correlating them with SPICE for stage 2. This article will describe the nuances of performing stages 0, 1, and 2 (with SPICE correlation only).

Stage 0: IBIS parsers

The first stage of QC for an IBIS model begins with an IBIS parser program. This computer program provides an essential first-stage model check, inspecting the IBIS file for the validity of the IBIS model data and for syntax errors. This type of program can create "Error," "Warning," and/or "Note" messages in relation to the IBIS model under test, but creating an IBIS model that is free of these messages is possible.

For instance, the parser program IBISCHK4 looks for illegal text types, verifies model types, insures that all proper variables are available for each model, validates end points of data, and performs other housekeeping checks. An example of the results of running an IBISCHK4 program with an IBIS model is shown in the sidebar below.

The "Error," "Warning," and "Note" messages from the parser check provide an opportunity for the IBIS-model designer to identify errors and easily correct them. Running a parser with an IBIS model is essential at the beginning of the quality check; however, the parser does not provide an exhaustive list of IBIS-model errors and does not necessarily guarantee a good model.

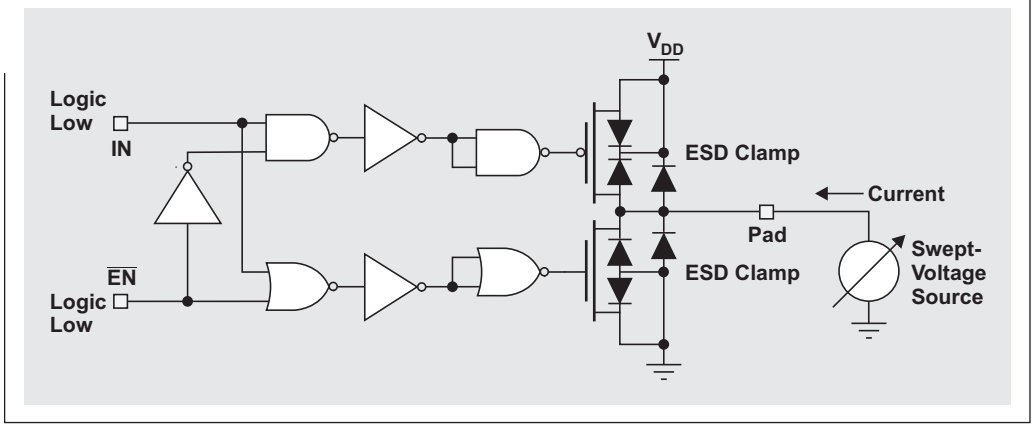
Example IBISCHK4 results

```
ERROR (line 137) - Invalid Model_type ("InputX")
WARNING (line 154) - Vinl should not be specified for model type (null)
WARNING (line 155) - Vinh should not be specified for model type (null)
ERROR - Model 'sdi_3p3': Ramp Not Defined

Errors : 2
Warnings: 2

File Failed
```

Figure 1. Pull-down I-V test circuit for three-state buffer



Parser freeware programs are available for dos32, hp_111, Linux®, and Sun® platforms at the IBIS Open Forum's Web site (http://www.eda.org/ibis). To date there are four parsers available: IBISCHK2, IBISCHK3, IBISCHK4, and IBISCHK5. The level number of each parser program corresponds respectively to the version number of the documented IBIS specification. For example, the most recent parser program, IBISCHK5, corresponds to Version 5.0 of the IBIS specification (Reference 3). TI uses IBISCHK4 and IBISCHK5 to validate its IBIS models.

Stage 1: Visual check

A visual QC check of an IBIS model consists of a manual review of its text and waveforms. During this visual review, the modeling engineer verifies that the header section of the IBIS model contains accurate information. For instance, the header must have the proper products within the product families listed and must have appropriate modeling comments and notes. Following the header, the model must have reasonable package parasitics and well-defined selector entries and must map directly to parameters in the product data sheet, including buffer types, load conditions, input-buffer thresholds, and operating or specified temperature range.

Additionally, the DC and transient waveforms must comply with IBIS standards. The measurement voltage span of the DC waveforms ranges from $-V_{DD}$ to $+2 \times V_{DD}$ (where V_{DD} is the power-supply voltage to the buffer). Across this range, the input and output current must not exceed 2 A. Notes in the comments section in the IBIS model header explain the reason for any excessive currents beyond 2 A. Figure 1 shows the pull-down test configuration for an output buffer, and Figure 2 shows a sample of a pull-down curve from an IBIS model.

Figure 2. Pull-down IBIS graph for DAC7718 output buffer

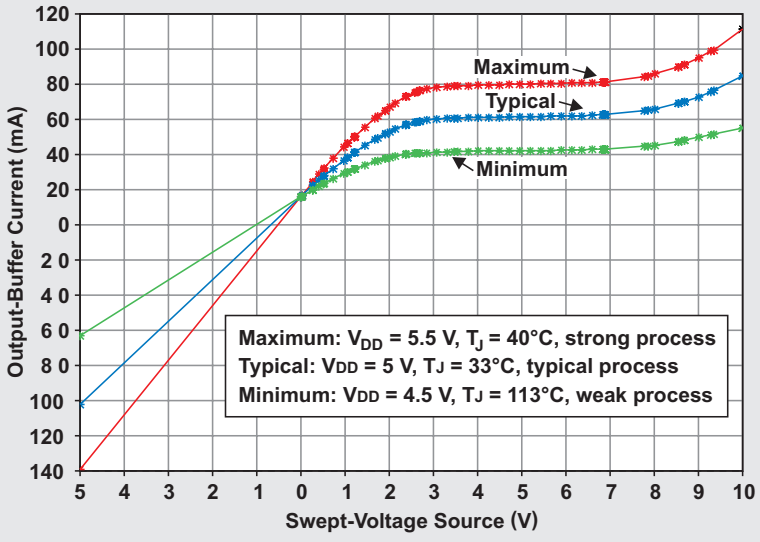


Figure 3. Falling-edge V-t test circuit for an output buffer

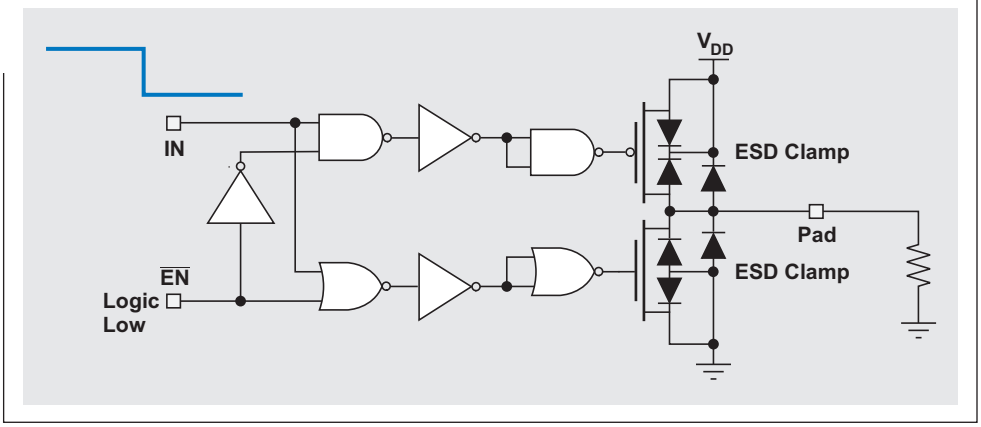


Figure 3 shows the proper test-circuit configuration for the transient falling edge of an output buffer. The resistor following the pad is usually 50 Ω; however, it can be a different value depending on the IC's requirements as stated in the product data sheet.

Figure 4 shows typical falling-edge data for an IBIS model. In this graph, the initial output voltage remains constant for at least two points in time. The data completes its migration to the final value within approximately two-thirds of the total x-axis time.

The text and graphics checks of the IBIS model can be found in Reference 2, where they are described in detail.

Stage 2: Correlation to SPICE or hardware test data

A primary use for IBIS models is to simulate timing and signal integrity, including over/undershoot or crosstalk behavior on an IC's PCB. For stage 2 QC, the modeling engineer compares the performance of an IBIS model in this environment to the device's IC SPICE simulation or test data. The engineer selects appropriate models for a typical board's transmission lines for the specific product under test and compares the test results graphically and with a figure of merit.

Figure 4. DAC7718 input-buffer fall-time analysis

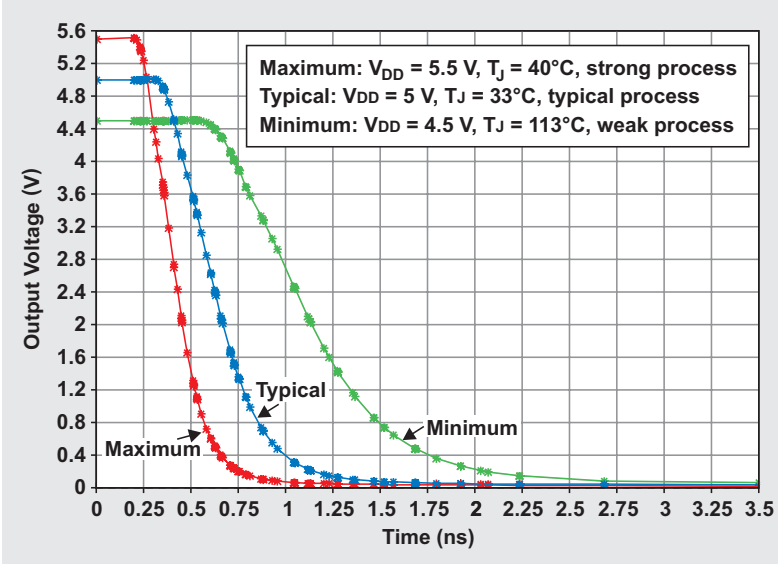


Figure 5 shows an example of a validation test circuit for a SPICE-deck output buffer. This circuit includes the resistive, inductive, and capacitive package parasitics (R_pkg, L_pkg, and C_pkg, respectively) at the output of the SPICE buffer. Following these parasitics is a model of a PCB transmission line, T1. The SPICE simulation collects data at the far end of the transmission line, $V_{(SPICE)}$.

Figure 6 shows an example of an output-buffer IBIS circuit. Notice that the package parasitics do not appear in the circuit, as they are embedded in the IBIS model. This IBIS simulation circuit has the same model of a PCB transmission line (T1) as that in the SPICE-deck simulation circuit.

Figure 7 provides a simulation rise-time comparison between the SPICE and IBIS models based on TI's ADS8319. The outputs were compared at the $V_{(SPICE)}$ node in Figure 5 and the $V_{(IBIS)}$ node in Figure 6. Simulated model conditions were based on a nominal or 1.8-V power supply, a junction temperature of 27°C, and a typical process corner.

Figure 5. Example circuit for SPICE test of an output buffer

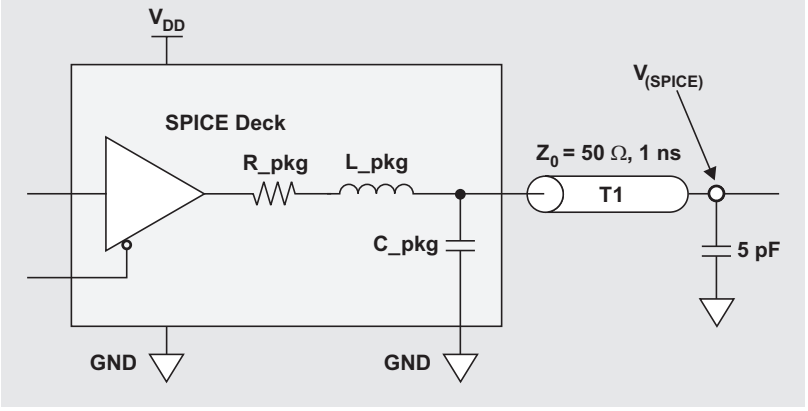


Figure 6. Example circuit for IBIS-model test of an output buffer

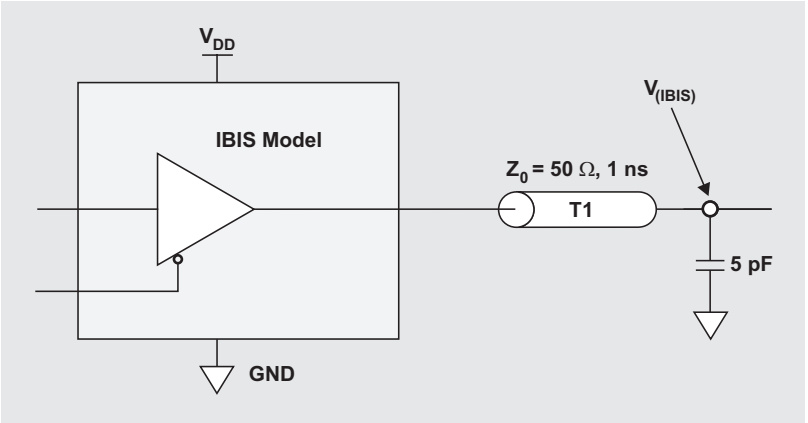


Figure 7. Comparison of output rise times for SPICE and IBIS models

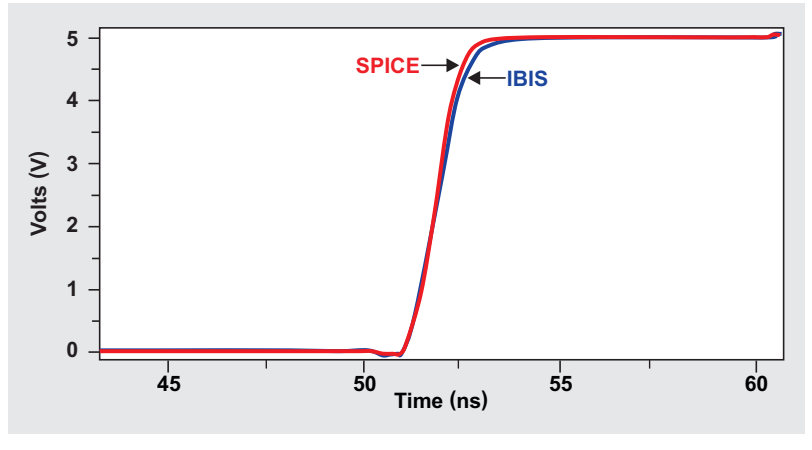


Figure 8. Comparison of output fall times for SPICE and IBIS models

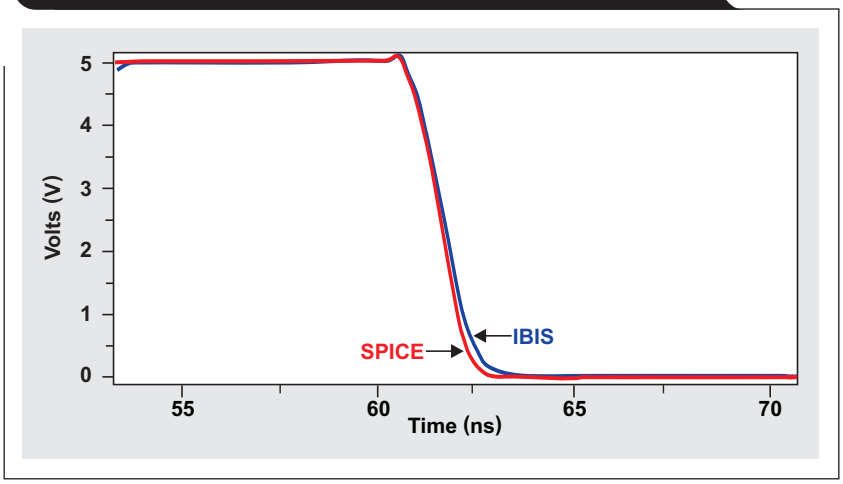


Figure 8 shows a similar fall-time comparison between the SPICE and IBIS models, also based on the ADS8319. Simulated model conditions were based on a 5-V power supply, a junction temperature of 25°C, and a typical process corner.

It is common to calculate a figure of merit (FOM) when curves like those in Figures 7 and 8 are compared. The FOM calculation is

$$FOM = 100 \times \left[1 - \frac{\sum_{i=1}^{N} \left| X_i(\text{golden}) - X_i(\text{DUT}) \right|}{\Delta X \times N} \right],$$

where X_i(golden) is a time sample of the SPICE-deck curve, X_i(DUT) is the matching time sample of the IBIS-model curve, ΔX is the range of data points, and N is the number of samples. The FOM formula compares the two waveforms by summing the absolute value of the x-axis differences between two data points. This sum is divided by the range of the data points as well as by the number of data points. A preliminary numerical task must map each set of data points to a common x-y grid by interpolation. The FOM for the curves in Figures 7 and 8 combined is 0.68%.

Conclusion

In the past, IBIS models have been known to be of poor quality. This lack of quality can be rectified by using the IBIS Open Forum's QC process. At stage 0 in this process, an IBIS parser software finds errors in syntax and in the IBIS model's format. Stage 1 IBIS QC is implemented with a visual inspection of the text and graphics. At stage 2, the IBIS model is mapped back to the product's data sheet. Finally, as the modeling engineer generates IBIS models for SPICE decks, it is important to complete the loop by validating that the IBIS model does match the SPICE-deck performance in a PCB environment. Using stages 0, 1, and 2 to validate the IBIS model insures reliable simulations with signal integrity.

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Related Web sites

dataconverter.ti.com
www.ti.com/sc/device/ADS8319
www.ti.com/sc/device/DAC7718
www.eda.org/ibis

An introduction to the Wireless Power Consortium standard and TI's compliant solutions

By Bill Johns
Senior Applications Engineer

Introduction

Wireless power is beginning to show great potential in the consumer market. The ability to power an electronic device without the use of wires provides a convenient solution for the users of portable devices and also gives designers the ability to develop more creative answers to problems. This technology's benefits can be seen in the many portable devices, from cell phones to electric cars, that normally operate on battery power.

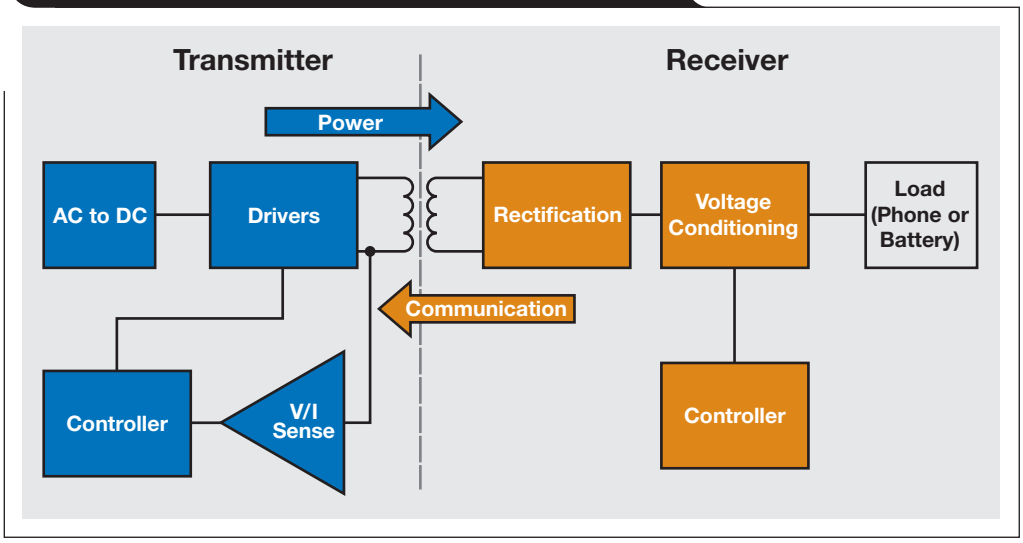
Inductive coupling is the method by which efficient and versatile wireless power can be achieved. For ease of use and the benefit of both designers and consumers, the Wireless Power Consortium (WPC) has developed a standard (see Reference 1) that creates interoperability between the device providing power (power transmitter, charging station) and the device receiving power (power receiver, portable device). Established in 2008, the WPC is a group of Asian, European, and American companies in diverse industries, including electronics manufacturers and original equipment manufacturers (OEMs). The WPC standard defines the type of inductive coupling (coil configuration) and the communications protocol to be used for low-power wireless devices. Any device operating under this standard will be able to pair with any other WPC-compliant device. One key benefit to this approach is that it makes use of the coils for communications between the power transmitter and the power receiver. See Figure 1 for a typical application diagram.

WPC standard for wireless power

Under the WPC standard, "low power" for wireless transfer means a draw of 0 to 5 W. Systems that fall within the scope of this standard are those that use inductive coupling between two planar coils to transfer power from the power transmitter to the power receiver. The distance between the two coils is typically 5 mm. Regulation of the output voltage is provided by a global digital control loop where the power receiver communicates with the power transmitter and requests more or less power. Communication is unidirectional from the power receiver to the power transmitter via backscatter modulation. In backscatter modulation, the power-receiver coil is loaded, changing the current draw at the power transmitter. These current changes are monitored and demodulated into the information required for the two devices to work together.

The WPC standard defines the three key areas of the system—the power transmitter that will supply power, the power receiver that will use the power, and the communications protocol between the two devices. These three areas are explored next.

Figure 1. Typical wireless-power functional diagram



Power transmitter

The direction of power transfer is always from the power transmitter to the power receiver. The key circuits of the power transmitter are the primary coil, used to transfer power to the power-receiver coil; the control unit for driving the primary coil; and the communications circuit for demodulating the voltage or current from the primary coil. Flexibility of the power-transmitter design is limited to provide consistent power and voltage levels to the power receiver.

The power receiver identifies itself to the power transmitter as a compliant device and also provides configuration information. Once the transmitter initiates power transfer, the power receiver sends error packets to the power transmitter requesting more or less power. The power transmitter stops supplying power upon receiving an "End Power" message, or if no packets are received for more than 1.25 seconds. While no power is being transmitted, the power transmitter enters a low-power standby mode.

The WPC specification allows for both fixed- and moving-coil configurations. A single fixed coil, referred to as type A1, is the solution that Texas Instruments (TI) supports.

The power transmitter, typically a flat surface upon which the user places the power receiver, is connected to the power source. The coils of a WPC-compliant device operate as a resonant half bridge on a 50% duty cycle, with a 19-VDC input (±1 V). If more or less power is needed at the power receiver, the frequency in the coil changes but stays between 110 and 205 kHz, depending on power demands.

Power receiver

The power receiver is typically a portable device. The key circuits of the power receiver are the secondary coil, used to receive power from the power-transmitter coil; the rectification circuit, used to convert AC to DC; the power-conditioning circuit, which buffers the unregulated DC into regulated DC; and the communications circuit, which modulates the signal to the secondary coil. The power receiver is responsible for all communications of its authentication and power requirements, as the power transmitter is only a "listener."

While design of the power transmitter is restricted to keep it WPC-compliant, much more freedom is permitted for designing the power receiver. The coil dimension of the power receiver can be adjusted to meet the device's form factor. The coil voltage at the power receiver is full-wave rectified, with a typical efficiency of 70% for a 5-V, 500-mA output. Because communication between the two devices is unidirectional, the WPC selected the power receiver to be the "talker." Inductive power transfer works by coupling a magnetic field from primary to secondary coils. Uncoupled field lines rotate around the primary coil and do not represent loss as long as the field lines don't couple a parasitic load (for example, eddy-current loss in metal).

Communications protocol

The communications protocol includes analog and digital pinging; identification and configuration; and power transfer. A typical start-up sequence that occurs when a power receiver is placed on a power transmitter proceeds as follows:

1. An analog ping from the power transmitter detects the presence of an object.
2. A digital ping from the power transmitter is a longer version of the analog ping and gives the power receiver time to reply with a signal-strength packet. If the signal-strength packet is valid, the power transmitter keeps power on the coil and proceeds to the next phase.
3. During the identification and configuration phase, the power receiver sends packets that identify it and that provide configuration and setup information to the power transmitter.
4. In the power-transfer phase, the power receiver sends control error packets to the power transmitter to increase or decrease the power supply. These packets are sent approximately every 250 ms during normal operation or every 32 ms during large signal changes. Also during normal operation, the power transmitter sends power packets every 5 seconds.
5. To end the power transfer, the power receiver sends an "End Power" message or sends no communications for 1.25 seconds. Either of these events places the power transmitter in a low-power state.

TI's WPC-compliant solutions

TI is a founding member of the WPC and has taken an active role in developing a robust wireless-power specification. TI has developed reliable solutions for both a power receiver and a power transmitter in the form of three newly developed ICs. The power receiver uses the MSP430bq1010 and bq25046 devices. The power transmitter is based on the bq500110, which supports type A1 (single-coil) configurations. Both receiver and transmitter ICs are designed to be interoperable with other WPC-compliant solutions.

The MSP430bq1010 in the power receiver handles all of the logic functions and communications. The onboard analog-to-digital converters monitor the levels of voltage into and current out of the bq25046. The bq25046 provides load-current information to the MSP430bq1010, which then uses this information to control the power transmitter's operating point. The bq25046 provides a low-current, 3.3-V low-dropout regulator (LDO) to power the MSP430bq1010 and logic circuit, while a larger 5.0-V LDO is capable of providing up to 1 A of current to the main output.

The power-transmitter solution is provided with the bq500110. This device demodulates and decodes serial data from the power receiver. The control circuits first

certify that the power receiver is indeed a WPC-compliant device, then configure the power transmitter accordingly.

TI's BQTESLA100LP EVM kit combines separate transmitter and receiver designs into a single kit that includes mechanical packaging. This kit can be used for evaluation of the ICs or as a design example. The WPC has certified that both the power-transmitter and the power-receiver solutions meet the Version 1.0 specification. No software is required to operate the EVM, which needs only a 19-V input. The EVM kit's output will be 5 V at up to 1 A. The transmitter EVM includes multiple LED options for visual indication of power-transmission status. Also, two buzzer options provide audio indication of the start of power transfer.

Conclusion

The WPC standard is a set of guidelines that allows manufacturers to develop solutions with the confidence that their components will mesh with a variety of other WPC-certified components designed for inductive power transfer.

References

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Replace *partnumber* with bq25046, bq500110, or MSP430bq1010

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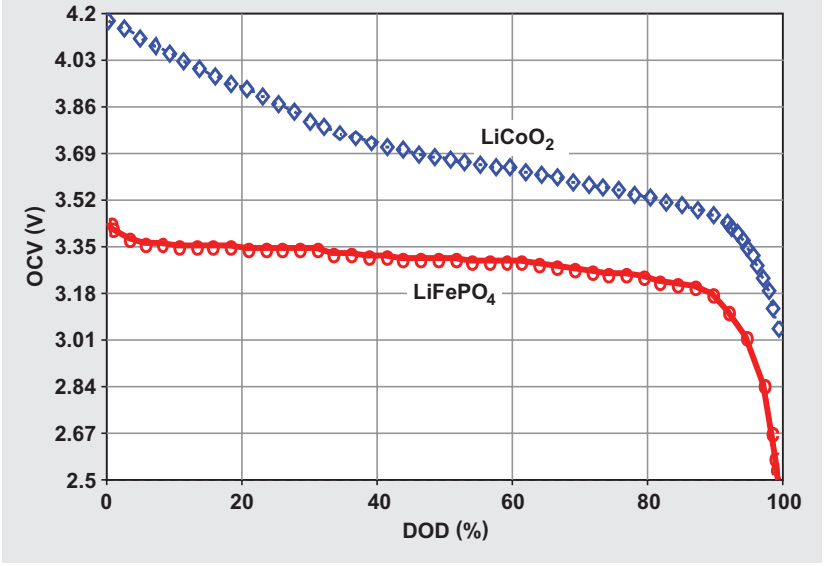
By Keith James Keller
Analog Field Applications

The Impedance Track™ battery-fuel-gauging technology from Texas Instruments (TI) is a powerful adaptive algorithm that learns how a battery's characteristics change over time. Combining this algorithm with knowledge of the battery pack's specific chemistry permits a very accurate determination of the battery's state of charge (SOC) for the life of the pack.

However, certain conditions are required for updating information about the total chemical capacity (Q_{max}) of the cell. This becomes more difficult with the extremely flat voltage profile of lithium-iron-phosphate ($LiFePO_4$) cells (see Figure 1), especially if it is not possible to fully discharge the battery and let it rest for several hours. Figure 1 shows typical open-circuit voltage (OCV) characteristics versus depth of discharge (DOD) for $LiCoO_2$ and $LiFePO_4$ battery chemistries. This article builds on the discussions about Impedance Track technology in References 1 and 2.

Figure 1. Battery OCV measurements based on DOD



TI recommends using the Impedance Track 3 (IT3) algorithm with any $LiFePO_4$ cell. The IT3's improvements to earlier Impedance Track algorithms include:

- Better cold-temperature performance from improved temperature compensation
- Added filtering to prevent capacity jumps in SOC
- Improved accuracy for unfavorable OCV readings with $LiFePO_4$ cells
- Conservative remaining-capacity estimation with additional load-selection configurations

IT3 is included in TI's bq20z4x, bq20z6x, and bq27541-V200 gas gauges (not a comprehensive list).

Typical conditions for Q_{max} update

The Impedance Track algorithm defines Q_{max} as the total chemical capacity of a cell, measured in milliampere-hours (mAh). For a proper Q_{max} update, two conditions must be met:

1. Two OCV measurements must be taken outside of the disqualified voltage range, which is based on the cell's chemical identification (ID) number established by TI. An OCV measurement can be done only on a relaxed cell that has not been charged or discharged for several hours.

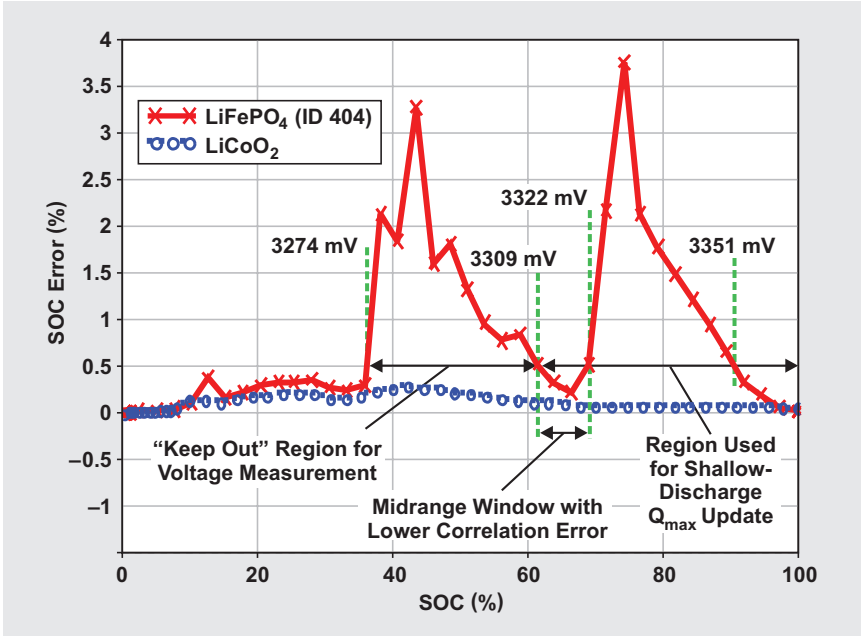
Reference 3 lists a subset of the disqualified voltage ranges, some of which are shown in Table 1. It can be seen that, for chemical ID 100, no OCV measurements are allowed if any cell voltages are above 3737 mV or below 3800 mV. This is essentially a "keep out" range for OCV measurements for best accuracy. Even though an SOC percentage is given in this article, the gauge determines disqualification based only on voltage.

2. A minimum amount of passed charge must be integrated by the fuel gauge. By default, it is set at 37% of the total cell capacity. This percentage of passed charge can be decreased to as low as 10% for a shallow-discharge Q_{max} update. This decrease will be at the expense of SOC accuracy but will be tolerable in a system that would not otherwise be able to update Q_{max}.

Table 1. Excerpt from Reference 3 showing disqualified voltage ranges based on chemistry for Q_{max} update

Description	Chemical ID	Vqdis_min (mV)	Vqdis_max (mV)	SOC_min, %	SOC_max, %
LiCoO2/graphitized carbon (default)	100	3737	3800	26	54
Mixed Co/Ni/Mn cathode	101	3749	3796	28	51
Mixed Co/Mn cathode	102	3672	3696	6	14
LiCoO2/carbon 2	103	3737	3800	26	54
Mixed Co/Mn cathode 2	104	4031	4062	77	88
LiFePO4/carbon	**404**	**3274**	**3351**	**34**	**93**
LiFePO4/carbon	409	3193	3329	12	92

Figure 2. SOC correlation error for 1-mV voltage error



Now that we have an understanding of what is required for a shallow-discharge Q_{max} update, let's look at an example of data-flash parameters that need to be changed in a configuration with a lower-capacity pack. The default Impedance Track algorithm is based on typical laptop battery packs having 2 parallel strings of 3 cells in series (3s2p). Each string has a 2200-mAh capacity, giving a total capacity of 4400 mAh. $LiFePO_4$ cells have approximately half of that capacity, so if they are used in a 3s1p configuration, the total pack capacity will be 1100 mAh. With smaller-capacity packs like this, specific data-flash parameters need to be fine-tuned in TI's gas-gauge evaluation software for optimal performance. The remainder of this article describes this process.

Example calculations

Consider a 3s1p-configuration battery pack using A123 Systems™ 1100-mAh 18650 $LiFePO_4$/carbon cells. TI's chemical ID number for this cell type is 404. This battery will be used in a storage system with normal temperatures of around 50°C. The discharge rate is 1C, and a 5-mΩ sense resistor is used with the gauge for coulomb counting.

As can be seen in Table 1, the disqualified voltage range for OCV measurements for chemical ID 404 is 3274 mV minimum (~34% SOC) and 3351 mV maximum (~93% SOC). Most $LiFePO_4$ cells have a very wide disqualified voltage range (see chemical ID 409 as a comparison). However, depending on the cell characteristics, it may be possible to identify a higher minimum disqualified voltage for a shallow-discharge Q_{max} update. For chemical ID 404 it is possible to raise this value to 3322 mV, allowing for a shallow Q_{max}-update window from 3309 to 3322 mV (see Figure 2). The designer can use this midrange low-error window with data-flash modifications. Since only a high and low disqualified voltage range can be programmed, the host system must guarantee that the lower OCV measurement will not happen below 3309 mV. (As the correlation error increases, OCV-measurement error increases dramatically between 3274 and 3309 mV.) Even though there is only a 13-mV window to work with for the lower OCV measurement (3322 – 3309 mV = 13 mV), it corresponds to an SOC range of 70% to 64%.

$LiFePO_4$ cells have a very long relaxation time, so let's increase the data-flash parameter "OCV Wait Time" to 18,000 seconds (5 hours). Since the battery's normal

operating temperature is elevated, the parameter "Q Invalid Max Temperature" should be changed to 55°C. Additionally, "Q_{max} Max Time" should be changed to 21,600 seconds (6 hours).

To decrease the Q_{max} passed charge from 37% to 10%, the "DOD Max Capacity Error," "Max Capacity Error," and "Q_{max} Filter" need to be modified, as they all play a part in the disqualification time between the OCV1 and OCV2 measurements. "Q_{max} Filter" is a compensation factor that varies Q_{max} relative to passed charge.

The goal of these parameters is to have less than 1% "Max Capacity Error" based on measured passed charge and including ADC maximum offset error ("CC Deadband"). However, these values need to be changed to allow for the shallow-discharge Q_{max} update.

Example 1: Time-out period for Q_{max} update

To have less than 1% of accumulated error across a 10-mΩ sense resistor with a 1000-mAh cell and "CC Deadband" set by the hardware to a fixed value of 10 µV, the time-out period for the Q_{max} update can be determined as follows:

10 µV/10 mΩ = 1-mA offset current.

1000-mAh capacity × 1% allowed error = 10-mAh capacity error.

10-mAh capacity error/1-mA offset current = 10 hours.

Therefore, from start to finish, including rest periods, only 10 hours are available to complete a Q_{max} update. After the 10-hour time-out, once the gauge takes its next proper OCV reading, this timer will restart.

Example 2: Modifying data-flash parameters

In the design scenario using 1100-mAh cells with a 5-mΩ sense resistor, the time-out period for the Q_{max} update is determined in the same way:

10 µV/5 mΩ = 2-mA offset current.

1100 mAh × 1% = 11 mAh.

11 mAh/2-mA offset current = 5.5 hours.

In this case, the percentage of capacity error needs to be relaxed to increase the Q_{max} time-out. Changing the "Max Capacity Error" to 3% (from the default of 1%) gives

1.1 Ah × 3% = 33 mAh,

which will increase the Q_{max} disqualification time to

33 mAh/2-mA capacity error = 16.5 hours.

The "DOD Capacity Error" needs to be set to twice the "Max Capacity Error," so let's change it to 6% (from the default of 2%).

The default value of 96 for "Q_{max} Filter" needs to be decreased proportionally, based on the percentage of passed charge:

"Q_{max} Filter" = 96/(37%/10%) = 96/3.7 = 26

Table 2 shows typical data-flash parameters in gas-gauge evaluation software that must be modified to implement a shallow-discharge Q_{max} update. These particular parameters are protected (classified as "hidden") but can be unlocked by TI's applications staff. The example battery pack used for this table is the one mentioned earlier,

Table 2. Protected data-flash parameters that can be changed by TI applications staff based on system usage

DATA-FLASH PARAMETER	DEFAULT VALUE	NEW VALUE
Min % Passed Charge for Q_{max}	37%	10%
Min % Passed Charge for 1st Q_{max}	90%	Keep default at 90%[1]
Q Invalid MaxV	3351 mV (chemical ID 404 default)	Keep chemical ID 404 default at 3351 mV
Q Invalid MinV	3274 mV (chemical ID 404 default)	3322 mV
OCV Wait Time	1800 seconds	18,000 seconds
DOD Capacity Err	2%	6%
Q_{max} Max Time	18,000 seconds	21,600 seconds
Max Capacity Error	1.0%	3.0%
Q_{max} Filter	96	26
Q Invalid MaxT	40.0°C	55.0°C
Q Invalid MinT	10.0°C	Keep default at 10.0°C[2]

[1] This parameter is important during the golden-image process. If a standard 4.2-V Li-ion cell is being used and charged only to 4.1 V in-system, it is still necessary for the first Q_{max} update to occur after the cell is charged to 4.2 V to meet the requirement for a 90% change in capacity. The capacity change is checked against both the specified cell capacity, or "Design Capacity," and the estimated DOD for the start and end points based on the chemical ID number programmed in the gauge.

[2] A wide-ranging temperature change can cause errors when Q_{max} is calculated. In a system with normal operation at high or low temperatures, it is necessary to modify this parameter.

a 3s1p pack using A123 1100-mAh 18650 $LiFePO_4$/carbon cells with chemical ID 404.

Events of Q_{max} update

The following events describe a practical approach to achieving a Q_{max} update after the data-flash parameters described in Examples 1 and 2 have been changed.

1. A Q_{max} update should start when the battery voltages are within the low-correlation-error window as shown in Figure 2. The designer's own algorithm can be used to discharge/charge the cells into this range.*
2. In this example, to be in the valid measurement range (for chemical ID 404), all cell voltages must be greater than or equal to 3309 mV and less than or equal to 3322 mV. If cell voltages happen to relax outside the valid range during the discharge routine, another discharge or charge cycle must be started prior to the programmed "OCV Wait Time" of 18,000 seconds. If all cell voltages are within 3309 to 3322 mV after 6 hours and 10 minutes, a proper OCV measurement has been taken.
3. The next step is to fully charge the battery. Once the battery is full, or at 100% SOC, it should rest for another 6 hours and 10 minutes before the second OCV measurement is taken. The Q_{max} value will then be updated. If charging takes approximately 2 hours, then a minimum of 8 hours will be needed for the time-out period. From the calculation of the 16.5-hour time-out period in Example 2, we know there is more than enough time with an additional cushion of 8.5 hours.
4. The OCV timer can always be reset by issuing the gas gauge a ResetCommand (0x41) while the gauge is in unsealed mode.

Table 3 shows the results from cycling the battery as just described when the example pack configuration is used.

Table 3. Results from full-cycle and shallow-charge Q_{max} updates

	NORMAL CHARGE CYCLE[1]	SHALLOW CHARGE CYCLE	
	UPDATED Q_{max} (mAh)	UPDATED Q_{max} (mAh)	RESTING VOLTAGE BEFORE CHARGING (mV)
Cell 0	1062	1062	3312
Cell 1	1066	1038	3310
Cell 2	1064	1063	3311
Pack	1062 (cell minimum)	1038 (cell minimum)	9933 (total)

[1]Charging from empty after rest to full charge with rest.

Conclusion

TI's Impedance Track technology is a very accurate algorithm for determining battery SOC over the life of the cell. In $LiFePO_4$ applications where a full discharge of the battery with a rest period is not possible, it is necessary to explore a shallow-discharge option for the Q_{max} update. This article has described the considerations and data-flash programming configurations for implementing a shallow-discharge Q_{max} update. Changes to these parameters must be approved by TI applications staff based on system configuration and requirements.

References

For more information related to this article, you can download an Acrobat® Reader® file at www.ti.com/lit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Theory and implementation of Impedance Track™ battery fuel-gauging algorithm in bq20zxx product family," Application Report . .	slua364
2. Keith James Keller, "Fuel-gauging considerations in battery backup storage systems," *Analog Applications Journal* (1Q 2010)	slyt364
3. chemistry_specific_Qmax_disqv_voltages_table.xls [Online]. Available: http://www.ti.com/litv/zip/slua372r	—

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with BQ20Z40-R1 or BQ27541-V200

*Because of the long voltage hysteresis of $LiFePO_4$ cells after charge or discharge, it is preferable to discharge the battery only into the shallow-discharge range. It is okay to charge the battery during the hone-in algorithm as long as the voltage does not rise above the specified "Q Invalid Max Voltage" at any time. It is also permissible to have multiple discharges to get the cells into the range of 3309 to 3322 mV after the OCV wait time.

Designing an isolated I²C Bus® interface by using digital isolators

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The continuing changes in legislation concerning both the design and use of machinery and equipment require the isolation of almost any type of industrial system or interface. The inter-integrated circuit bus (I²C Bus®) is a single-ended, multi-master, two-wire bus; and, while designed only for short-distance I²C communication, it is no exception to isolation requirements.

The particular challenge in designing an isolated I²C interface by using standard digital isolators lies in the different operation modes between the two. The I²C Bus operates in bidirectional, half-duplex mode, while standard digital isolators are unidirectional devices. To make efficient use of one technology supporting the other, external circuitry is required that separates the bidirectional bus into two unidirectional signal paths without introducing significant propagation delay.

This article provides a short introduction to I²C Bus operation and then describes how to design an isolated I²C interface by adding only a few external components to a digital capacitive isolator.

I²C Bus operation

The I²C uses open-drain technology, thus requiring the serial data line (SDA) and serial clock line (SCL) to be connected to V_{DD} by resistors (see Figure 1). Pulling the line to ground is considered a logic "0," and letting the line float is a logic "1." This logic configuration is used as a channel-access method. Transitions of logic states must occur while SCL is low, because transitions while SCL is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted.

I²C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified total bus capacitance of 400 pF, which restricts communication distances to a few meters. The specified signaling rates are 100 kbps (standard mode), 400 kbps (fast mode), 1 Mbps (fast mode plus), and 3.4 Mbps (high-speed mode).

Figure 1. The I²C Bus®

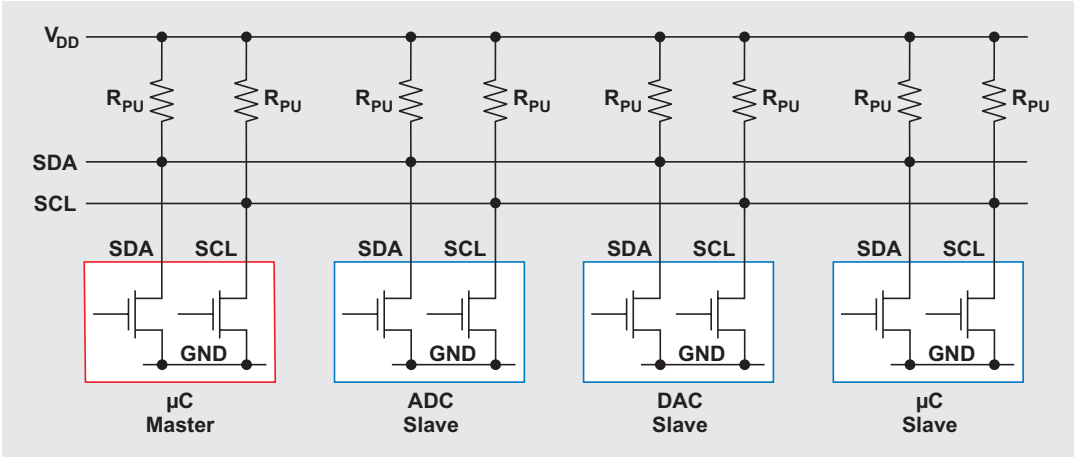
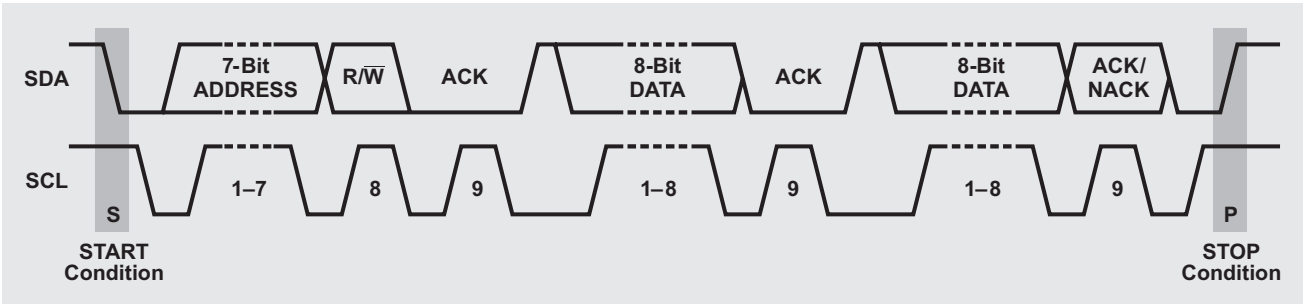


Figure 2. Timing diagram of a complete data transfer



The bus has two roles for nodes: master and slave. A master issues the clock and slave addresses and also initiates and ends data transactions. A slave receives the clock and addresses and responds to requests from the master. Figure 2 shows a typical data transfer between master and slave.

The master initiates a transaction by creating a START condition, then transmits the 7-bit address of the slave it wishes to communicate with. This is followed by a single READ/WRITE (R/W) bit, representing whether the master wishes to write to "0" or to read from "1," the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge (ACK) bit by pulling SDA low during the entire high time of the ninth clock pulse on SCL. Then the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and 8-bit data bytes are sent with the most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte to the slave, which sends an ACK bit for each byte received. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave while sending an ACK bit to acknowledge the receipt of every byte but the last one (see Figure 3). In this situation the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit or may send another START bit to maintain bus control for further transfers.

When writing to a slave, a master mainly operates in transmit mode and changes to receive mode only when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit mode and then changes to receive mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note that the master ends a reading sequence by not acknowledging the last byte received—i.e., by sending a NACK bit. This procedure resets the slave state machine and allows the master to send the STOP command.

Figure 3. Changes in transmit/receive modes during a data transfer

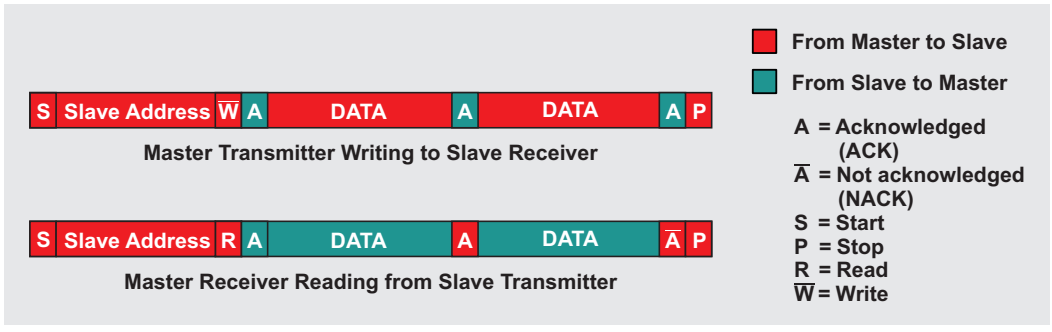
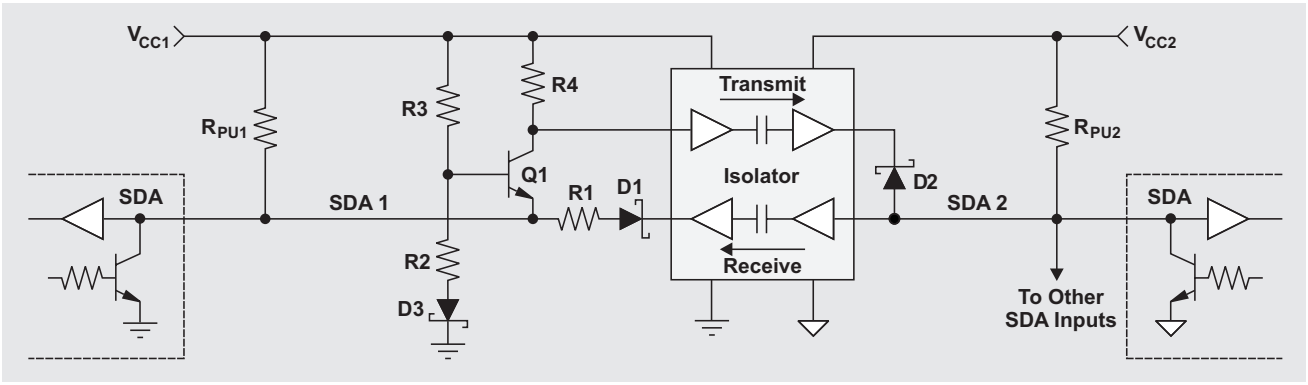


Figure 4. Isolating an I²C line by using a digital isolator



Isolator design

Isolating an I²C signal path by using standard digital isolators requires splitting the half-duplex line into separate transmit and receive paths and converting the isolator's push-pull outputs into open-collector outputs via Schottky diodes (Figure 4). To prevent a transmitted signal from feeding back to its source, a comparator function is implemented that detects the direction of the signal flow and switches the signal paths accordingly.

Transistor Q1 and its surrounding resistor network provide the comparator function. Since the dominant switching level in I²C is logic low, the base of Q1 is so biased that a low level applied to SDA1 turns the transistor on, and a low level sent from SDA2 keeps Q1 at high impedance. While the R3/R2 voltage divider primarily determines the biasing, diode D3 provides temperature compensation. To prevent SDA2 from turning Q1 on, the low-level output at D1 is raised by a voltage drop across R1, which raises Q1's emitter potential, V_E, and decreases the base-emitter voltage below the minimum turn-on level. However, care must be taken to maintain V_E below the minimum input high-level threshold of SDA1, which the I²C specification lists as $V_{IHmin} = 0.3 \times V_{CC}$.

So, when the I²C Bus at SDA2 is pulled low, the low state passing in receive direction causes a voltage increase at SDA1 that is just enough to block Q1 but well below V_{IHmin}, thus presenting a valid low for an I²C input. At the same time, R4 provides a logic high to the isolator input in transmit direction, preventing diode D2 from conducting. Once SDA2 is released and returns to the level of V_{CC2}, SDA1 follows after one propagation delay through the isolator. When the isolator is driven from the bus side (SDA2), the added signal delays for both the falling and the rising edges mainly consist of only one propagation delay through the isolator.

In the opposite direction, when SDA1 is pulled low, its maximum low-level output, V_{OLmax}, is significantly lower than V_E and causes Q1 to conduct. The low-state signal passing through the isolator in transmit direction forward biases D2, and SDA2 goes low. However, when SDA1 is released, its voltage cannot return to the level of V_{CC1} immediately due to the remaining low-level signal at SDA2. Instead, SDA1 rises to the necessary V_E potential that blocks Q1, and it will stay at this level until a high-impedance Q1 allows R4 to provide a logic high to the isolator input, thus releasing SDA2 and D1. Only then will SDA1 be able to return to the level of V_{CC1}.

When the isolator is driven from the device side (SDA1), the added signal delays for both edges increase due to the involvement of the comparator function.

Figure 5. Final isolator circuit

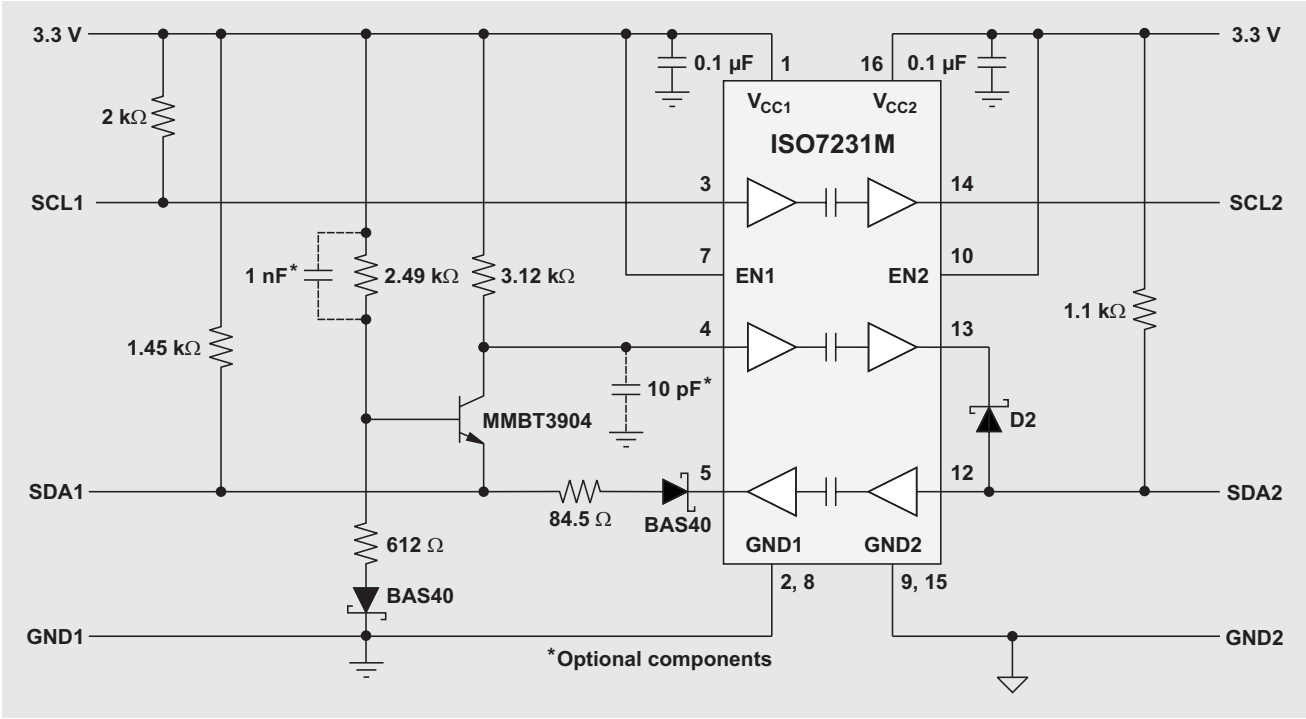


Figure 5 shows the final isolator circuit for the majority of I²C applications where the master is isolated from a slave bus. In this case, only the SDA line is bidirectional, while the SCL is unidirectional. For a multi-master system in which both lines must be bidirectional, the SDA circuit design can also be applied to the SCL when an ISO7242M isolator is used.

The typical propagation delays listed in Table 1 were measured under light capacitive loading at SDA1 and SDA2. Note that at low supply voltages, switching transients at Q1's collector might require a 10-pF filter capacitor to avoid false triggering of the internal isolator logic. Also, propagation delays can be reduced by switching a capacitor parallel to the upper base resistor to increase the charge injection into Q1's base.

Table 1. Propagation delays

SDA1 TO SDA2		SDA2 TO SDA1		CONDITION
RISING EDGE (ns)	FALLING EDGE (ns)	RISING EDGE (ns)	FALLING EDGE (ns)	
121	124	113	82	No caps
136	140	113	82	10 pF
103	136	113	82	10 pF + 1 nF
86	140	113	82	1 nF

Related Web sites

interface.ti.com
www.ti.com/sc/device/ISO7231M
www.ti.com/sc/device/ISO7242M

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