Virtex-6 FPGA GTX Transceiver Characterization Report

PCI Express 2.0 (2.5 and 5.0 Gb/s) Electrical Standard

RPT121 (v1.0) November 3, 2010

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/03/10	1.0	Initial Xilinx release.

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Virtex-6 FPGA GTX Transceiver Characterization Report for the PCI Express 2.0 Electrical Standard

Introduction

This characterization report compares the electrical performance of the Virtex®-6 FPGA GTX transceiver against the PCI Express® Revision 2.0 specifications published in the *PCI Express Base Specification, Revision 2.1* and the *PCI Express Card Electromechanical Specification, Revision 2.0*. All testing for this report is based on line rates of 2.5 and 5.0 Gb/s across voltage, temperature, and worst-case transceiver performance corners.

This report includes test results for these PCI Express, Revision 2.0 specifications:

Test Conditions

Table 1 and Table 2 show the supply voltage and temperature conditions used in the characterizations, respectively. All combinations of voltage and temperature conditions are used for the tests performed.

Table 1: **Supply Voltage Test Conditions**

Condition	MGTAVCC (V)	MGTAVTT (V)
V_{MIN}	Note(1)	1.14
V_{MAX}	Note(1)	1.26

Notes:

1. Refer to DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*, for the MGTAVCC values.
2. Other FPGA voltages stay at their nominal values during the test.

Table 2: **Temperature Test Conditions**

Condition	Temperature (°C)
T_{-40}	–40
T_0	0
T_{100}	100

Transceiver Selection

Xilinx first performs volume generic transceiver characterization across process, voltage, and temperature. The generic data can be found in RPT120, *Virtex-6 FPGA GTX Transceiver Characterization Report*. Protocol-specific characterization is subsequently performed using representative transceivers from generic characterization.

The chosen Virtex-6 FPGA GTX transceiver channels represent a mixture of transmitters and receivers having worst-case and typical performance based on volume generic characterization data. Transceivers with the worst performing transmitter output jitter and receiver jitter tolerances are selected within the worst-case distribution of the transceivers found in the generic volume characterization. The histograms in this characterization report do not show a true statistical representation normally present in a random (or even typical) population. The histograms are skewed toward the worst-case performance because of the transceiver selection process and are not representative of the typical production silicon.

Summary of Results

Table 3 and Table 4 show the tested Virtex-6 FPGA GTX transceiver performance results against the *PCI Express Base Specification, Revision 2.1* and the *PCI Express Card Electromechanical Specification, Revision 2.0*. The data reported in these tables represents the values obtained under the worst-case voltage, temperature, and performance corner conditions.

Table 3: **PCI Express 2.0 Characterization Summary of Results for 2.5 Gb/s Line Rate**

Test Name	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Unit Interval(1)	Minimum	399.88	400.03	ps	Yes
	Maximum	400.12	400.04	ps	Yes
Template Tests(1)	Maximum	Zero Mask Failure	Zero	Number of failures	Yes
Peak Differential Output Voltage(1)	Minimum	360	Programmable	mV	Yes
	Maximum	1200	Programmable	mV	Yes
Minimum Eye Width(1)	Minimum	287	334.6	ps	Yes
Median to Max Jitter(1)	Maximum	56.5	30.08	ps	Yes
TX Differential Return Loss	Frequency Profile	See Figure 20		dB	Yes
TX Common Mode Return Loss	Frequency Profile	See Figure 21		dB	Yes
PLL Bandwidth	Minimum	1.5	4.00	MHz	Yes
	Maximum	22	15.00	MHz	Yes
PLL Peaking	Maximum	3	1.32	dB	Yes
RX Differential Return Loss	Frequency Profile	See Figure 34		dB	Yes
RX Common Mode Return Loss	Frequency Profile	See Figure 35		dB	Yes

Notes:

1. Part of the Add-in Card Transmitter test for PCI Express, Revision 2.0.

Table 4: **PCI Express 2.0 Characterization Summary of Results for 5.0 Gb/s Line Rate**

Test Name	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Unit Interval(1)	Minimum	199.94	200.01	ps	Yes
	Maximum	200.06	200.01	ps	Yes
Template Tests(1)	Maximum	Zero Mask Failure	Zero	Number of failures	Yes

Table 4: **PCI Express 2.0 Characterization Summary of Results for 5.0 Gb/s Line Rate *(Cont'd)***

Test Name	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Peak Differential Output Voltage(1)	Minimum	380	Programmable	mV	Yes
	Maximum	1200	Programmable	mV	Yes
Minimum Eye Width(1),(2)	Minimum	126	131.94	ps	Yes
Deterministic Jitter(1),(2)	Maximum	54	15.88	ps	Yes
Total Jitter at BER^{-12}(1),(2)	Maximum	74	68.06	ps	Yes
TX Differential Return Loss	Frequency Profile	See Figure 20		dB	Yes
TX Common Mode Return Loss	Frequency Profile	See Figure 21		dB	Yes
PLL Bandwidth	Minimum	5	5.48	MHz	Yes
	Maximum	16	14.00	MHz	Yes
PLL Peaking	Maximum	1	0.96	dB	Yes
RX Input Jitter Tolerance	TJ (not including SJ)	See Table 18(3)		UI	Yes
	SJ at 22.82 MHz(4)	Not defined	0.22	UI	Yes
RX Differential Return Loss	Frequency Profile	See Figure 34		dB	Yes
RX Common Mode Return Loss	Frequency Profile	See Figure 35		dB	Yes

Notes:

1. Part of the Add-in Card Transmitter test for PCI Express, Revision 2.0.
2. Without crosstalk.
3. Total jitter components and amplitude specification limits are defined in the table called "5.0 GT/s Tolerancing Limits for Common Refclk Rx Architecture" from the *PCI Express Base Specification, Revision 2.1.*
4. BER = 10^{-12}.

Electrical Characterization Details

This section describes the test methodology used to characterize the Virtex-6 FPGA GTX transceiver's performance against the *PCI Express Base Specification, Revision 2.1* and the *PCI Express Card Electromechanical Specification, Revision 2.0*. The Virtex-6 FPGA GTX transceiver under test is configured using the default PCI Express setting generated from the Virtex-6 FPGA GTX Transceiver Wizard, version 1.6. The Virtex-6 FPGA GTX transceiver attribute settings that differ from the Wizard default settings are identified in the "Test Setup and Conditions" table for each test. Table 5 shows the PLL settings used in the characterization. This characterization report is based on the 100 MHz reference clock. The 125 MHz and 250 MHz reference clock PLL settings are provided as a comparison.

Table 5: **PLL Settings for 2.5 Gb/s and 5.0 Gb/s Line Rate**

Data Rate (Gb/s)	PLL Frequency (GHz)	Reference Clock Frequency (MHz)	Reference Clock Divider: M(1)	PLL Feedback Dividers: N1(2) x N2(3)	PLL Output Divider: D(4)
2.5	2.5	100	1	5 x 5 = 25	2
2.5	2.5	125	1	5 x 4 = 20	2
2.5	2.5	250	1	5 x 2 = 10	2
5.0	2.5	100	1	5 x 5 = 25	1
5.0	2.5	125	1	5 x 4 = 20	1
5.0	2.5	250	1	5 x 2 = 10	1

Notes:

1. M = [TX/RX]PLL_DIVSEL_REF.
2. N1 = [TX/RX]PLL_DIVSEL45_FB.
3. N2 = [TX/RX]PLL_DIVSEL_FB.
4. D = [TX/RX]PLL_DIVSEL_OUT.

Add-in Card Transmitter Test

Test Methodology

The Add-in Card Transmitter test for the 2.5 Gb/s line rate comprises the unit interval, template tests, peak differential output voltage, eye width, and median to maximum jitter tests. For the 5.0 Gb/s line rate, the test comprises the unit interval, template tests, peak differential output voltage, eye width, deterministic jitter, and total jitter tests. These tests are compared against the *PCI Express Card Electromechanical Specification, Revision 2.0*. The Add-in Card Transmitter specification for the 2.5 and 5.0 Gb/s line rates is defined in Table 6 and Table 7, respectively.

Table 6: **Add-in Card Transmitter Specification for the 2.5 Gb/s Line Rate**

Test Name	Specification Range	Units
Unit Interval (UI)	399.88 to 400.12	ps
Template Tests	Zero Eye Mask Failures	Number of failures
Peak Different Output Voltage	360 to 1200	mV
Eye Width	287 (minimum)	ps
Median to Maximum Jitter	56.5 (maximum)	ps

Table 7: **Add-in Card Transmitter Specification for the 5.0 Gb/s Line Rate**

Test Name	Specification Range	Units
Unit Interval (UI)	199.94 to 200.06	ps
Template Tests	Zero Eye Mask Failures	Number of failures
Peak Different Output Voltage	380 to 1200	mV
Eye Width(1)	126 (minimum)	ps
Deterministic Jitter(1)	54 (maximum)	ps
Total Jitter at BER^{-12}(1)	74 (maximum)	ps

Notes:

1. Without crosstalk.

These tests are performed using the test setup shown in Figure 1. An Agilent Infiniium DSA91304A Digital Signal Analyzer installed with a PCI Express automated test application performs the Add-in Card Transmitter test using the test methodology defined in the PCI-SIG® document *PCI Express 2.0 CEM Signal Quality Testing for Add-in Cards using Agilent DSO91304A*, and *DSA91304A 13 GHz Real-Time Oscilloscopes*. Agilent DSA91304A Analyzer calibration is performed prior to data collection.

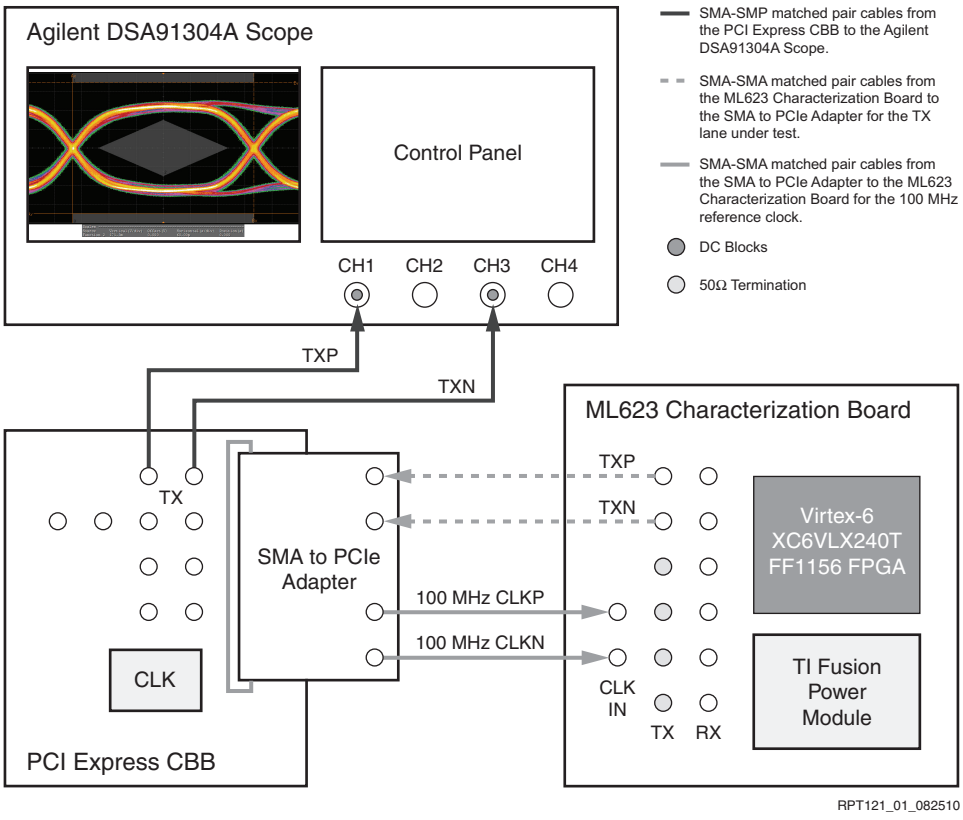

Figure 1: **Add-in Card Transmitter Test Setup Block Diagram**

The Virtex-6 device under test is configured to PCI Express mode and set to transmit the PCI Express compliance pattern on all available TX lanes of the ML623 Virtex-6 FPGA GTX Transceiver Characterization Board. Table 8 defines the test setup and conditions for the Add-in Card Transmitter test.

Table 8: **Add-in Card Transmitter Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent Infiniium DSA91304A Digital Signal Analyzer: • AC coupled using DC blocks.

Software Application	• Agilent N5393B PCI Express Automated Test Application Version 2.10:
	  • Installed on the Agilent DSA91304A scope to automate the Add-in Card Transmitter test.
	  • PCI-SIG accepted methodology.
	• SIGTEST 3.1.9:
	  • Used only to compare the measurement results with the Agilent PCI Express automated test application.
	  • Uses the setup described in Figure 1.
	  • PCI-SIG accepted methodology.

Voltage	TI Fusion Power Module: • Installed on the ML623 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and V_{MAX}.
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, and T_{100}.
Data Pattern	Transmitting the PCI Express compliance pattern on all available TX lanes of the ML623 board.
FPGA	Virtex-6 FPGA XC6VLX240T FF1156.

Load Boards	• ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C:
	  • 50Ω terminator on TX channels not under test.
	  • On the various ML623 board channels used, there are about 4 to 8 inches of FR4 in the TX paths.
	• PCI Express Compliance Base Board (CBB), Revision 2.0:
	  • Standard PCI-SIG board for the Add-in Card Transmitter Test.
	• SMA to PCIe® Adapter, Revision D:
	  • Used to connect the ML623 board to the x16 interface of the PCI Express CBB.

Cables	• One pair of matched 50Ω Rosenberger SMA-SMP cables from the PCI Express CBB to the Agilent DSA91304A oscilloscope. • One pair of matched 50 Ω SMA-SMA cables from the SMA to PCIe Adapter to the ML623 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the ML623 board to the SMA to PCIe Adapter for the TX lane under test.

Table 8: **Add-in Card Transmitter Test Setup and Conditions *(Cont'd)***

Parameter	Value

GTX Transceiver Attributes	• TX Amplitude and Pre-Emphasis:
	  • TX_DRIVE_MODE = PIPE
	  • TXDEEMPH = `1'b1`
	  • TXSWING = `1'b0`
	  • TXMARGIN = `3'b000`
	  • TX_DEEMPH_1 = `5'b10010`
	  • TX_MARGIN_FULL_0 = `7'b1001101`
	• PLL Charge Pump Configuration:
	  • TXPLL_CP_CFG = `8'h05`
	  • RXPLL_CP_CFG = `8'h05`

Reference Clock	100 MHz sourced from the PCI Express CBB.

Test Results for the 2.5 Gb/s Line Rate

Figure 2 is a transition eye diagram, and Figure 3 is a non-transition eye diagram generated from the Agilent PCI Express automated test application. The Add-in Card Transmitter unit interval test reported UI between 400.03 ps and 400.04 ps, and template tests reported zero eye mask failures.

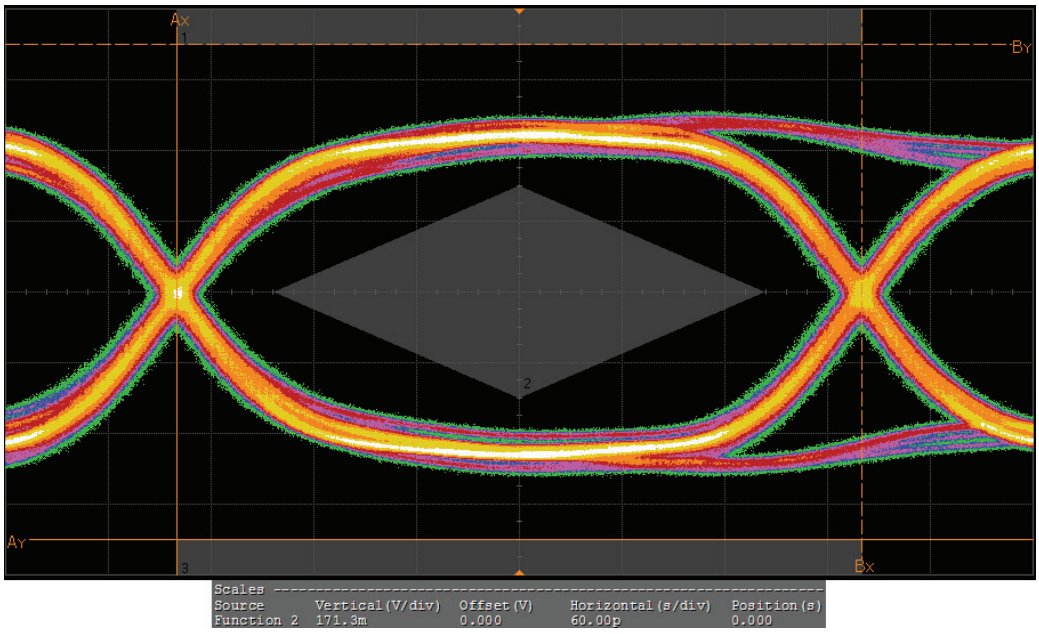

Figure 2: **Transition Eye Diagram for the 2.5 Gb/s Line Rate**

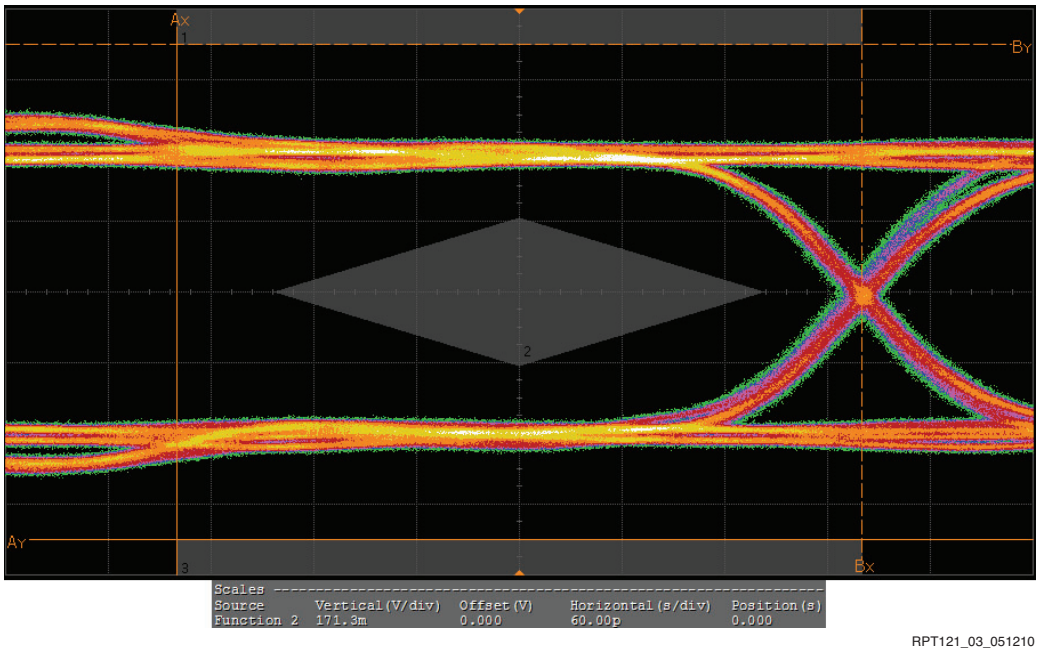

Figure 3: **Non-Transition Eye Diagram for the 2.5 Gb/s Line Rate**

Figure 4 shows the peak differential output voltage results, Figure 5 shows the eye width results, and Figure 6 shows the median to maximum jitter results at a 2.5 Gb/s line rate with a 100 MHz reference clock. These histogram results are skewed towards the worst-case performance because of the transceiver selection process. The vertical axis of the histogram represents the frequency or number of data points. Additional output jitter margin can be gained by using a 125 MHz or 250 MHz reference clock. Table 9 summarizes the maximum and minimum Add-in Card Transmitter test results at the 2.5 Gb/s line rate with a 100 MHz reference clock.

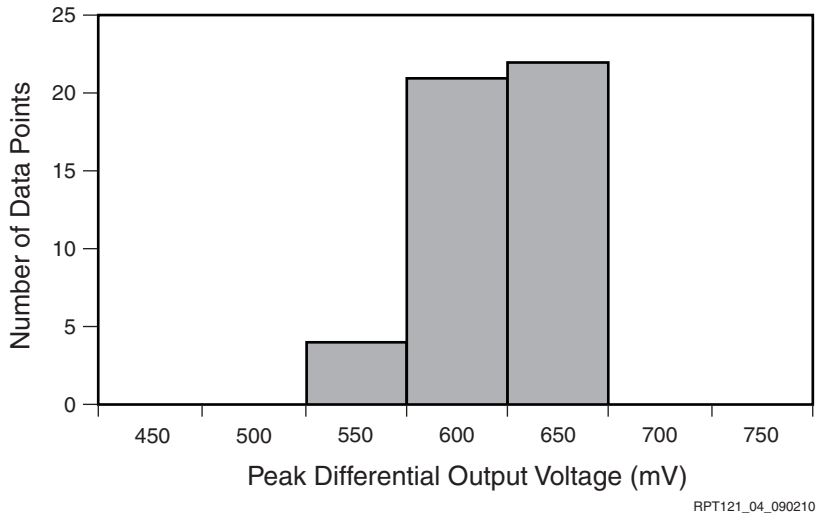

Figure 4: **Peak Differential Output Voltage for the 2.5 Gb/s Line Rate**

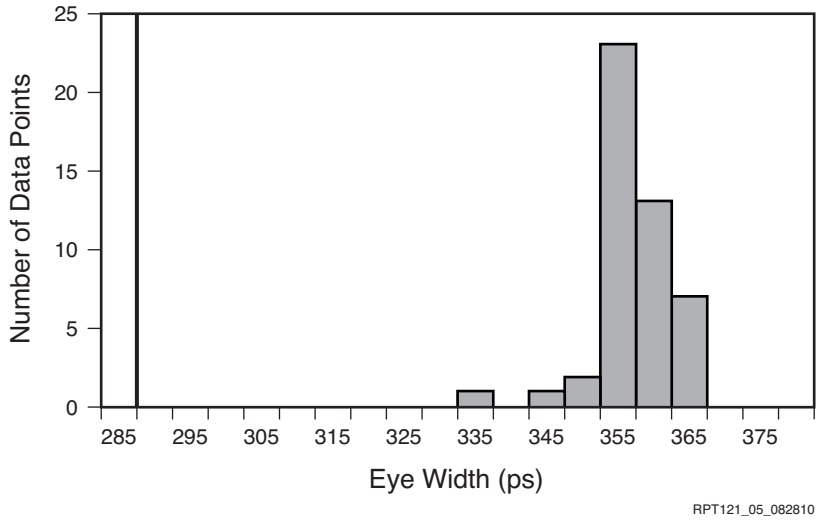

Figure 5: **Eye Width for the 2.5 Gb/s Line Rate**

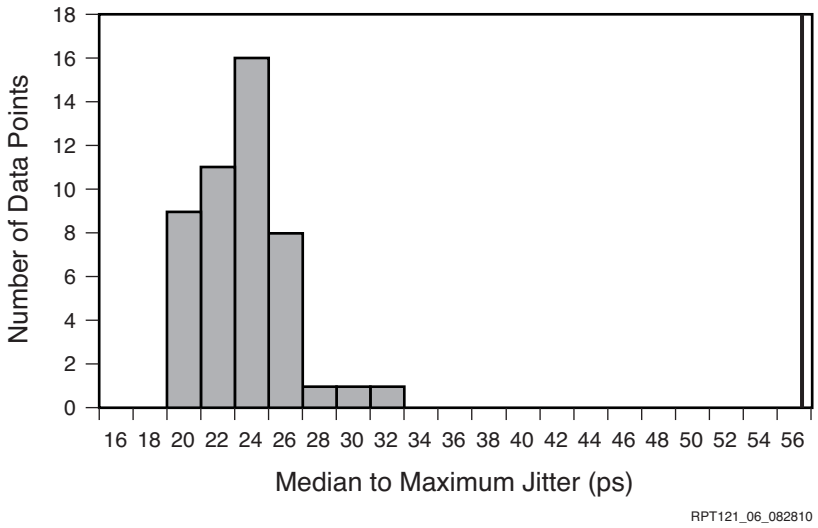

Figure 6: **Median to Maximum Jitter for the 2.5 Gb/s Line Rate**

Table 9: **Minimum and Maximum Test Results for the 2.5 Gb/s Line Rate**

Test Name	Minimum	Maximum	Units
Unit Interval (UI)	400.03	400.04	ps
Template Tests	Zero	Zero	Number of failures
Peak Differential Output Voltage	505.0	646.4	mV
Eye Width	334.60	363.32	ps
Median to Maximum Jitter	18.26	30.08	ps

Notes:

1. In PCI Express mode, the TX_DRIVE_MODE is set to PIPE and the Peak Differential Output Voltage is programmable by setting TXDEEMPH and TXMARGIN.
2. Additional output jitter margin can be gained by using a 125 MHz or 250 MHz reference clock. This is based on using an external ICS874002AG-02 EVB PCI Express Jitter Attenuator with an onboard ICS874003-05 PCI Express Jitter Attenuator that can be used to convert the 100 MHz reference clock from the PCI Express CBB to 125 MHz or 250 MHz. This PCI Express Jitter Attenuator meets the PLL bandwidth and peaking requirements.

SIGTEST Results for the 2.5 Gb/s Line Rate

Figure 7 shows a transition eye diagram, and Figure 8 shows a non-transition eye diagram generated from the SIGTEST application. The SIGTEST results were used only to compare the measurement results from the Agilent PCI Express automated test application. Figure 9 shows the summary of a SIGTEST result.

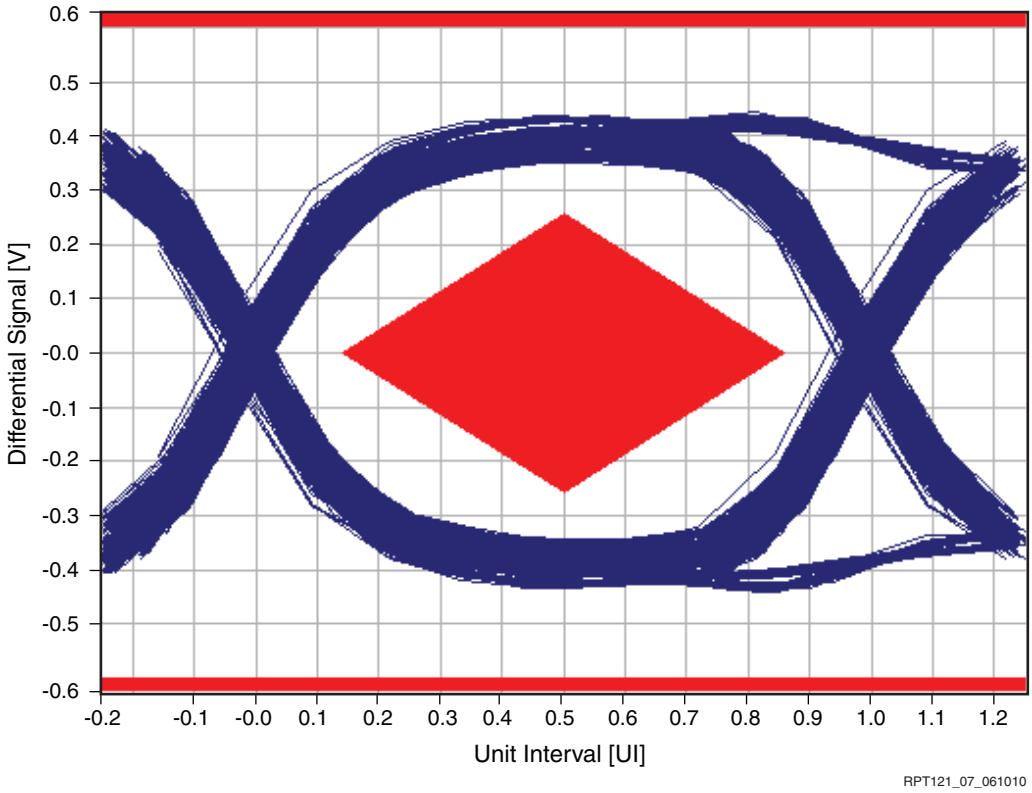

Figure 7: **SIGTEST Transition Eye Diagram for the 2.5 Gb/s Line Rate**

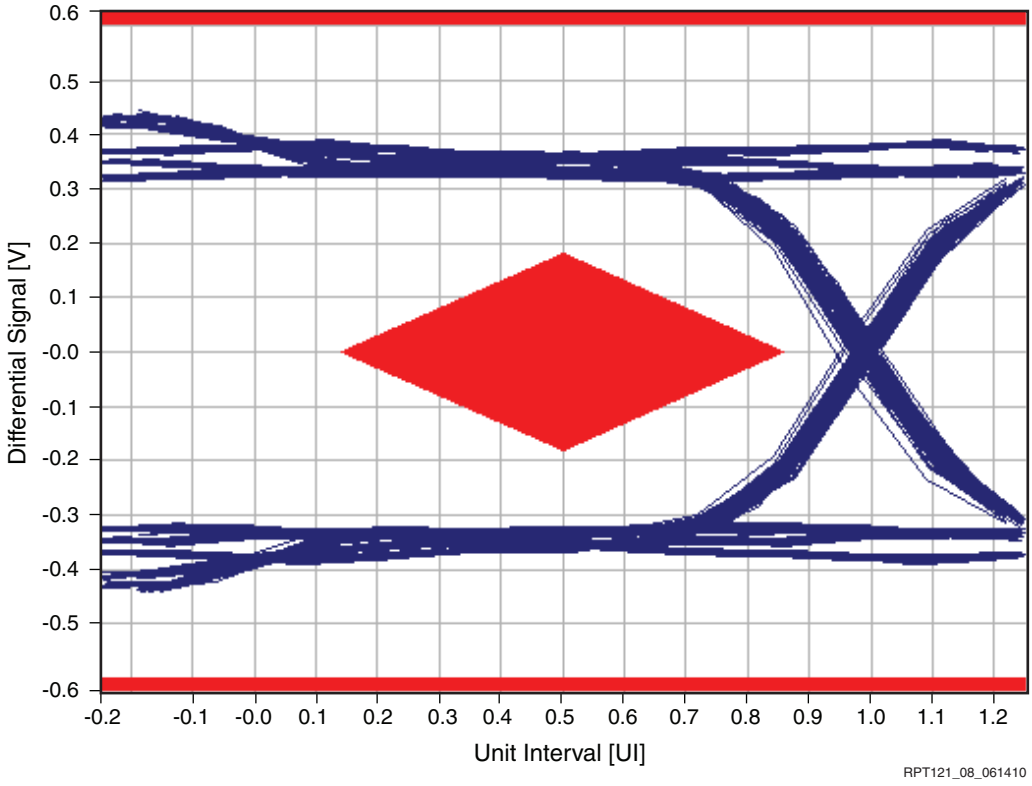

Figure 8: **SIGTEST Non-Transition Eye Signal Diagram for the 2.5 Gb/s Line Rate**

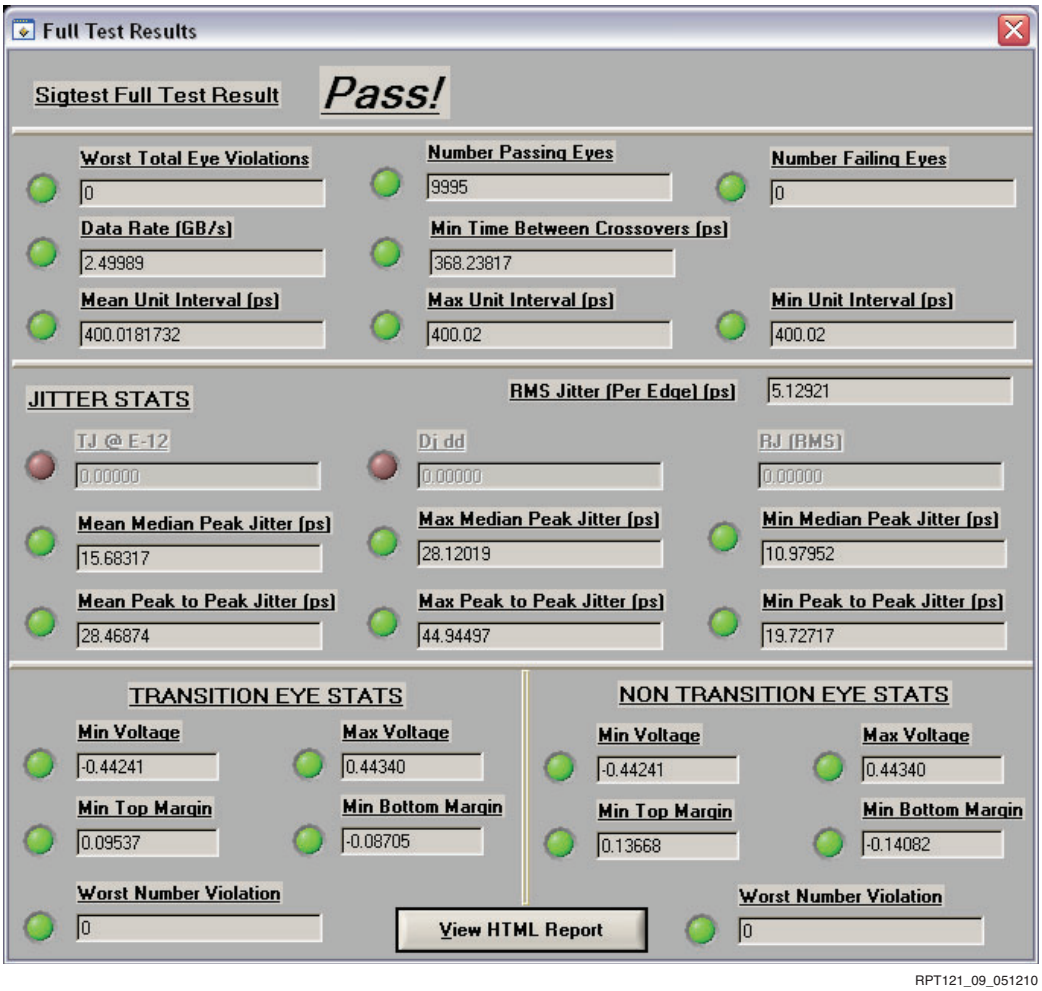

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Figure 9: **SIGTEST Result for the 2.5 Gb/s Line Rate**

Test Results for the 5.0 Gb/s Line Rate

Figure 10 is a transition eye diagram, and Figure 11 is a non-transition eye diagram generated from the Agilent PCI Express automated test application. The Add-in Card Transmitter unit interval test reported UI of 200.01 ps, and template tests reported zero eye mask failures.

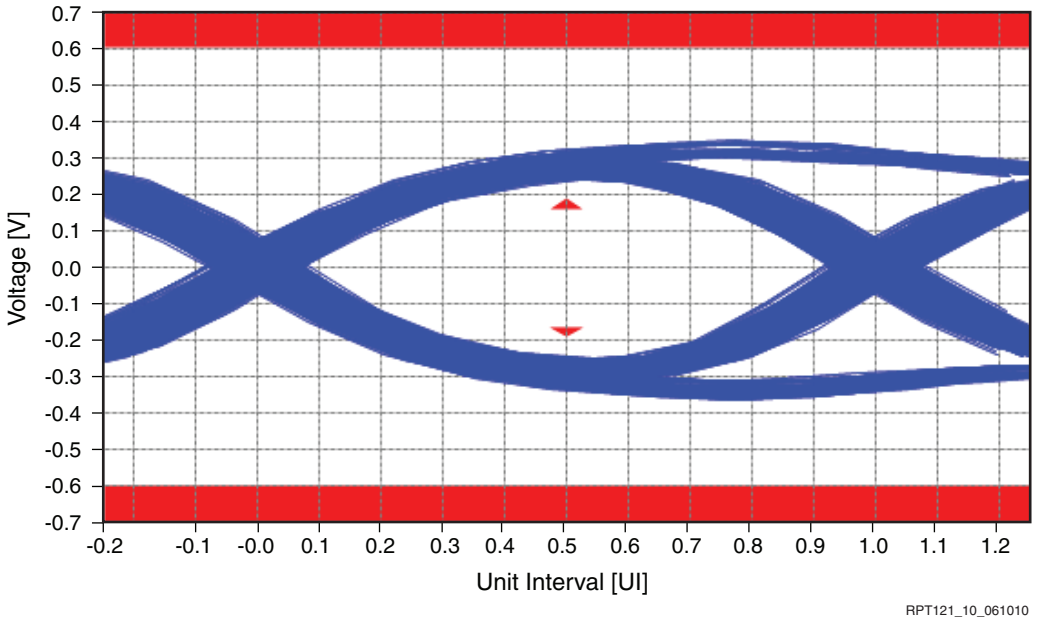


Figure 10: **Transition Eye Diagram for the 5.0 Gb/s Line Rate**

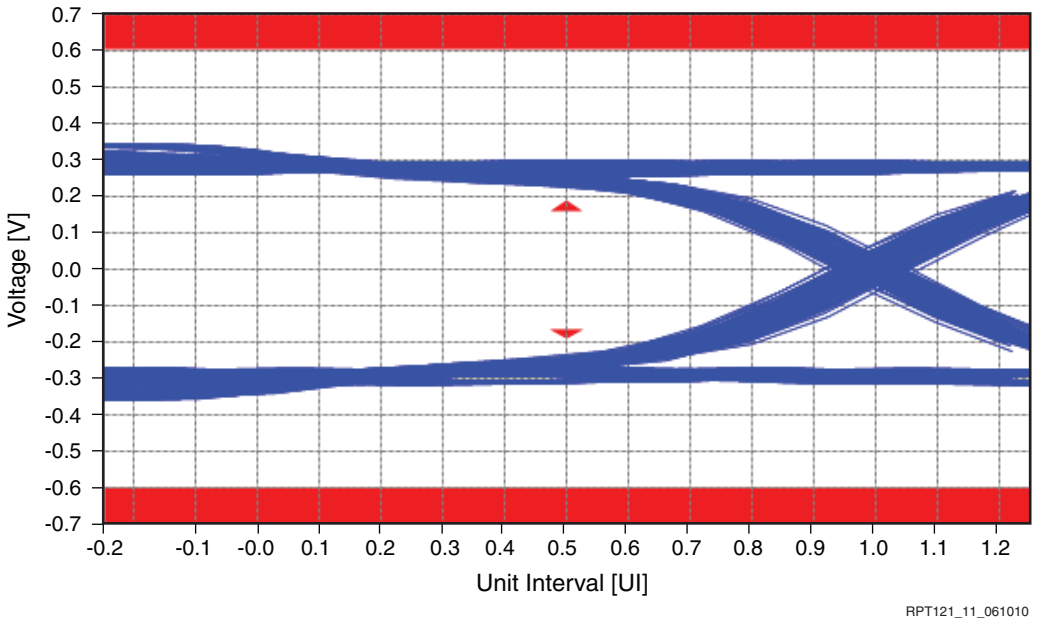


Figure 11: **Non-Transition Eye Diagram for the 5.0 Gb/s Line Rate**

Figure 12 shows the peak differential output voltage results, Figure 13 shows the eye width results, Figure 14 shows the deterministic jitter results, and Figure 15 shows the total jitter results at the 5.0 Gb/s line rate with a 100 MHz reference clock. These histogram results are skewed towards the worst-case performance because of the transceiver selection process. The vertical axis of the histogram represents the frequency or number of data points. Additional output jitter margin can be gained by using a 125 MHz or 250 MHz reference clock. Table 10 summarizes the maximum and minimum Add-in Card Transmitter test results at the 5.0 Gb/s line rate with a 100 MHz reference clock.

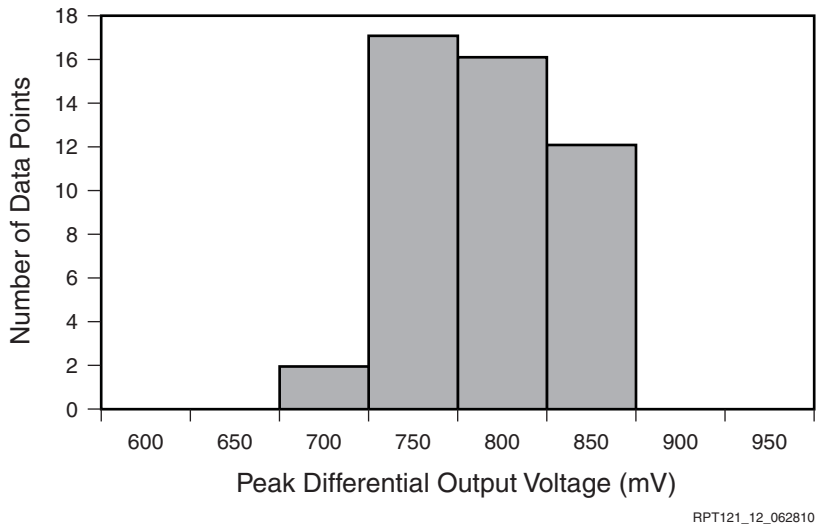


Figure 12: **Peak Differential Output Voltage for the 5.0 Gb/s Line Rate**

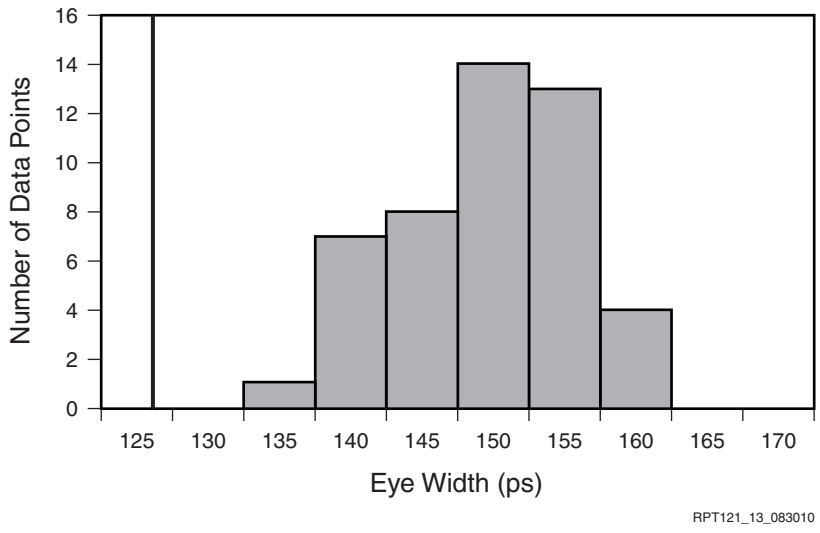


Figure 13: **Eye Width for the 5.0 Gb/s Line Rate**

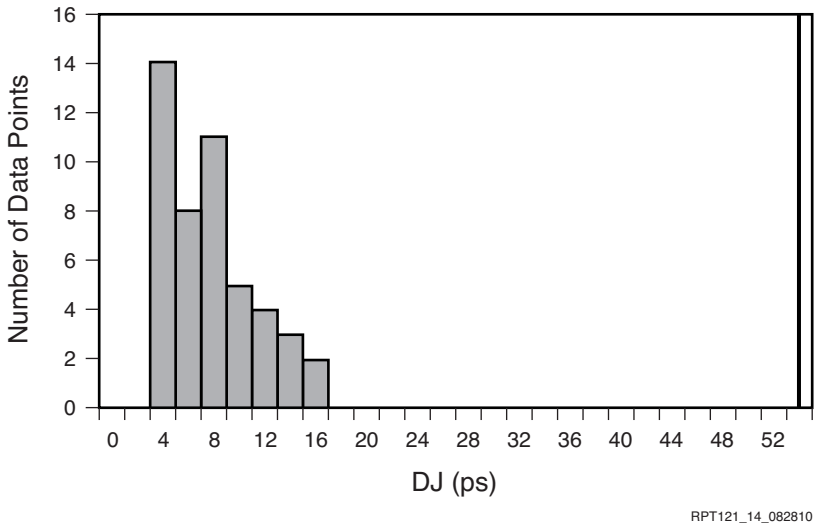


Figure 14: **Deterministic Jitter for the 5.0 Gb/s Line Rate**

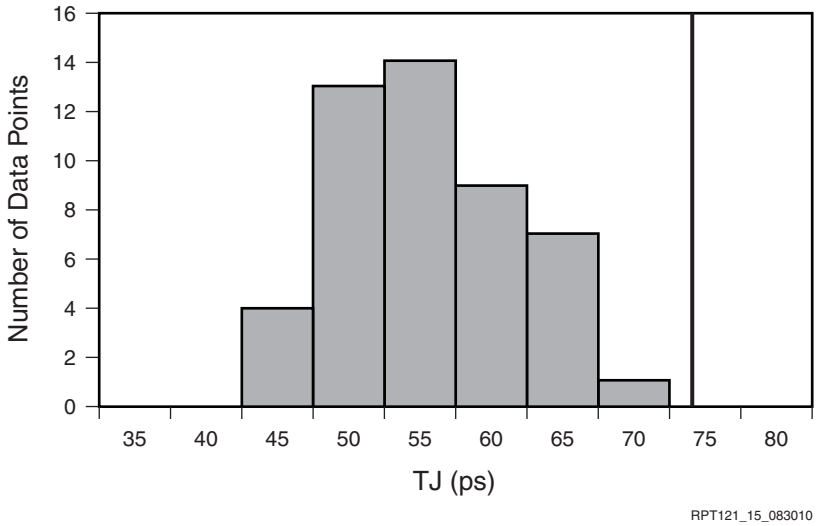


Figure 15: **Total Jitter for the 5.0 Gb/s Line Rate**

Table 10: **Minimum and Maximum Test Results for the 5.0 Gb/s Line Rate**

Test Name	Minimum	Maximum	Units
Unit Interval (UI)	200.01	200.01	ps
Template Tests	Zero	Zero	Number of failures
Peak Differential Output Voltage	671.5	845.9	mV
Eye Width(1)	131.94	157.01	ps
Deterministic Jitter(1)	2.06	15.88	ps

Table 10: **Minimum and Maximum Test Results for the 5.0 Gb/s Line Rate *(Cont'd)***

Test Name	Minimum	Maximum	Units
Total Jitter at BER^{-12} (1)	42.99	68.06	ps

Notes:

1. Without crosstalk.
2. In PCI Express mode, the TX_DRIVE_MODE is set to PIPE and the Peak Differential Output Voltage is programmable by setting TXDEEMPH and TXMARGIN.
3. Additional output jitter margin can be gained by using a 125 MHz or 250 MHz reference clock. This is based on using an external ICS874002AG-02 EVB PCI Express Jitter Attenuator with an onboard ICS874003-05 PCI Express Jitter Attenuator that can be used to convert the 100 MHz reference clock from the PCI Express CBB to 125 MHz or 250 MHz. This PCI Express Jitter Attenuator meets the PLL bandwidth and peaking requirements.

SIGTEST Results for the 5.0 Gb/s Line Rate

Figure 16 shows a transition eye diagram, and Figure 17 shows a non-transition eye diagram generated from the SIGTEST application. The SIGTEST results were used only to compare the measurement results from the Agilent PCI Express automated test application. Figure 18 shows the summary of a SIGTEST result.

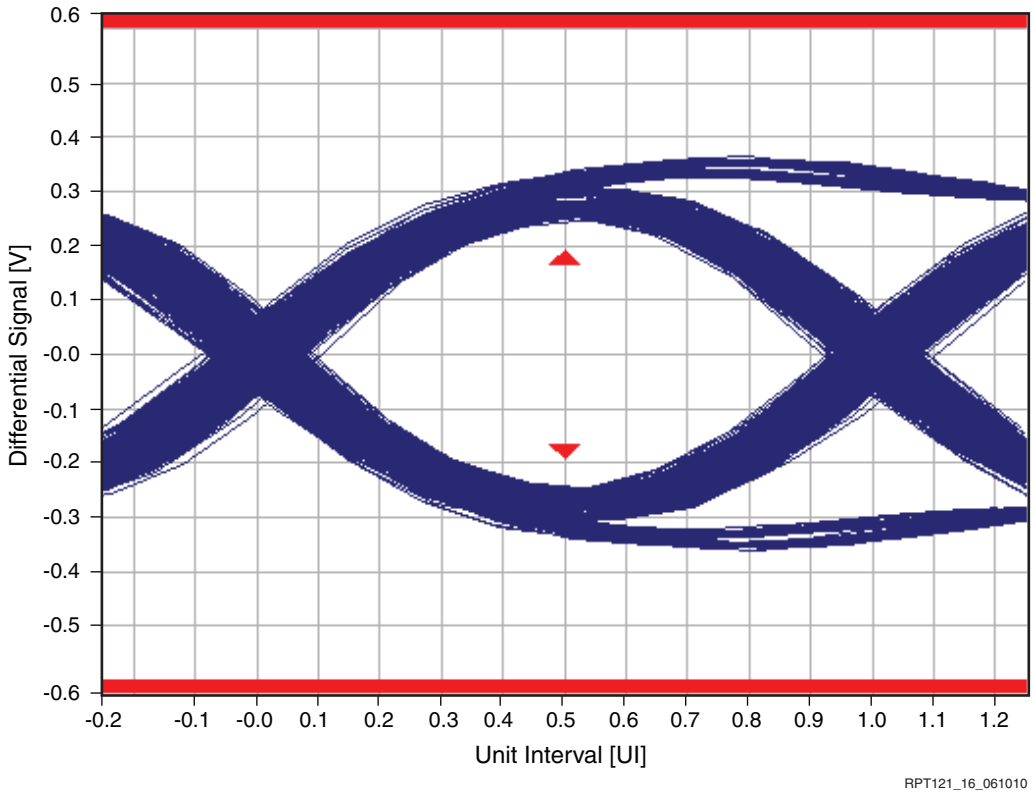


Figure 16: **SIGTEST Transition Eye Diagram for the 5.0 Gb/s Line Rate**

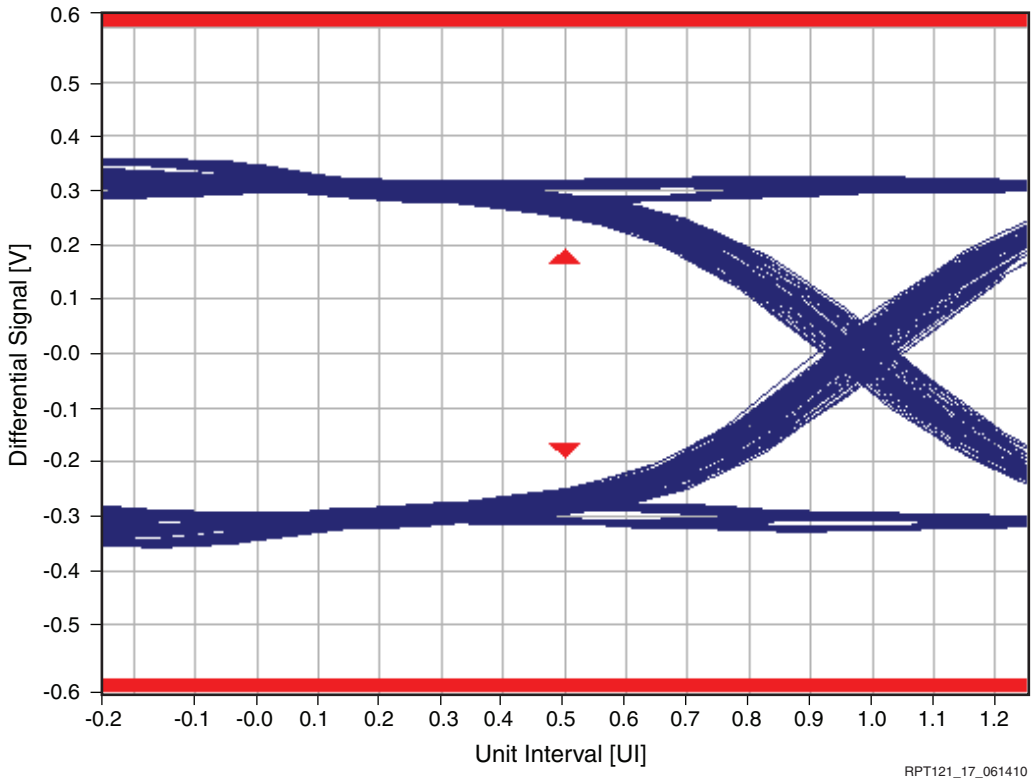


Figure 17: **SIGTEST Non-Transition Eye Signal Diagram for the 5.0 Gb/s Line Rate**

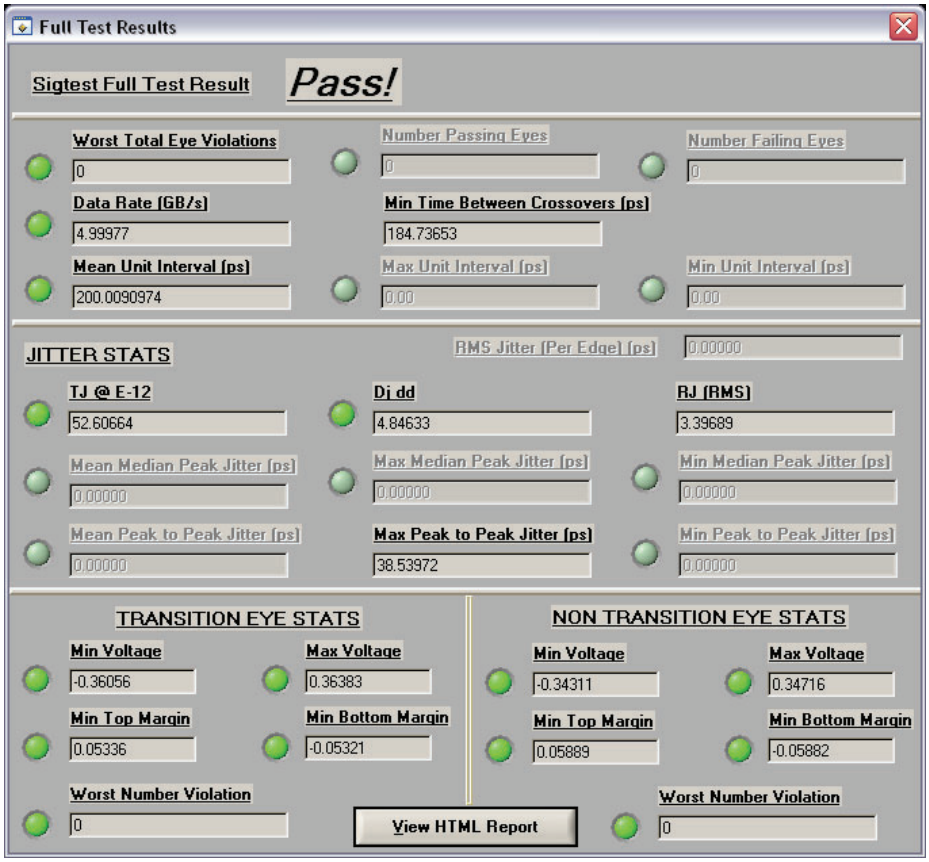


Figure 18: **SIGTEST Result for the 5.0 Gb/s Line Rate**

Transmitter Differential and Common Mode Return Loss

Test Methodology

The *PCI Express Base Specification, Revision 2.1* defines the transmitter differential and common mode return loss as described in Table 11. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

Table 11: **Transmitter Differential and Common Mode Return Loss Specification**

Parameter	Specification Range	Frequency Range	Units
TX Differential Return Loss	10 (minimum)	From 50 MHz to 1.25 GHz	dB
	8 (minimum)	From 1.25 GHz to 2.50 GHz	dB
TX Common Mode Return Loss	6 (minimum)	From 50 MHz to 2.50 GHz	dB

The Agilent 8720ES Vector Network Analyzer (VNA) test equipment used for measuring the transmitter differential and common mode return loss interfaces to a host PC through a GPIB interface. Calibration begins after the measurement parameters are set. These VNA measurements are independent of voltage and are accurate up to 11 GHz. A digital multimeter confirms that the differential resistance is 100Ω before the measurement. Table 12 defines the test setup and conditions. Figure 19 shows the return loss measurement setup.

Table 12: **Transmitter Differential and Common Mode Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 8720ES Vector Network Analyzer
TX Coupling / Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical Voltage
Temperature	Room Temperature
Load Boards	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C
FPGA	Virtex-6 FPGA XC6VLX240T FF1156
Reference Clock	Not necessary for this test
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

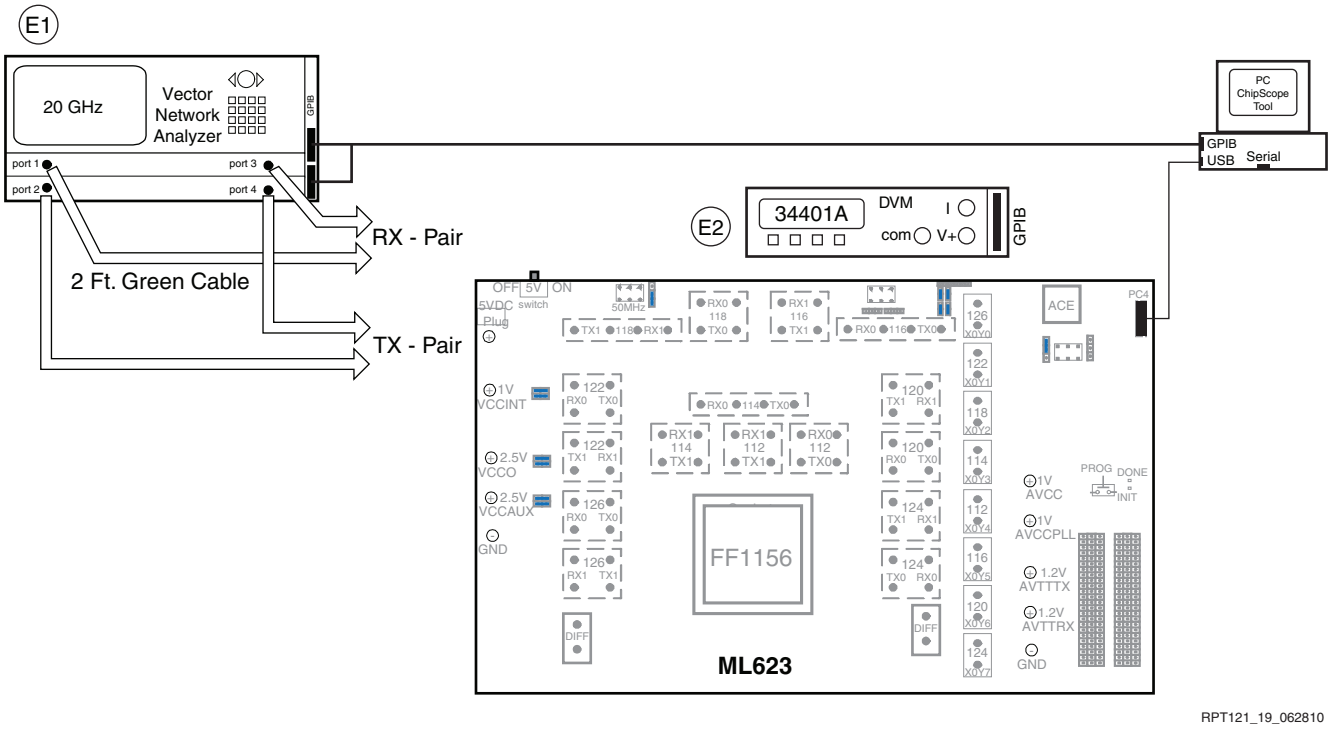


Figure 19: **Transmitter Return Loss Test Setup Block Diagram**

Test Results for Transmitter Return Loss

Figure 20 describes the transmitter differential return loss measurement, and Figure 21 describes the transmitter common mode output return loss measurement. The return loss results are recorded in negative dB.

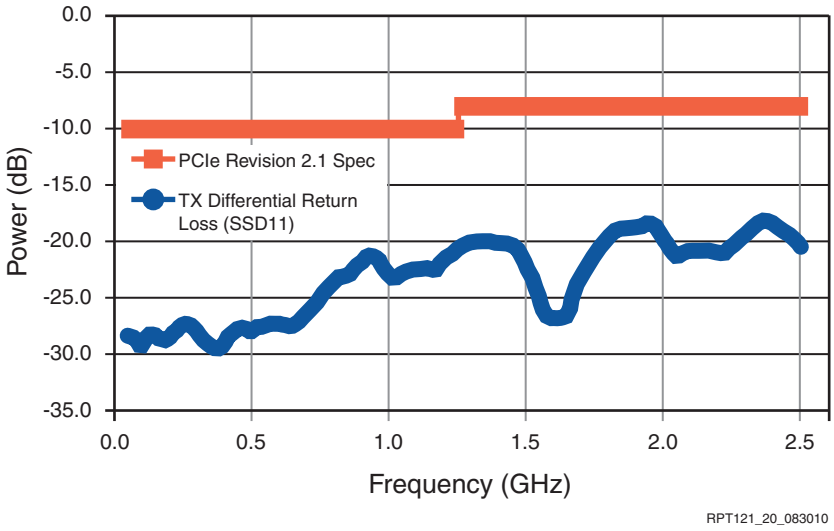


Figure 20: **Transmitter Differential Return Loss Measurement**

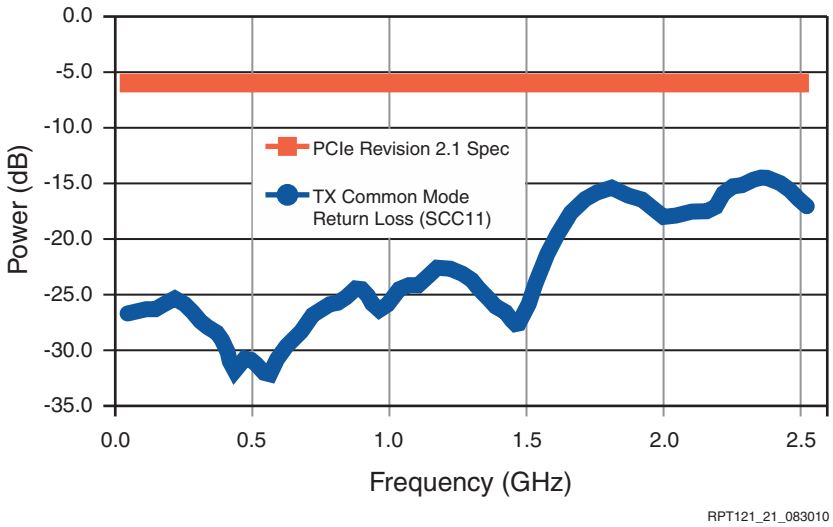


Figure 21: **Transmitter Common Mode Return Loss Measurement**

PLL Bandwidth Test

Test Methodology

The PLL Bandwidth test consists of PLL bandwidth and peaking measurements. The *PCI Express Base Specification, Revision 2.1* defines the transmitter PLL bandwidth and peaking as described in Table 13 (for the 2.5 Gb/s line rate) and Table 14 (for the 5.0 Gb/s line rate).

Table 13: **PLL Bandwidth Specification for the 2.5 Gb/s Line Rate**

Parameter	Specification Range	Units
PLL Bandwidth	From 1.5 to 22	MHz
PLL Peaking	3 (maximum)	dB

Table 14: **PLL Bandwidth Specification for the 5.0 Gb/s Line Rate**

Parameter	Specification Range A	Specification Range B	Units
PLL Bandwidth	From 5 to 16	From 8 to 16	MHz
PLL Peaking	1 (maximum)	3 (maximum)	dB

Notes:

1. Two combinations of PLL bandwidth and peaking are specified for the 5.0 Gb/s line rate to make a trade-off between the two parameters. If the PLL's minimum bandwidth is ≥ 8 MHz, then up to 3.0 dB of peaking is permitted (Specification Range A). If the PLL's minimum bandwidth is relaxed to ≥ 5 MHz, then a peaking value of up to 1.0 dB must be met (Specification Range B).
2. All transceivers characterized in this report fall within Specification Range A.

This test is performed using the test setup shown in Figure 22. An Agilent J-BERT N4903B Bit Error Rate Tester is used as the clock source, and an Agilent DCA-J 86100C Digital Communication Analyzer with an 86108A Precision Waveform Analyzer is used to perform the PLL Bandwidth test. The Jitter Spectrum Phase Noise (JSPN) application running on an external host PC is used to control the measurement equipment via a GPIB

interface. Hardware calibration was completed with the PCIe compliance pattern prior to data collection. The calibration and test procedure methodologies are documented in *PCI Express PLL Loop Bandwidth Test Methodology Users Guide*, *Agilent DCAj 86100C, 86108A Precision Waveform Analyzer*, or *83496B Clock Recovery Module*, and *J-BERT N4903A Bit Error Rate Tester*.

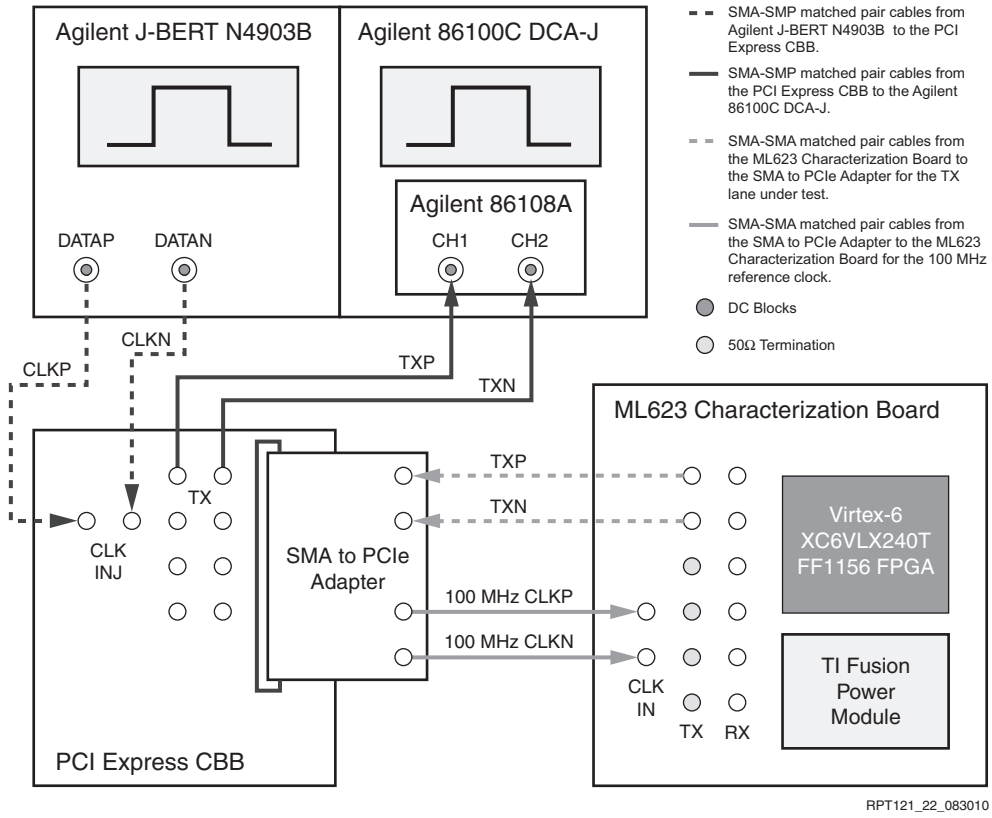


Figure 22: **PLL Bandwidth Test Setup Block Diagram**

The Virtex-6 device under test is configured to transmit the PCI Express compliance pattern on the TX differential lanes on the ML623 board. This device is configured to the default PCI Express mode with the settings described in Table 15. The test setup and conditions for the PLL Bandwidth test are also defined in Table 15.

Table 15: **PLL Bandwidth Test Setup and Conditions**

Parameter	Value
Measurement Instrument	• Agilent J-BERT N4903B. • Agilent DCA-J 86100C Digital Communication Analyzer with 86108A Precision Waveform Analyzer: • AC coupled using DC blocks.
Software Application	JSPN application: • Running on an external host PC to control the measurement instrument via GPIB. • PCI-SIG accepted methodology.
Voltage	TI Fusion Power Module: • Installed on the ML623 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and V_{MAX}.

Table 15: **PLL Bandwidth Test Setup and Conditions *(Cont'd)***

Parameter	Value
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, and T_{100}.
Data Pattern	Transmitting the PCI Express compliance pattern on the TX lanes of the ML623 board.
FPGA	Virtex-6 FPGA XC6VLX240T FF1156.

Load Boards	• ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C:
	  • 50Ω terminator on TX channels not under test.
	  • On the various ML623 board channels used, there are about 4 to 8 inches of FR4 in the TX paths.
	• PCI Express Compliance Base Board (CBB), Revision 2.0:
	  • Standard PCI-SIG board for the Add-in Card Transmitter test.
	• SMA to PCIe Adapter, Revision D:
	  • Used to connect the ML623 board to the x16 interface of the PCI Express CBB.

Cables	• One pair of matched 50Ω Rosenberger SMA-SMP cables from the PCI Express CBB to the Agilent DCA-J 86100C. • One pair of matched 50Ω Rosenberger SMA-SMP cables from the Agilent J-BERT N4903B to the PCI Express CBB. • One pair of matched 50Ω SMA-SMA cables from the SMA to PCIe Adapter to the ML623 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the ML623 board to the SMA to PCIe Adapter for the TX lane under test.
GTX Transceiver Attributes	TX Amplitude and Pre-Emphasis: • TX_DRIVE_MODE = PIPE • TXDEEMPH = `1'b1` • TXSWING = `1'b0` • TXMARGIN = `3'b000` • TX_DEEMPH_1 = `5'b10010` • TX_MARGIN_FULL_0 = `7'b1001101` PLL Charge Pump Configuration: • TXPLL_CP_CFG = `8'h05` • RXPLL_CP_CFG = `8'h05`
Reference Clock	100 MHz sourced from the Agilent J-BERT N4903B.

Test Results for the 2.5 Gb/s Line Rate

Figure 23 shows the histogram for the PLL bandwidth, and Figure 24 shows the histogram for PLL peaking. All results are measured across process, voltage, and temperature. Figure 25 shows an example of the jitter transfer function of a PLL bandwidth test. Table 16 summarizes the maximum and minimum test result values.

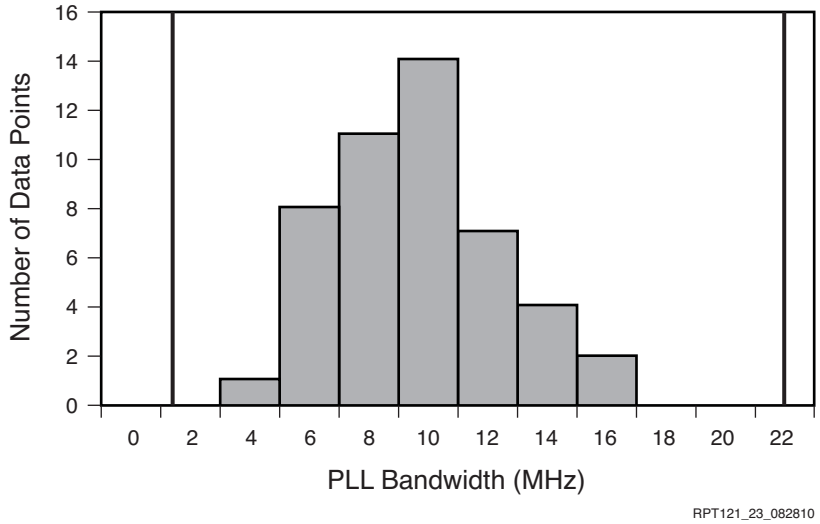


Figure 23: **PLL Bandwidth for the 2.5 Gb/s Line Rate**

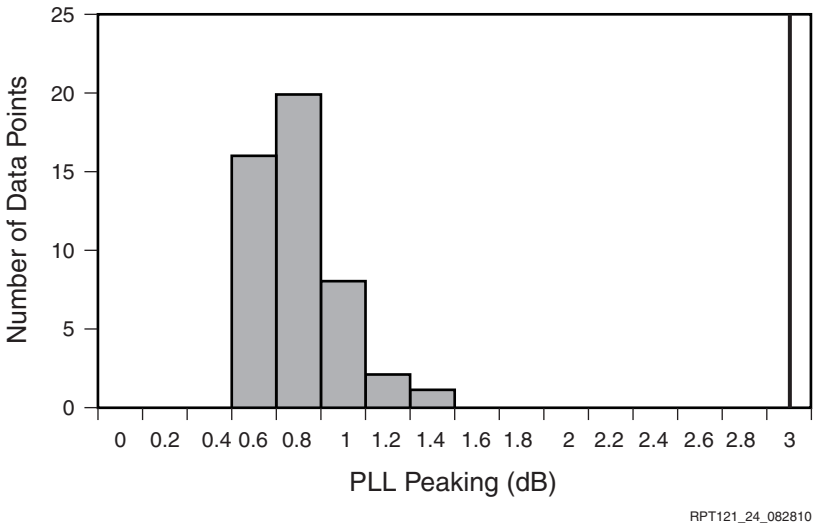


Figure 24: **PLL Peaking for the 2.5 Gb/s Line Rate**

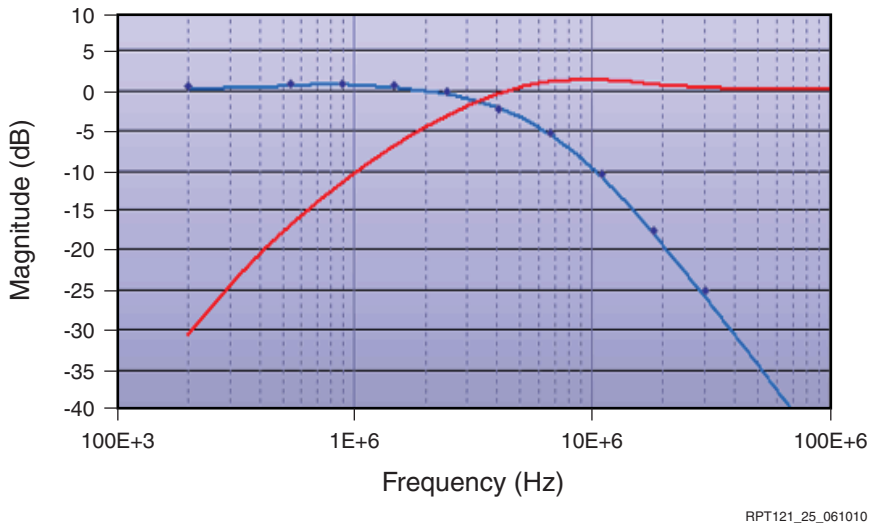


Figure 25: **Jitter Transfer Function for the 2.5 Gb/s Line Rate**

Table 16: **Minimum and Maximum Test Results for the 2.5 Gb/s Line Rate**

Test Name	Minimum	Maximum	Units
PLL Bandwidth	4.00	15.00	MHz
PLL Peaking	0.46	1.32	dB

Notes:

1. Hardware calibration with PCIe compliance pattern is performed prior to data collection.
2. These results are confirmed with a BERTScope CRJ 125A-PCIE using the PCI-SIG accepted test procedure documented in *PCI Express (Rev2.0) Test Methodology for PLL Loop Bandwidth Response in Add-in cards*.

Test Results for the 5.0 Gb/s Line Rate

Figure 26 shows the histogram for the PLL bandwidth, and Figure 27 shows the histogram for PLL peaking. All results are measured across process, voltage, and temperature. Figure 28 shows an example of the jitter transfer function of a PLL bandwidth test. Table 17 summarizes the maximum and minimum test result values.

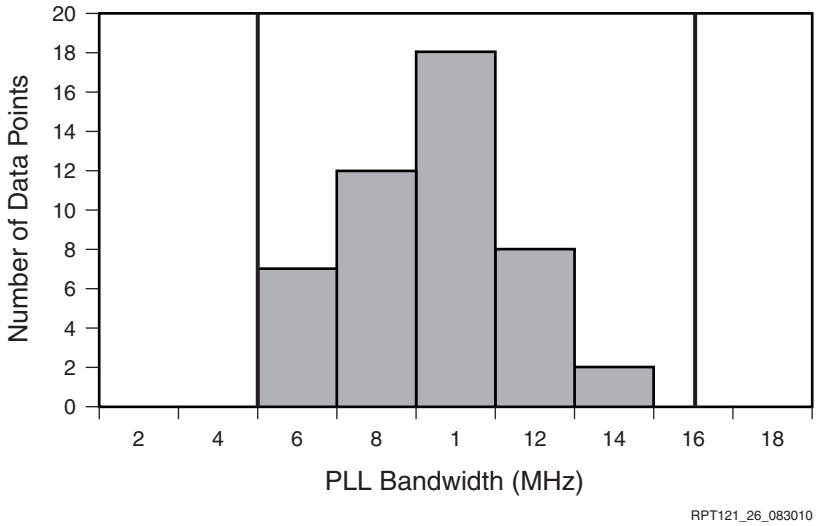


Figure 26: **PLL Bandwidth for the 5.0 Gb/s Line Rate**

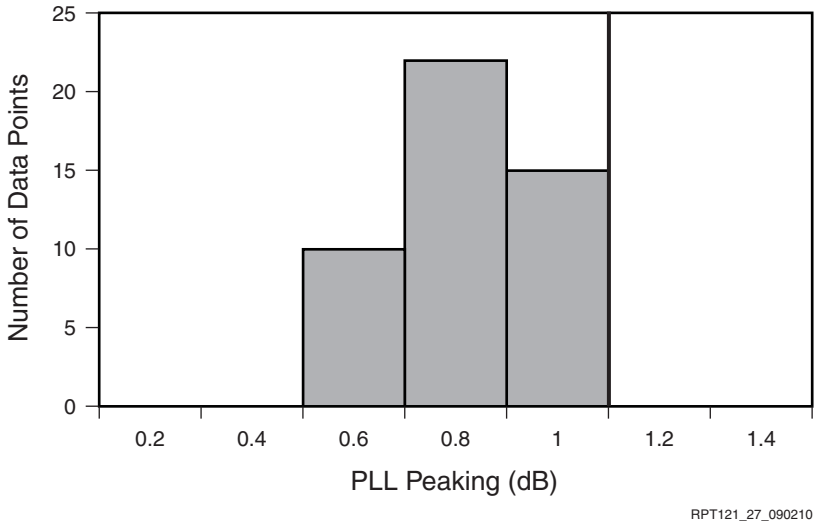


Figure 27: **PLL Peaking for the 5.0 Gb/s Line Rate**

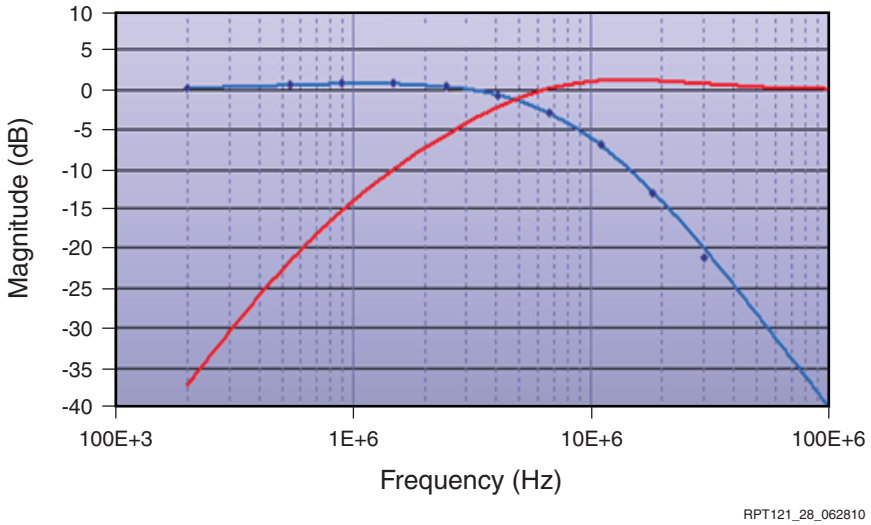


Figure 28: **Jitter Transfer Function for the 5.0 Gb/s Line Rate**

Table 17: **Minimum and Maximum Test Results for the 5.0 Gb/s Line Rate**

Test Name	Minimum	Maximum	Units
PLL Bandwidth	5.48	14.00	MHz
PLL Peaking	0.50	0.96	dB

Notes:

1. Hardware calibration with PCIe compliance pattern is performed prior to data collection.
2. These results are confirmed with a BERTScope CRJ 125A-PCIE using the PCI-SIG accepted test procedure documented in *PCI Express (Rev2.0) Test Methodology for PLL Loop Bandwidth Response in Add-in cards*.

Receiver Input Jitter Tolerance Test

Test Methodology

The receiver input jitter tolerance as defined by the *PCI Express Base Specification, Revision 2.1* is measured using the test setup shown in Figure 29. The BERTScope BSA125B-PCIE generates a CJTPAT pattern with various components of jitter injected and signal characteristics, as described in Table 18. This table is based on the table labeled "5.0 GT/s Tolerancing Limits for Common Refclk Rx Architecture" in the *PCI Express Base Specification, Revision 2.1*. Part of the deterministic jitter (DJ), in the form of ISI, is added using 42.42 inches of FR4 through the BERTScope Inter Symbol Interference (ISI) test board.

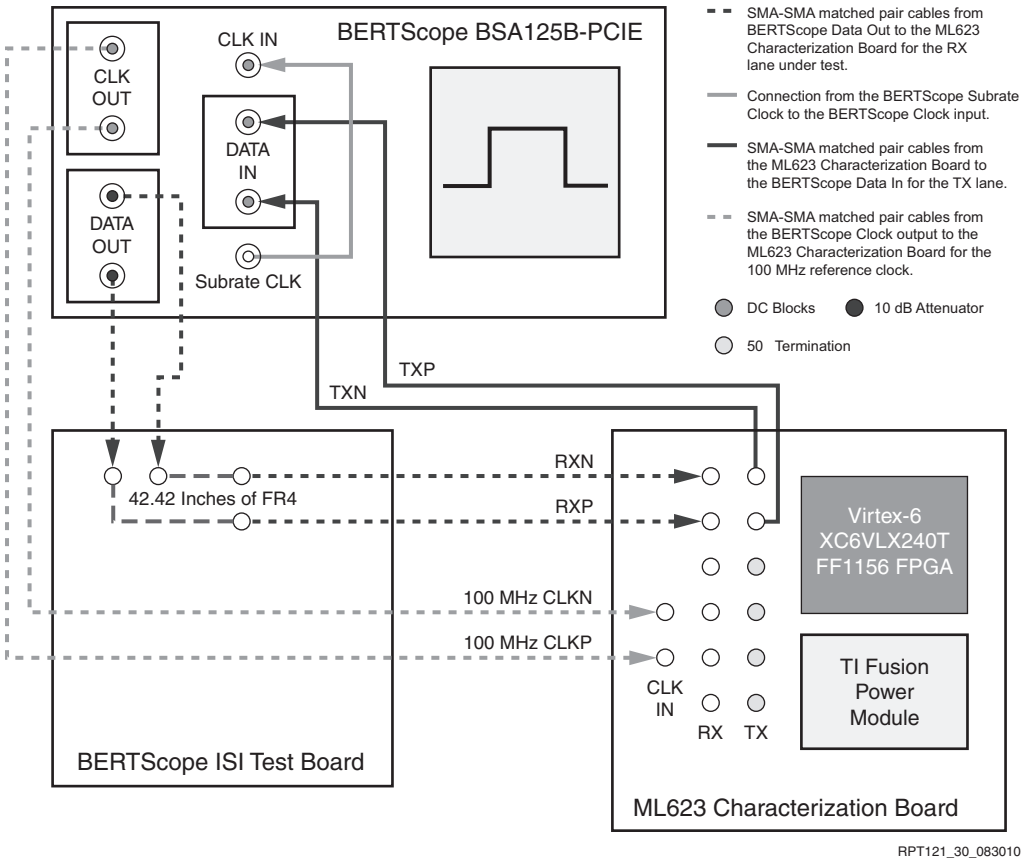


Figure 29: **Receiver Input Jitter Tolerance Test Setup Block Diagram**

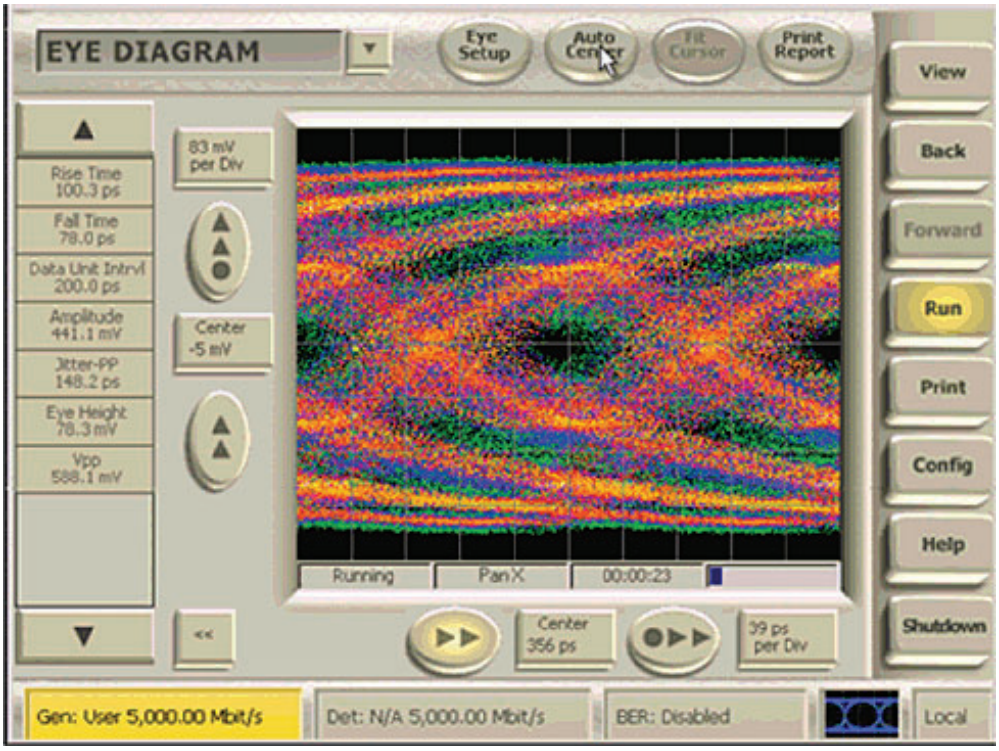
Table 18: **Tolerancing Limits for Common Refclk RX Architecture Specification for the 5.0 Gb/s Line Rate**

Parameter	Specification Limit	Units
1.5 to 100 MHz RMS jitter (High Frequency RJ)	3.4	ps RMS
< 1.5 MHz RMS jitter (Low Frequency RJ)	4.2	ps RMS
Maximum DJ impinging on RX under test (High Frequency DJ)	88	ps
33 kHz REFCLK residual (Low Frequency DJ)	75	ps
Minimum single pulse applied at RX(1)	120	ps
Minimum/Maximum pulse voltage ratio(2)	5	
Receive eye voltage opening	120	mV_{PP} diff
Common mode noise from RX	300	mV_{PP}

Notes:

1. Calibrated by tuning data output amplitude in BERTScope.
2. V_{PP}/Eye Height ratio measured using BERTScope and achieved using 42.42 inches of FR4 through the BERTScope ISI test board.

After all of the jitter components listed in Table 18 are added, the resulting eye diagram on the BERTScope is as shown in Figure 30. Sinusoidal jitter (SJ) is swept from 1 kHz to 80 MHz.



RPT121_29_062910

Figure 30: **Eye Diagram with Jitter Injected for the 5.0 Gb/s Line Rate**

The Virtex-6 FPGA GTX transceiver under test recovers the input data and transmits the pattern back to the Data In (Error Detector) of the BERTScope, where bit errors are measured. This is a synchronous test setup with no PPM offset between the BERTScope data generator and the reference clock provided to the Virtex-6 FPGA GTX transceiver under test. Calibration and test are performed based on the methodology described in BERTScopes's *PCI Express 5.0 GT/s Add-in Card Receiver Testing* documentation. The PCIe Compliance Base Board (CBB) for the add-in card is not used in this setup. The CJTPAT pattern is used because it is a more strenuous test pattern compared to the PCIe compliance test pattern.

Table 19 defines the test setup and conditions for the Receiver Input Jitter Tolerance test.

Table 19: **Receiver Input Jitter Tolerance Test Setup and Conditions**

Parameter	Value
Measurement Instrument	BERTScope BSA125B-PCIE: • AC coupled using DC blocks.
Voltage	TI Fusion Power Module: • Installed on the ML623 board to change the MGTAVTT and MGTAVCC voltages between V_{MIN} and V_{MAX}.
Temperature	Temperature Unit: • A socket attached with a temperature controller is used to change the temperature condition of the device under test between T_{-40}, T_0, and T_{100}.
Data Pattern	CJTPAT.

Table 19: **Receiver Input Jitter Tolerance Test Setup and Conditions *(Cont'd)***

Parameter	Value
FPGA	Virtex-6 FPGA XC6VLX240T FF1156.
Injected Jitter	See Table 18.
BER	10^{-12} (measured at 10^{-9}, extrapolated to 10^{-12}).

Load Boards	• ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C:
	  • 50Ω terminator on TX channels not under test.
	  • On the various ML623 board channels used, there are about 4 to 10 inches of FR4 in the RX paths.
	• BERTScope ISI Test Board:
	  • With a pair of 10 dB attenuators.
	  • Used to add 42.42 inches of FR4 on the receive path.

Cables	• One pair of matched 50Ω SMA-SMA cables BERTScope to the ML623 board for the 100 MHz reference clock. • One pair of matched 50Ω SMA-SMA cables from the BERTScope to the ML623 board for the RX lane under test. • One pair of matched 50Ω SMA-SMA cables from the ML623 board to the BERTScope for the forwarded data on the TX lane. • SMA-SMA connection from the BERTScope Subrate Clock to the BERTScope Clock input for the 100 MHz clock.

GTX Transceiver Attributes	• PLL Charge Pump Configuration:
	  • TXPLL_CP_CFG = `8'h05`
	  • RXPLL_CP_CFG = `8'h05`
	• RX Equalizer:
	  • RXEQMIX = `10'b0000000110`
	• RX CDR:
	  • PMA_RX_CFG = `25'h05CE008`
	• DFE:
	  • DFETAP1 = `5'b00000`
	  • DFETAP2 = `5'b00000`
	  • DFETAP3 = `4'b0000`
	  • DFETAP4 = `4'b0000`
	• RX Termination:
	  • AC_CAP_DIS = FALSE
	  • RCV_TERM_GND = TRUE
	  • RCV_TERM_VTTRX = FALSE

Reference Clock	100 MHz sourced from the BERTScope.

Test Results for the 5.0 Gb/s Line Rate

Figure 31 shows the receiver jitter tolerance SJ sweep. Figure 32 shows the minimum receiver sinusoidal jitter tolerance histogram at 22.82 MHz. SJ is applied for each test performed in addition to all the jitter components and amplitude settings defined in Table 18. Table 20 shows the minimum SJ tolerance at 22.82 MHz for the transceivers characterized.

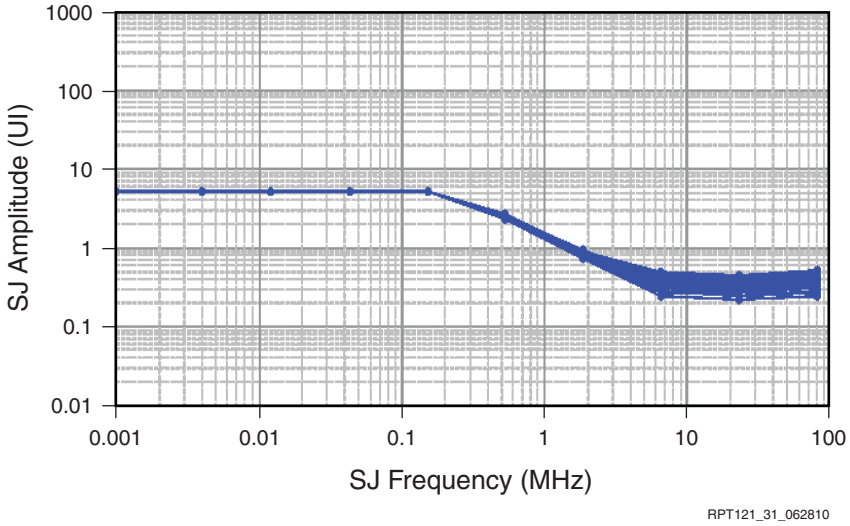


Figure 31: **Receiver Input Jitter Tolerance SJ Sweep for the 5.0 Gb/s Line Rate (CJTPAT, BER = 10^{-12})**

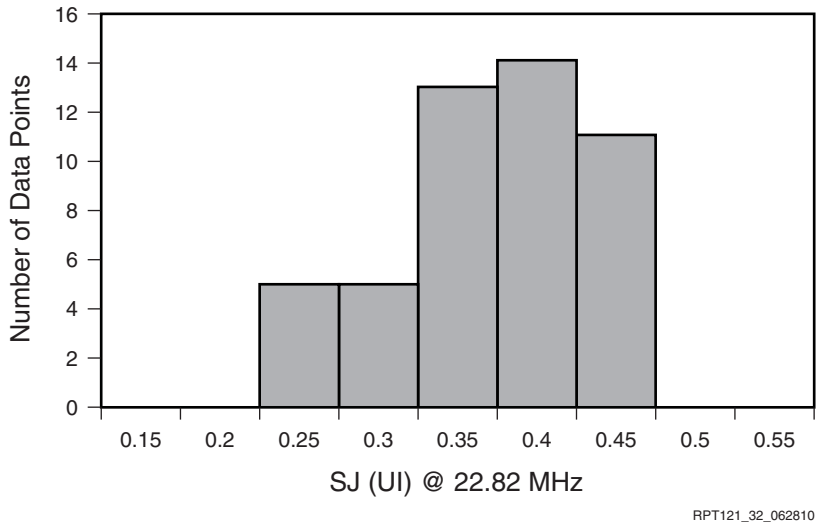


Figure 32: **Receiver Sinusoidal Jitter Tolerance at 22.8 MHz Test Results (CJTPAT, BER = 10^{-12})**

Table 20: **Receiver Input Jitter Tolerance Test Results for the 5.0 Gb/s Line Rate**

Parameter	Test Condition	BER	Minimum SJ Tolerance	Units
Receiver Jitter Tolerance	SJ at 22.8 MHz	10^{-12}	0.22	UI

Receiver Differential and Common Mode Return Loss

Test Methodology

The *PCI Express Base Specification, Revision 2.1* defines the receiver differential and common mode return loss as described in Table 21. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

Table 21: **Receiver Differential and Common Mode Return Loss Specification**

Parameter	Specification Range	Frequency Range	Units
RX Differential Return Loss	10 (minimum)	From 50 MHz to 1.25 GHz	dB
	8 (minimum)	From 1.25 GHz to 2.50 GHz	dB
RX Common Mode Return Loss	6 (minimum)	From 50 MHz to 2.50 GHz	dB

The Agilent 8720ES VNA test equipment used for measuring the receiver differential and common mode return loss interfaces to a host PC through a GPIB interface. Calibration begins after the measurement parameters are set. These VNA measurements are independent of voltage and are accurate up to 11 GHz. A digital multimeter confirms that the differential resistance is 100Ω before the measurement. Table 22 defines the test setup and conditions. Figure 33 shows the return loss measurement setup.

Table 22: **Receiver Differential and Common Mode Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 8720ES Vector Network Analyzer
RX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical Voltage
Temperature	Room Temperature
Load Boards	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C
FPGA	Virtex-6 FPGA XC6VLX240T FF1156
Reference Clock	Not necessary for this test
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency	100 Hz

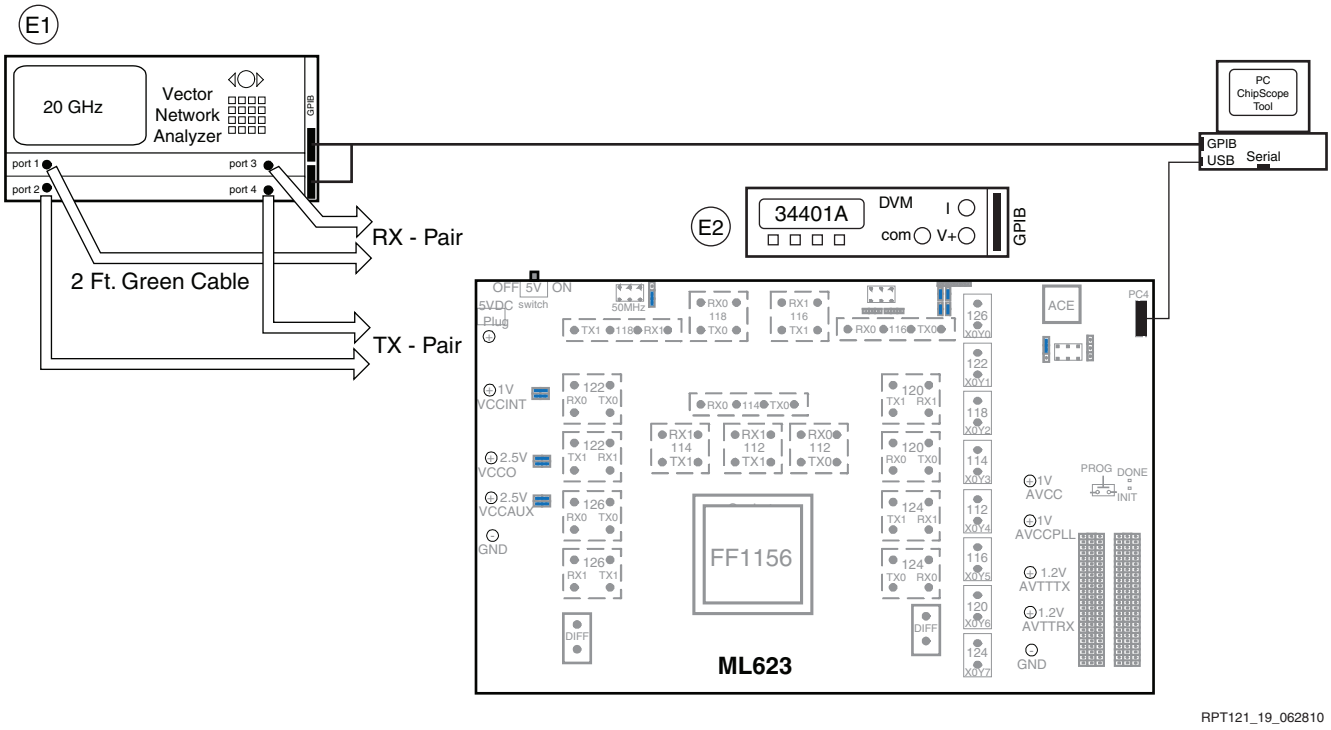


Figure 33: **Receiver Return Loss Test Setup Block Diagram**

Test Results for Receiver Return Loss

Figure 34 describes the receiver differential return loss measurement, and Figure 35 describes the receiver common mode output return loss measurement. The return loss results are recorded in negative dB.

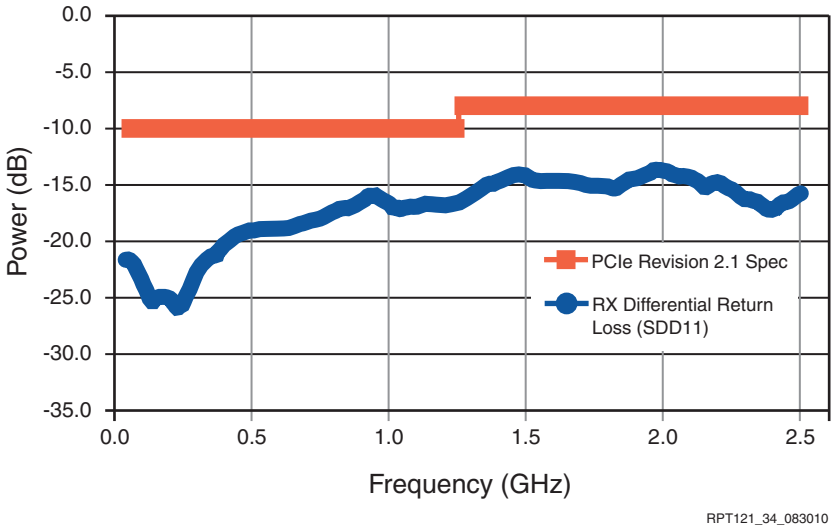


Figure 34: **Receiver Differential Return Loss Measurement**

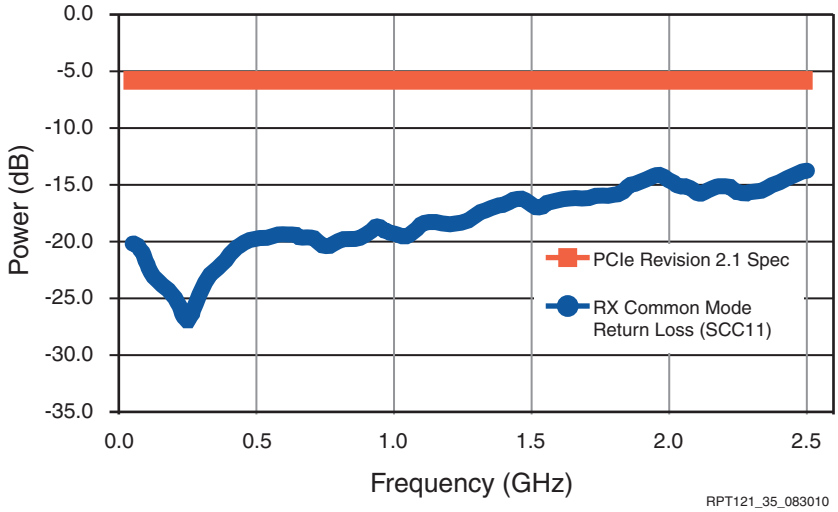


Figure 35: **Receiver Common Mode Return Loss Measurement**