Spartan-3A DSP Starter Board

Avnet Engineering Services

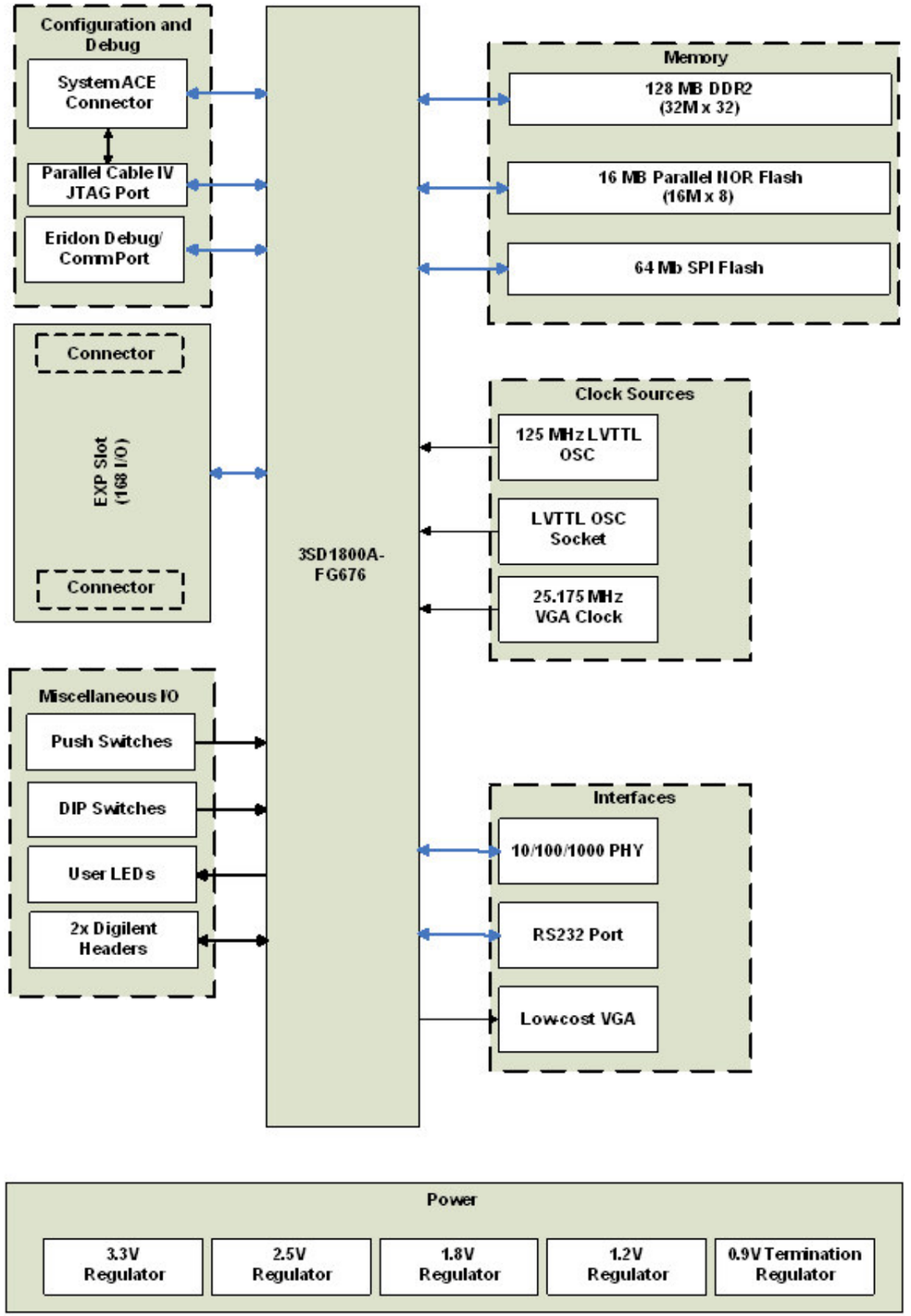
www.em.avnet.com/xilinx

http://www.xilinx.com/s3adspstarter

Xilinx Document Control Number 0381257

09/21/07

Avnet, Inc. *Engineering Services*			Copyright 2007
Title: Spartan-3A DSP Starter Board		Sheet 1 - Lead Sheet	
Size: B	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007		Sheet 1 of 17	



Avnet, Inc. *Engineering Services*

Title	Spartan-3A DSP Starter Board	Sheet 2 - Block Diagram
Size B	Document Number 0381257	Rev 1
Date: Friday, September 21, 2007	Sheet 2 of 17	

4,5,15 EXP2_SE_IO_[0:33] — EXP2_SE_IO_33

14 EXP1_SE_IO_[0:33]
EXP1_SE_IO_0
EXP1_SE_IO_1
EXP1_SE_IO_2
EXP1_SE_IO_3
EXP1_SE_IO_4
EXP1_SE_IO_5
EXP1_SE_IO_6
EXP1_SE_IO_7
EXP1_SE_IO_8
EXP1_SE_IO_9
EXP1_SE_IO_10
EXP1_SE_IO_11
EXP1_SE_IO_12
EXP1_SE_IO_13
EXP1_SE_IO_14
EXP1_SE_IO_15
EXP1_SE_IO_16
EXP1_SE_IO_17
EXP1_SE_IO_18
EXP1_SE_IO_19
EXP1_SE_IO_20
EXP1_SE_IO_21
EXP1_SE_IO_22
EXP1_SE_IO_23
EXP1_SE_IO_24
EXP1_SE_IO_25
EXP1_SE_IO_26
EXP1_SE_IO_27
EXP1_SE_IO_28
EXP1_SE_IO_29
EXP1_SE_IO_30
EXP1_SE_IO_31
EXP1_SE_IO_32
EXP1_SE_IO_33

14 EXP1_DIFF_p[0:21]
EXP1_DIFF_p0
EXP1_DIFF_p1
EXP1_DIFF_p2
EXP1_DIFF_p3
EXP1_DIFF_p4
EXP1_DIFF_p5
EXP1_DIFF_p6
EXP1_DIFF_p7
EXP1_DIFF_p8
EXP1_DIFF_p9
EXP1_DIFF_p11
EXP1_DIFF_p12
EXP1_DIFF_p13
EXP1_DIFF_p14
EXP1_DIFF_p15
EXP1_DIFF_p16
EXP1_DIFF_p17
EXP1_DIFF_p18
EXP1_DIFF_p19
EXP1_DIFF_p20
EXP1_DIFF_p21

14 EXP1_DIFF_n[0:21]
EXP1_DIFF_n0
EXP1_DIFF_n1
EXP1_DIFF_n2
EXP1_DIFF_n3
EXP1_DIFF_n4
EXP1_DIFF_n5
EXP1_DIFF_n6
EXP1_DIFF_n7
EXP1_DIFF_n8
EXP1_DIFF_n9
EXP1_DIFF_n11
EXP1_DIFF_n12
EXP1_DIFF_n13
EXP1_DIFF_n14
EXP1_DIFF_n15
EXP1_DIFF_n16
EXP1_DIFF_n17
EXP1_DIFF_n18
EXP1_DIFF_n19
EXP1_DIFF_n20
EXP1_DIFF_n21

+3.3V
U7
VDD n/c
E/D OUT
GND n/c
C20 0.1uF
R33 33R0
CLK_125MHz
OSC_HC53x_125mhZ

U6A
BANK 0

IP_0	A13	
IP_0	A17	
IP_0_VREF_0	D7	
IP_0	D12	
IP_0_VREF_0	D14	
IP_0	E11	
IP_0	E18	
IP_0_VREF_0	G11	
IP_0	G14	
IP_0	H13	
IP_0	H18	
IP_0	J10	
IP_0	J13	
IP_0	J15	
IP_0	J17	
IP_0_VREF_0		
IO_L01p_0	G20	EXP1_SE_IO_1
IO_L01n_0	F20	EXP1_SE_IO_17
IO_L02p_0_VREF_0	G19	EXP1_SE_IO_3
IO_L02n_0	F19	EXP1_SE_IO_21
IO_L05p_0	D22	EXP1_SE_IO_13
IO_L05n_0	C22	EXP1_SE_IO_0
IO_L06p_0	D23	EXP1_SE_IO_7
IO_L06n_0	C23	EXP1_SE_IO_11
IO_L07p_0	B23	EXP1_SE_IO_9
IO_L07n_0	A22	EXP1_SE_IO_2
IO_L08p_0	H17	EXP1_SE_IO_19
IO_L08n_0	G17	EXP1_SE_IO_23
IO_L09p_0	C21	EXP1_SE_IO_4
IO_L09n_0	B21	EXP1_SE_IO_6
IO_L10p_0	F21	EXP1_SE_IO_5
IO_L10n_0	D21	EXP1_SE_IO_15
IO_L11p_0	D20	EXP1_SE_IO_14
IO_L11n_0	C20	EXP1_SE_IO_8
IO_L12p_0	J16	EXP1_SE_IO_33
IO_L12n_0	K16	EXP1_SE_IO_25
IO_L13p_0	F17	EXP1_SE_IO_27
IO_L13n_0	E17	EXP1_SE_IO_29
IO_L14p_0_VREF_0	B20	EXP1_SE_IO_10
IO_L14n_0	A20	EXP1_SE_IO_12
IO_L15p_0	B19	EXP1_SE_IO_16
IO_L15n_0	A19	EXP1_SE_IO_18
IO_L16p_0	G15	EXP1_DIFF_p15
IO_L16n_0	H15	EXP1_DIFF_n15
IO_L17p_0	D18	EXP1_SE_IO_28
IO_L17n_0	C18	EXP1_SE_IO_20
IO_L18p_0	B18	EXP1_SE_IO_22
IO_L18n_0	A18	EXP1_SE_IO_24
IO_L19p_0	C17	EXP1_SE_IO_26
IO_L19n_0	B17	EXP1_SE_IO_31
IO_L20p_0	E15	EXP1_DIFF_p19
IO_L20n_0_VREF_0	E15	EXP1_DIFF_n19
IO_L21p_0	D17	EXP1_SE_IO_30
IO_L21n_0	C16	EXP1_SE_IO_32
IO_L22p_0	D16	EXP1_DIFF_p20
IO_L22n_0	C15	EXP1_DIFF_n20
IO_L23p_0	B15	EXP1_DIFF_p21
IO_L23n_0	A15	EXP1_DIFF_n21
IO_L24p_0	F14	EXP1_DIFF_p17
IO_L24n_0	F14	EXP1_DIFF_n17
IO_L25p_0_GCLK4	K14	
IO_L25n_0_GCLK5	J14	EXP1_SE_CLK_IN 14
IO_L26p_0_GCLK6	B14	EXP1_DIFF_CLK_IN_p 14
IO_L26n_0_GCLK7	A14	EXP1_DIFF_CLK_IN_n 14
IO_L27p_0_GCLK8	F13	CLK_125MHz
IO_L27n_0_GCLK9	G13	
IO_L28p_0_GCLK10	R13	EXP1_DIFF_p10 14
IO_L28n_0_GCLK11	C13	EXP1_DIFF_n10 14
IO_L29p_0	A12	EXP1_DIFF_p16
IO_L29n_0	B12	EXP1_DIFF_n16
IO_L30p_0	D13	EXP1_DIFF_p18
IO_L30n_0	C12	EXP1_DIFF_n18
IO_L31p_0	F12	EXP1_DIFF_p11
IO_L31n_0	F12	EXP1_DIFF_n11
IO_L32p_0	C11	EXP1_DIFF_p14
IO_L32n_0_VREF_0	D11	EXP1_DIFF_n14
IO_L33p_0	A10	EXP1_DIFF_p7
IO_L33n_0	R10	EXP1_DIFF_n7
IO_L34p_0	C10	EXP1_DIFF_p12
IO_L34n_0	D10	EXP1_DIFF_n12
IO_L35p_0	G12	EXP1_DIFF_p13
IO_L35n_0	H12	EXP1_DIFF_n13
IO_L36p_0	A9	EXP1_DIFF_p8
IO_L36n_0	B9	EXP1_DIFF_n8
IO_L37p_0	E10	EXP1_DIFF_p5
IO_L37n_0	D9	EXP1_DIFF_n5
IO_L38p_0	A8	EXP1_DIFF_p6
IO_L38n_0	B8	EXP1_DIFF_n6
IO_L39p_0	H11	EXP1_DIFF_p9
IO_L39n_0	K12	EXP1_DIFF_n9
IO_L40p_0	C8	EXP1_DIFF_p3
IO_L40n_0	D8	EXP1_DIFF_n3
IO_L41p_0	B6	EXP1_DIFF_p2
IO_L41n_0	C6	EXP1_DIFF_n2
IO_L42p_0	B7	EXP1_DIFF_p4
IO_L42n_0	C7	EXP1_DIFF_n4
IO_L43p_0	J11	EXP1_DIFF_p1
IO_L43n_0	K11	EXP1_DIFF_n1
IO_L44p_0	C5	EXP1_DIFF_p0
IO_L44n_0	D6	EXP1_DIFF_n0
IO_L45p_0	A4	EXP1_DIFF_CLK_OUT_p 14
IO_L45n_0	B4	EXP1_DIFF_CLK_OUT_n 14
IO_L46p_0	G10	EXP1_SE_CLK_OUT 14
IO_L46n_0	H10	
IO_L47p_0	G9	
IO_L47n_0	H9	
IO_L48p_0	F7	
IO_L48n_0	E7	
IO_L51p_0	A3	
IO_L51n_0	B3	
IO_L52p_0_VREF_0	F8	
IO_L52n_0_PUDC_B	G8	FPGA_PUDC 5
IP_0	A7	
IP_0	G16	
IP_0	E9	
IP_0	D15	
IP_0	D19	
IP_0	B24	
IP_0	A5	
IP_0	A23	
IP_0	F9	
IP_0	E20	
IP_0	A24	
IP_0	G18	
IP_0	F10	
IP_0	F18	
IP_0	E6	
IP_0	D5	
IP_0	C4	
IP_0		

XC3SD1800AFG676_1

SWITCH_PB4 — SW8 SPST
SWITCH_PB3 — SW7 SPST
SWITCH_PB2 — SW6 SPST
SWITCH_PB1 — SW5 SPST
Vcco_0
R150 1K
R149 1K
R148 1K
R147 1K

Vcco_0
R156 49.9
R157 49.9
C240 0.1uF
R1 0R0
J1 SMA Connector
DNP

SW3 SW DIP-8
Vcco_0
RP40 1K
RP39 1K

Avnet, Inc. *Engineering Services*			Copyright 2007
Title: Spartan-3A DSP Starter Board		Sheet 3 - FPGA Bank 0	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 3 of 17		

U6B

BANK 1

IP_L65p_1_VREF_1	B26			
IP_L52n_1_VREF_1	G25			
IP_L48n_1	H24			
IP_L44p_1_VREF_1	H26			
IP_L24n_1_VREF_1	U26			
IP_L20n_1_VREF_1	V26			
IP_L28p_1_VREF_1	R23			
IP_L28n_1	R24			
IP_L32p_1	N26			
IP_L32n_1	N25			
IP_L36p_1_VREF_1	M24			
IP_L36n_1	N23			
IP_L40p_1	K24			
IP_L40n_1	L23	SAM_IRQ		10
IO_L01p_1_HDC	Y20	FLASH_WE#		10
IO_L01n_1_LDC2	Y21			
IO_L02p_1_LDC1	AE26	FLASH_OE#		10
IO_L02n_1_LDC0	AD25	FLASH_CE#		10
IO_L03p_1_A0	AC23	FLASH_A0		
IO_L03n_1_A1	AC24	FLASH_A1		
IO_L04p_1	W20	SPISEL_1	5	
IO_L04n_1	W21	SPISEL_2	5	
IO_L05p_1	AD26	SPISEL_3	5	
IO_L05n_1	AC26	SPISEL_4	5	
IO_L06p_1	AC25	SAM_A0		10
IO_L06n_1	AB26	SAM_A1		10
IO_L07p_1	AB23	SAM_A2		10
IO_L07n_1_VREF_1	AB24	SAM_A3		10
IO_L08p_1	V18	SAM_A4		10
IO_L08n_1	V19	SAM_A5		10
IO_L09p_1	AA22	SAM_A6		10
IO_L09n_1	AA23	SAM_D0		10
IO_L10p_1	V21	SAM_D1		10
IO_L10n_1	U20	SAM_D2		10
IO_L11p_1	AA24	SAM_D3		10
IO_L11n_1	AA25	SAM_D4		10
IO_L12p_1	U19	SAM_D5		10
IO_L12n_1	U18	SAM_D6		10
IO_L13p_1	Y22	SAM_D7		10
IO_L13n_1	Y23	SAM_D8		10
IO_L14p_1	U21	SAM_D9		10
IO_L14n_1	T20	SAM_D10		10
IO_L15p_1	Y24	SAM_D11		10
IO_L15n_1	Y25	SAM_D12		10
IO_L17p_1	T18	SAM_D13		10
IO_L17n_1	T17	SAM_D14		10
IO_L18p_1	W23	SAM_D15		10
IO_L18n_1	V22	SAM_OEn		10
IO_L19p_1	V24	SAM_WEn		10
IO_L19n_1	V25	SAM_CEn		10
IO_L21p_1	V23	SAM_RESETn		10
IO_L21n_1	U22	EXP2_SE24		
IO_L22p_1	R19	EXP2_SE29		
IO_L22n_1	R20	EXP2_SE28		
IP_L23p_1	U23	EXP2_SE17		
IO_L23n_1_VREF_1	U24	EXP2_SE19		
IO_L25p_1_A2	R21	FLASH_A2		
IO_L25n_1_A3	R22	FLASH_A3		
IO_L26p_1_A4	T23	FLASH_A4		
IO_L26n_1_A5	T24	FLASH_A5		
IO_L27p_1_A6	R18	FLASH_A6		
IO_L27n_1_A7	R17	FLASH_A7		
IO_L29p_1_A8	R25	FLASH_A8		
IO_L29n_1_A9	R26	FLASH_A9		
IO_L30p_1_RHCLK0	P21	SAM_BRDY		10
IO_L30n_1_RHCLK1	P20	SUSPEND		7
IO_L31p_1_RHCLK2	P26	CLK_25.175MHz		
IO_L31n_1_TRDY1_RHCLK3	P25	LED2		
IO_L33p_1_RHCLK4	P23			
IO_L33n_1_RHCLK5	N24	FLASH_Reset#		10
IO_L34p_1_RDY1_RHCLK6	P18	LED1		
IO_L34n_1_RHCLK7	N19	LED3		
IO_L35p_1_A10	M26	FLASH_A10		
IO_L35n_1_A11	M25	FLASH_A11		
IO_L37p_1	P22	FPGA_RS232_Tx		
IO_L37n_1	N21	FPGA_RS232_Rx		
IO_L38p_1_A12	L24	FLASH_A12		
IO_L38n_1_A13	M23	FLASH_A13		
IO_L39p_1_A14	N18	FLASH_A14		
IO_L39n_1_A15	N17	FLASH_A15		
IO_L41p_1	K25	DAC_VSYNC		13
IO_L41n_1	K26	DAC_HSYNC		13
IO_L42p_1_A16	N20	FLASH_A16		
IO_L42n_1_A17	M20	FLASH_A17		
IO_L43p_1_A18	J26	FLASH_A18		
IO_L43n_1_A19	J25	FLASH_A19		
IO_L45p_1	M21	EXP2_SE20		
IO_L45n_1	M22	EXP2_SE33		
IO_L46p_1	K23	EXP2_SE32		
IO_L46n_1	K22	LED4		
IO_L47p_1	M19	DAC_G0		
IO_L47n_1	M18	DAC_G1		
IO_L49p_1	J23	DAC_G2		
IO_L49n_1	J22	DAC_G3		
IO_L50p_1	L22	DAC_B0		
IO_L50n_1	K21	DAC_B1		
IO_L51p_1	G23	DAC_B2		
IO_L51n_1	G24	DAC_B3		
IO_L53p_1	L20	DAC_R0		
IO_L53n_1	K20	DAC_R1		
IO_L54p_1	F25	DAC_R2		
IO_L54n_1	F24	DAC_R3		
IO_L55p_1	L18	DIGI1_1		
IO_L55n_1	L17	DIGI1_2		
IO_L56p_1	E24	DIGI1_3		
IO_L56n_1	F23	DIGI1_4		
IO_L57p_1	K19	DIGI2_1		
IO_L57n_1	K18	DIGI2_2		
IO_L58p_1_VREF_1	F22	DIGI2_3		
IO_L58n_1	G22	DIGI2_4		
IO_L59p_1	J19	DBG_Rx_p		
IO_L59n_1	J20	DBG_Rx_n		
IO_L60p_1	E26	DBG_Tx_p		
IO_L60n_1	D26	DBG_Tx_n		
IO_L61p_1	D25	LED8		
IO_L61n_1	D24	LED7		
IO_L62p_1_A20	J21	FLASH_A20		
IO_L62n_1_A21	H21	FLASH_A21		
IO_L63p_1_A22	C26	FLASH_A22		
IO_L63n_1_A23	C25	FLASH_A23		
IO_L64p_1_A24	H20	LED5		
IO_L64n_1_A25	G21	LED6		
IP_L16n_1	Y26			
IP_L44n_1	H25			
IP_L16p_1	W25			
IP_L24p_1	U25			
IP_L65n_1	B25			
IP_L20p_1	W26			
IP_L48p_1	H23			
IP_L52p_1	G26			

XC3SD1800AFG676_1

DAC_G[0:3] 13

DAC_B[0:3] 13

DAC_R[0:3] 13

+3.3V

R11 8.25K

R12 49R9

R10 100

R9 49R9

R7 49R9

R6 49R9

R8 4.99K

J3 SATA Connector

Place resistors as close as possible to the FPGA

LED4 R107 681 D11 LED_GREEN

LED1 R110 681 D14 LED_GREEN

LED5 R106 681 D10 LED_GREEN

LED6 R105 681 D9 LED_GREEN

LED2 R109 681 D13 LED_GREEN

LED3 R108 681 D12 LED_GREEN

LED8 R103 681 D7 LED_GREEN

LED7 R104 681 D8 LED_GREEN

FLASH_A0
FLASH_A1
FLASH_A2
FLASH_A3
FLASH_A4
FLASH_A5
FLASH_A6
FLASH_A7
FLASH_A8
FLASH_A9
FLASH_A10
FLASH_A11
FLASH_A12
FLASH_A13
FLASH_A14
FLASH_A15
FLASH_A16
FLASH_A17
FLASH_A18
FLASH_A19
FLASH_A20
FLASH_A21
FLASH_A22
FLASH_A23

FLASH_A[0:23] 10

C56 0.1uF

Vcco_2

U5 SN74CB3T3245DGVR

	19	OE	VCC	20	
EXP2_SE29	2	A1	B1	18	EXP2_SE_IO_29 15
EXP2_SE28	3	A2	B2	17	EXP2_SE_IO_28 15
EXP2_SE17	4	A3	B3	16	EXP2_SE_IO_17 15
EXP2_SE19	5	A4	B4	15	EXP2_SE_IO_19 15
EXP2_SE24	6	A5	B5	14	EXP2_SE_IO_24 15
EXP2_SE20	7	A6	B6	13	EXP2_SE_IO_20 15
EXP2_SE33	8	A7	B7	12	EXP2_SE_IO_33 15
EXP2_SE32	9	A8	B8	11	EXP2_SE_IO_32 15
	10	GND	n/c	1	

+3.3V

DIGI1_1 1
DIGI1_2 2
DIGI1_3 3
DIGI1_4 4
5 6

+3.3V

DIGI2_1 1
DIGI2_2 2
DIGI2_3 3
DIGI2_4 4
5 6

+3.3V

C30 0.1uF

C28 0.1uF C29 0.1uF

U10 MAX3221

1	EN	F_OFF	16
2	C1+	VCC	15
3	V+	GND	14
4	C1-	DOUT	13
5	C2+	F_ON	12
6	C2-	DIN	11
7	V-	INVALID	10
8	RIN	ROUT	9

C27 0.1uF

+3.3V

C32 0.1uF

P2 CONNECTOR DB9

R39 10R0

FPGA_RS232_Tx

FPGA_RS232_Rx

U4 OSC_HC53x_25.175mhZ

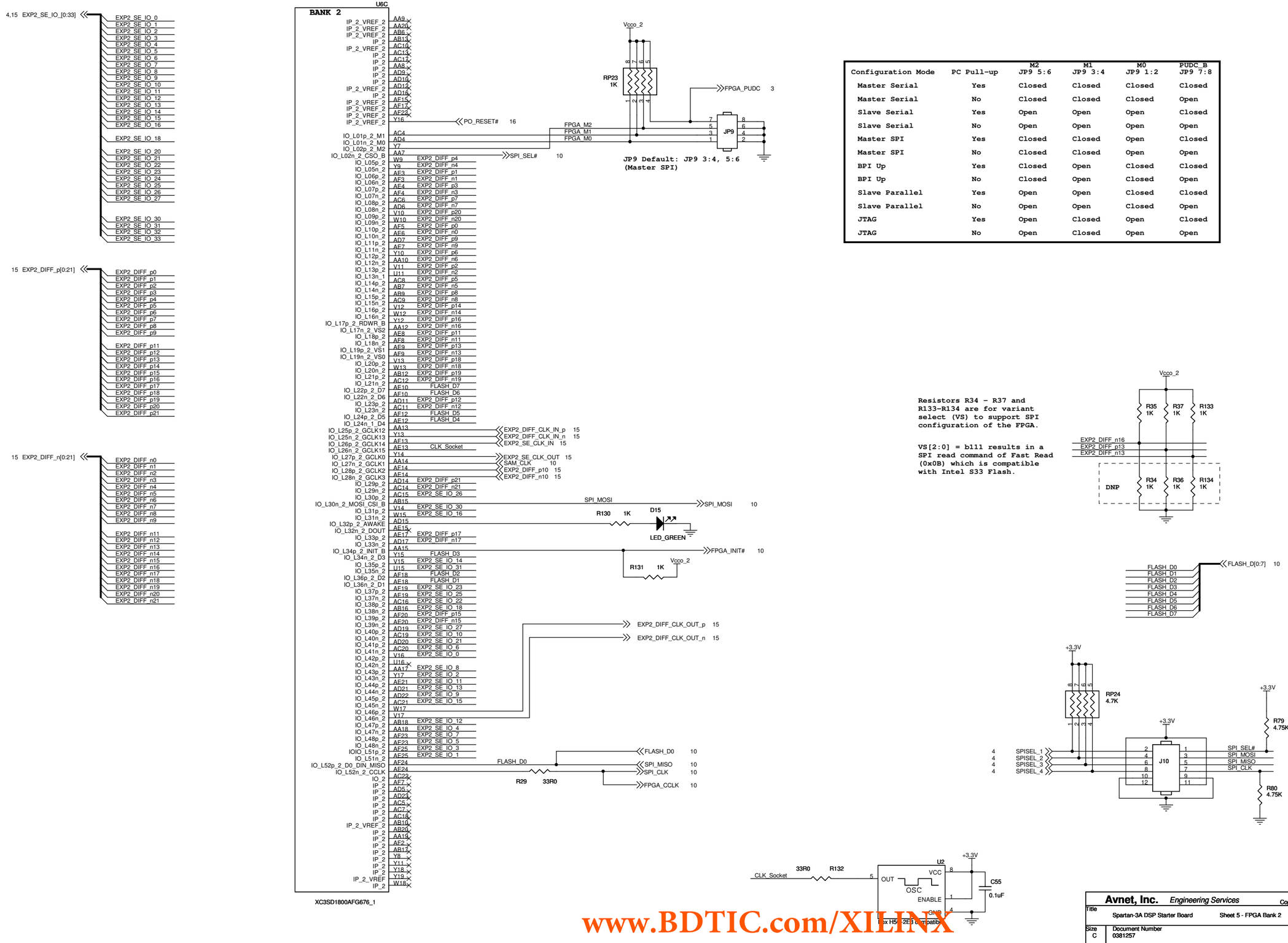
CLK_25.175MHz R22 33R0

n/c VDD 5 6
OUT E/D 4 1
n/c GND 2 3

+3.3V

C1 0.1uF

Avnet, Inc. *Engineering Services*		Copyright 2007
Title: Spartan-3A DSP Starter Board	Sheet 4 - FPGA Bank 1	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 4 of 17	



Configuration Mode	PC Pull-up	M2 JP9 5:6	M1 JP9 3:4	M0 JP9 1:2	PUDC_B JP9 7:8
Master Serial	Yes	Closed	Closed	Closed	Closed
Master Serial	No	Closed	Closed	Closed	Open
Slave Serial	Yes	Open	Open	Open	Closed
Slave Serial	No	Open	Open	Open	Open
Master SPI	Yes	Closed	Closed	Open	Closed
Master SPI	No	Closed	Closed	Open	Open
BPI Up	Yes	Closed	Open	Closed	Closed
BPI Up	No	Closed	Open	Closed	Open
Slave Parallel	Yes	Open	Open	Closed	Closed
Slave Parallel	No	Open	Open	Closed	Open
JTAG	Yes	Open	Closed	Open	Closed
JTAG	No	Open	Closed	Open	Open

Avnet, Inc. *Engineering Services*			Copyright 2007
Title: Spartan-3A DSP Starter Board		Sheet 5 - FPGA Bank 2	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 5 of 17		

1.8V

FPGA_DDR2_VREF

U6D

BANK 3

IP_L16n_3	G1	ETH_CRS
IP_L54p_3	Y3	ETH_COL
IP_L58n_3_VREF_3	AA5	
IP_L04n_3_VREF_3	C1	
IP_L08n_3	D1	ETH_Rx_DV
IP_L12n_3_VREF_3	H4	
IP_L20p_3	J3	ETH_Rx_ER
IP_L20n_3_VREF_3	J2	
IP_L24p_3	J1	ETH_INT#
IP_L24n_3	K1	
IP_L46p_3	U3	
IP_L46n_3	V4	
IP_L50p_3	W1	
IP_L50n_3_VREF_3	W2	
IP_L66p_3	AE1	
IP_L66n_3_VREF_3	AE2	
IO_L01p_3	J8	ETH_Tx_D0
IO_L01n_3	J9	ETH_Tx_D1
IO_L02p_3	R2	ETH_Tx_D2
IO_L02n_3	R1	ETH_Tx_D3
IO_L03p_3	G6	ETH_Tx_D4
IO_L03n_3	H7	ETH_Tx_D5
IO_L05p_3	K9	ETH_Tx_D6
IO_L05n_3	K8	ETH_Tx_D7
IO_L06p_3	D3	ETH_Tx_EN
IO_L06n_3	E4	ETH_Tx_ER
IO_L07p_3	E3	ETH_GTX_CLK
IO_L07n_3	F4	ETH_MDC
IO_L09p_3	F5	ETH_MDIO
IO_L09n_3	G4	ETH_RST#
IO_L10p_3	J7	
IO_L10n_3	H6	
IO_L11p_3	E1	
IO_L11n_3	F2	
IO_L13p_3	K7	
IO_L13n_3	J6	
IO_L14p_3	G3	DDR2_ODT
IO_L14n_3	F3	
IO_L15p_3	L10	DDR2_CAS#
IO_L15n_3	L9	DDR2_WE#
IO_L17p_3	H2	DDR2_CS#
IO_L17n_3	H1	DDR2_RAS#
IO_L18p_3	K6	DDR2_BS0
IO_L18n_3	L7	DDR2_CKE
IO_L19p_3	J5	DDR2_A0
IO_L19n_3	J4	DDR2_BS1
IO_L21p_3	M10	DDR2_A2
IO_L21n_3	M9	DDR2_A1
IO_L22p_3	K5	DDR2_A4
IO_L22n_3	K4	DDR2_A3
IO_L23p_3	K3	DDR2_A6
IO_L23n_3	K2	DDR2_A5
IO_L25p_3	L4	DDR2_A8
IO_L25n_3	L3	
IO_L26p_3	M8	DDR2_A10
IO_L26n_3	M7	DDR2_A9
IO_L27p_3	M4	DDR2_A12
IO_L27n_3	M3	DDR2_A11
IO_L28p_3	M5	
IO_L28n_3	M6	CLK_FB_MB
IO_L29p_3	L2	
IO_L29n_3_VREF_3	M1	
IO_L30p_3	N5	FPGA_DDR_CLK1_p
IO_L30n_3	N4	FPGA_DDR_CLK1_n
IO_L31p_3	N1	FPGA_DDR_CLK0_p
IO_L31n_3	N2	FPGA_DDR_CLK0_n
IO_L32p_3_LHCLK0	N6	ETH_MCLK
IO_L32n_3_LHCLK1	N7	MB_FB_CLK
IO_L33p_3_LHCLK2	P1	ETH_Rx_CLK
IO_L33n_3_IRDY2_LHCLK3	P2	ETH_Tx_CLK
IO_L34p_3_LHCLK4	P4	FPGA_DDR_D30
IO_L34n_3_LHCLK5	P3	FPGA_DDR_D31
IO_L35p_3_TRDY2_LHCLK6	N9	FPGA_DDR_D28
IO_L35n_3_LHCLK7	P10	FPGA_DDR_D29
IO_L36p_3_VREF_3	R1	DDR2_LDM_1
IO_L36n_3	R2	
IO_L37p_3	R3	DDR2_UDQS_1
IO_L37n_3	R4	DDR2_UDQS#_1
IO_L38p_3	T3	FPGA_DDR_D26
IO_L38n_3	T4	FPGA_DDR_D27
IO_L39p_3	P7	FPGA_DDR_D24
IO_L39n_3	P6	FPGA_DDR_D25
IO_L40p_3	R5	FPGA_DDR_D22
IO_L40n_3	R6	FPGA_DDR_D23
IO_L41p_3	P8	FPGA_DDR_D20
IO_L41n_3	P9	FPGA_DDR_D21
IO_L42p_3	T5	DDR2_UDQS_0
IO_L42n_3	U4	DDR2_UDQS#_0
IO_L43p_3_VREF_3	R10	
IO_L43n_3	R9	
IO_L44p_3	U1	FPGA_DDR_D18
IO_L44n_3	U2	FPGA_DDR_D19
IO_L45p_3	R8	FPGA_DDR_D16
IO_L45n_3	R7	FPGA_DDR_D17
IO_L47p_3	V1	DDR2_UDM_0
IO_L47n_3	V2	DDR2_LDM_0
IO_L48p_3	T10	
IO_L48n_3	T9	RST_DQS_DIV
IO_L49p_3	U5	FPGA_DDR_D14
IO_L49n_3	V5	FPGA_DDR_D15
IO_L51p_3	T7	FPGA_DDR_D12
IO_L51n_3	U6	FPGA_DDR_D13
IO_L52p_3	W3	DDR2_LDQS_1
IO_L52n_3	W4	DDR2_LDQS#_1
IO_L53p_2	Y1	FPGA_DDR_D10
IO_L53n_3	Y2	FPGA_DDR_D11
IO_L55p_3	AA2	FPGA_DDR_D8
IO_L55n_3	AA3	FPGA_DDR_D9
IO_L56p_3	U7	FPGA_DDR_D6
IO_L56n_3	U8	FPGA_DDR_D7
IO_L57p_3	Y5	FPGA_DDR_D4
IO_L57n_3	Y6	FPGA_DDR_D5
IO_L59p_3	V7	DDR2_LDQS_0
IO_L59n_3	V6	DDR2_LDQS#_0
IO_L60p_3	AB1	FPGA_DDR_D2
IO_L60n_3	AC1	FPGA_DDR_D3
IO_L61p_3	U9	FPGA_DDR_D0
IO_L61n_3	V8	FPGA_DDR_D1
IO_L63p_3	W7	
IO_L63n_3	W6	
IO_L64p_3	AC2	
IO_L64n_3	AC3	
IO_L65p_3	AD1	
IO_L65n_3	AD2	
IP_L04p_3	C2	ETH_Rx_D0
IP_L16p_3	G2	ETH_Rx_D1
IP_L12p_3	G5	ETH_Rx_D2
IP_L08p_3	D2	ETH_Rx_D3
IP_L62p_3	AB3	ETH_Rx_D4
IP_L58p_3	AA4	ETH_Rx_D5
IP_L62n_3	AB4	ETH_Rx_D6
IP_L54n_3	Y4	ETH_Rx_D7

XC3SD1800AFG676_1

R141 22R0 FPGA_DDR_BS0 8,9

R140 24R3 FPGA_DDR_A7

R138 22R0 FPGA_DDR_UDM_1 8,9

Place R136 close to pin N7

R136 60R4 FPGA_0.9V_TT

MB_FB_CLK - This trace should have length equal to DDR_CLK trace length + DQStrace length

RST_DQS_DIV - The trace from T10 to T9 should have length equal to DDR_CLK trace length + DQStrace length

R137 22R0

R135 60R4 FPGA_0.9V_TT

Place R135 close to pin T9

FPGA_DDR2_VREF

C127 0.01uF C117 0.01uF C112 0.01uF C129 0.01uF C133 0.01uF C135 1.0uF C138 1.0uF C137 1.0uF C131 1.0uF

RP3 33R0

DDR2_A0	8	1 FPGA_DDR_A0
DDR2_CAS#	7	2 FPGA_DDR_CAS# 8,9
DDR2_WE#	6	3 FPGA_DDR_WE# 8,9
DDR2_A2	5	4 FPGA_DDR_A2

R139 10K

RP4 33R0

DDR2_CKE	8	1 FPGA_DDR_CKE 8
DDR2_A4	7	2 FPGA_DDR_A4
DDR2_A1	6	3 FPGA_DDR_A1
DDR2_A10	5	4 FPGA_DDR_A10

RP11 33R0

DDR2_ODT	8	1
DDR2_BS1	7	2 DDR2_ODT_Control 8
DDR2_A3	6	3 FPGA_DDR_BS1 8,9
	5	4 FPGA_DDR_A3

RP2 33R0

	8	1
	7	2
DDR2_RAS#	6	3 FPGA_DDR_RAS# 8,9
DDR2_CS#	5	4 FPGA_DDR_CS# 8,9

RP13 33R0

DDR2_A8	8	1 FPGA_DDR_A8
	7	2
DDR2_A11	6	3 FPGA_DDR_A11
DDR2_A12	5	4 FPGA_DDR_A12

RP12 33R0

DDR2_A5	8	1 FPGA_DDR_A5
DDR2_A6	7	2
DDR2_A9	6	3 FPGA_DDR_A6
	5	4 FPGA_DDR_A9

RP6 33R0

FPGA_DDR_CLK1_n	8	1
FPGA_DDR_CLK1_p	7	2 FPGA_DDR_CLK_1# 8
FPGA_DDR_CLK0_n	6	3 FPGA_DDR_CLK_1 8
FPGA_DDR_CLK0_p	5	4 FPGA_DDR_CLK_0# 8
		FPGA_DDR_CLK_0 8

RP15 33R0

CLK_FB_MB	8	1 MB_FB_CLK
DDR2_LDM_1	7	2 FPGA_DDR_LDM_1 8,9
DDR2_UDQS_1	6	3 FPGA_DDR_UDQS_1 8,9
DDR2_UDQS#_1	5	4 FPGA_DDR_UDQS#_1 8,9

RP16 24R0

DDR2_UDQS_0	8	1 FPGA_DDR_UDQS_0 8,9
DDR2_UDQS#_0	7	2 FPGA_DDR_UDQS#_0 8,9
DDR2_LDM_0	6	3 FPGA_DDR_LDM_0 8,9
DDR2_UDM_0	5	4 FPGA_DDR_UDM_0 8,9

RP33 24R0

DDR2_LDQS#_1	8	1 FPGA_DDR_LDQS#_1 8,9
DDR2_LDQS_1	7	2 FPGA_DDR_LDQS_1 8,9
DDR2_LDQS#_0	6	3 FPGA_DDR_LDQS#_0 8,9
DDR2_LDQS_0	5	4 FPGA_DDR_LDQS_0 8,9

+1.8V +2.5V

C26 0.1uF C25 0.1uF

U9

ETH_MDIO 2 A1 Y1 13 GMII_MDIO 11
ETH_MDC 3 A2 Y2 12 GMII_MDC 11
4 A3 Y3 11
5 A4 Y4 10
1 VCCA 14 VCCY
8 EN GND 7

ADG3304

R151 1K +1.8V

FPGA_DDR_A[0:12] 8,9

FPGA_DDR_A0 FPGA_DDR_A1 FPGA_DDR_A2 FPGA_DDR_A3 FPGA_DDR_A4 FPGA_DDR_A5 FPGA_DDR_A6 FPGA_DDR_A7 FPGA_DDR_A8 FPGA_DDR_A9 FPGA_DDR_A10 FPGA_DDR_A11 FPGA_DDR_A12

FPGA_DDR_D[0:31] 8,9

FPGA_DDR_D0 FPGA_DDR_D1 FPGA_DDR_D2 FPGA_DDR_D3 FPGA_DDR_D4 FPGA_DDR_D5 FPGA_DDR_D6 FPGA_DDR_D7 FPGA_DDR_D8 FPGA_DDR_D9 FPGA_DDR_D10 FPGA_DDR_D11 FPGA_DDR_D12 FPGA_DDR_D13 FPGA_DDR_D14 FPGA_DDR_D15 FPGA_DDR_D16 FPGA_DDR_D17 FPGA_DDR_D18 FPGA_DDR_D19 FPGA_DDR_D20 FPGA_DDR_D21 FPGA_DDR_D22 FPGA_DDR_D23 FPGA_DDR_D24 FPGA_DDR_D25 FPGA_DDR_D26 FPGA_DDR_D27 FPGA_DDR_D28 FPGA_DDR_D29 FPGA_DDR_D30 FPGA_DDR_D31

U18

+1.8V C4 H4 VCCA VCCB C3 H3 +2.5V

ETH_CRS	A6	1A1	1B1	A1	GMII_CRS 11
ETH_COL	A5	1A2	1B2	A2	GMII_COL 11
ETH_Rx_DV	B6	1A3	1B3	B1	GMII_RX_DV 11
ETH_Rx_ER	B5	1A4	1B4	B2	GMII_RX_ER 11
ETH_INT#	C6	1A5	1B5	C1	GBEINT# 11
ETH_MCLK	C5	1A6	1B6	C2	GBE_MCLK 11
ETH_Rx_CLK	D6	1A7	1B7	D1	GMII_RX_CLK 11
ETH_Tx_CLK	D5	1A8	1B8	D2	GMII_TX_CLK 11
	E6	1A9	1B9	E1	
	E5	1A10	1B10	E2	
ETH_Rx_D0	F6	2A1	2B1	F1	GMII_RXD0 11
ETH_Rx_D1	F5	2A2	2B2	F2	GMII_RXD1 11
ETH_Rx_D2	G6	2A3	2B3	G1	GMII_RXD2 11
ETH_Rx_D3	G5	2A4	2B4	G2	GMII_RXD3 11
ETH_Rx_D4	H6	2A5	2B5	H1	GMII_RXD4 11
ETH_Rx_D5	H5	2A6	2B6	H2	GMII_RXD5 11
ETH_Rx_D6	J6	2A7	2B7	J1	GMII_RXD6 11
ETH_Rx_D7	J5	2A8	2B8	J2	GMII_RXD7 11
	K6	2A9	2B9	K1	
	K5	2A10	2B10	K2	
	A3	1DIR	2DIR	K3	
	A4	1OE	2OE	K4	
	B3	GND	GND	G3	
	B4	GND	GND	G4	
	D3	GND	GND	J3	
	D4	GND	GND	J4	

SN74AVC20T245ZQL

+1.8V C203 0.1uF C201 0.1uF C202 0.1uF C200 0.1uF

+2.5V C208 0.1uF C205 0.1uF C207 0.1uF C206 0.1uF

U17

+1.8V C4 H4 VCCA VCCB C3 H3 +2.5V

ETH_Tx_D0	A6	1A1	1B1	A1	GMII_TXD0 11
ETH_Tx_D1	A5	1A2	1B2	A2	GMII_TXD1 11
ETH_Tx_D2	B6	1A3	1B3	B1	GMII_TXD2 11
ETH_Tx_D3	B5	1A4	1B4	B2	GMII_TXD3 11
ETH_Tx_D4	C6	1A5	1B5	C1	GMII_TXD4 11
ETH_Tx_D5	C5	1A6	1B6	C2	GMII_TXD5 11
ETH_Tx_D6	D6	1A7	1B7	D1	GMII_TXD6 11
ETH_Tx_D7	D5	1A8	1B8	D2	GMII_TXD7 11
ETH_Tx_EN	E6	1A9	1B9	E1	GMII_TX_EN 11
ETH_Tx_ER	E5	1A10	1B10	E2	GMII_TX_ER 11
ETH_GTX_CLK	F6	2A1	2B1	F1	GMII_GTX_CLK 11
	F5	2A2	2B2	F2	
	G6	2A3	2B3	G1	
ETH_RST#	G5	2A4	2B4	G2	GBE_RST# 11
	H6	2A5	2B5	H1	
	H5	2A6	2B6	H2	
	J6	2A7	2B7	J1	
	J5	2A8	2B8	J2	
	K6	2A9	2B9	K1	
	K5	2A10	2B10	K2	
	A3	1DIR	2DIR	K3	
	A4	1OE	2OE	K4	
	B3	GND	GND	G3	
	B4	GND	GND	G4	
	D3	GND	GND	J3	
	D4	GND	GND	J4	

+1.8V +1.8V

SN74AVC20T245ZQL

Avnet, Inc.	Engineering Services	Copyright 2007
Title: Spartan-3A DSP Starter Board	Sheet 6 - FPGA Bank 3	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 6 of 17	

EXP1 VOLTAGE SELECT

+2.5V Vcco_0 +3.3V

JP2

Default: JP2 1:2 (VCCO_0 = +3.3V)

EXP2 VOLTAGE SELECT

+2.5V Vcco_2 +3.3V

JP3

Default: JP3 1:2 (VCCO_2 = +3.3V)

Cap Size 0201: C83 C119 C72 C116 C66 C102 C122 C68 (0.01uF); C61 C67 C58 C60 C63 (0.01uF)

Cap Size 0402: C64 C123 C75 C62 (1.0uF); C57 C69 C59 (1.0uF)

Cap Size 0603: C5 C14 (4.7uF); C6 C8 (4.7uF)

Cap Size TAND: +2.5V C23 470uF; +3.3V C7 470uF

10 JTAG_TCK — JTAG_TCK
10 JTAG_TMS — JTAG_TMS
10 FPGA_TDO — JTAG_TDO
10 FPGA_TDI — JTAG_TDI

+2.5V R53 4.75K **Default: JP7 Unpopulated**

SW2 SPST; C43 0.1uF; JP7

FPGA_PROG# 10

4 SUSPEND

+2.5V R113 4.02K **JP11 default setting 1:2** JP11; R112 10K

+3.3V R83 681; D1 LED_BLU; Q2 2N7002

+2.5V R78 4.75K

10 FPGA_DONE

VCC_INT: U12 T11 T13 T15 R12 R14 B16 P11 P13 P14 P15 N12 N13 N14 M6 M11 M13 M15 L12 L13 L14 L16 K15 (VCCINT)

+2.5V: V9 J14 T22 P17 N10 K3 K13 J18 E5 E18 E22 AB5 AB11 AB22 (VCCAUX)

U6E

JTAG_TCK A25 TCK
JTAG_TMS D4 TMS
FPGA_TDO F23 TDO
FPGA_TDI G7 TDI
A2 PR0G_B
V20 SUSPEND
AB21 DONE

W8 W14 W19 W24 V3 U10 U13 U17 T1 T6 T12 T14 T16 T21 T26 R11 R13 R15 P12 P16 P19 P24 N8 N11 N15 M12 M14 M16 L1 L6 L11 (GND)

L13 L15 L23 L25 K10 K17 J24 H3 H8 H14 H19 F1 F5 F11 F16 F21 F26 C3 C9 C14 C20 C24 AE1 AE6 AE11 AE15 AE21 AE26 AD3 AD8 AD13 AD18 AD24 AA1 AA6 AA11 AA16 AA21 AA26 A1 A6 A11 A16 A21 A26 (GND)

XC3SD1800AFG676_1

Vcco_0: H11 H16 E8 E13 E19 R5 B11 B16 B22 (VCCO_0)

+3.3V: W22 T19 T25 N22 L19 L25 H22 E25 AB25 (VCCO_1)

Vcco_2: W11 W16 AE5 AE11 AE16 AE22 AB8 AB14 AB19 (VCCO_2)

+1.8V: W5 T2 T8 P5 L2 L8 H5 E2 AB2 (VCCO_3)

Cap Size 0201: C94 C104 C78 C86 C82 C108 C79 C88 C80 C81 C97 C107 C105 (0.01uF); C115 C73 C110 C84 C109 (0.01uF); C101 C77 C71 C114 C103 (0.01uF); C118 C132 C120 C121 C130 (0.01uF)

Cap Size 0402: C93 C98 C106 C92 C96 C95 C87 (1.0uF); C125 C70 C99 (1.0uF); C65 C124 C91 (1.0uF); C128 C134 C139 (1.0uF)

Cap Size 0603: C12 C15 C13 C16 (4.7uF); C2 C4 (4.7uF); C11 C9 (4.7uF); C24 C31 (4.7uF)

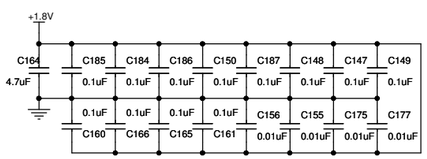
Cap Size TAND: VCC_INT C17 470uF; Vcco_0 C3 470uF; Vcco_2 C10 470uF; +1.8V C22 470uF

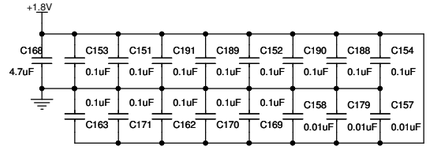
Avnet, Inc. *Engineering Services* Copyright 2007

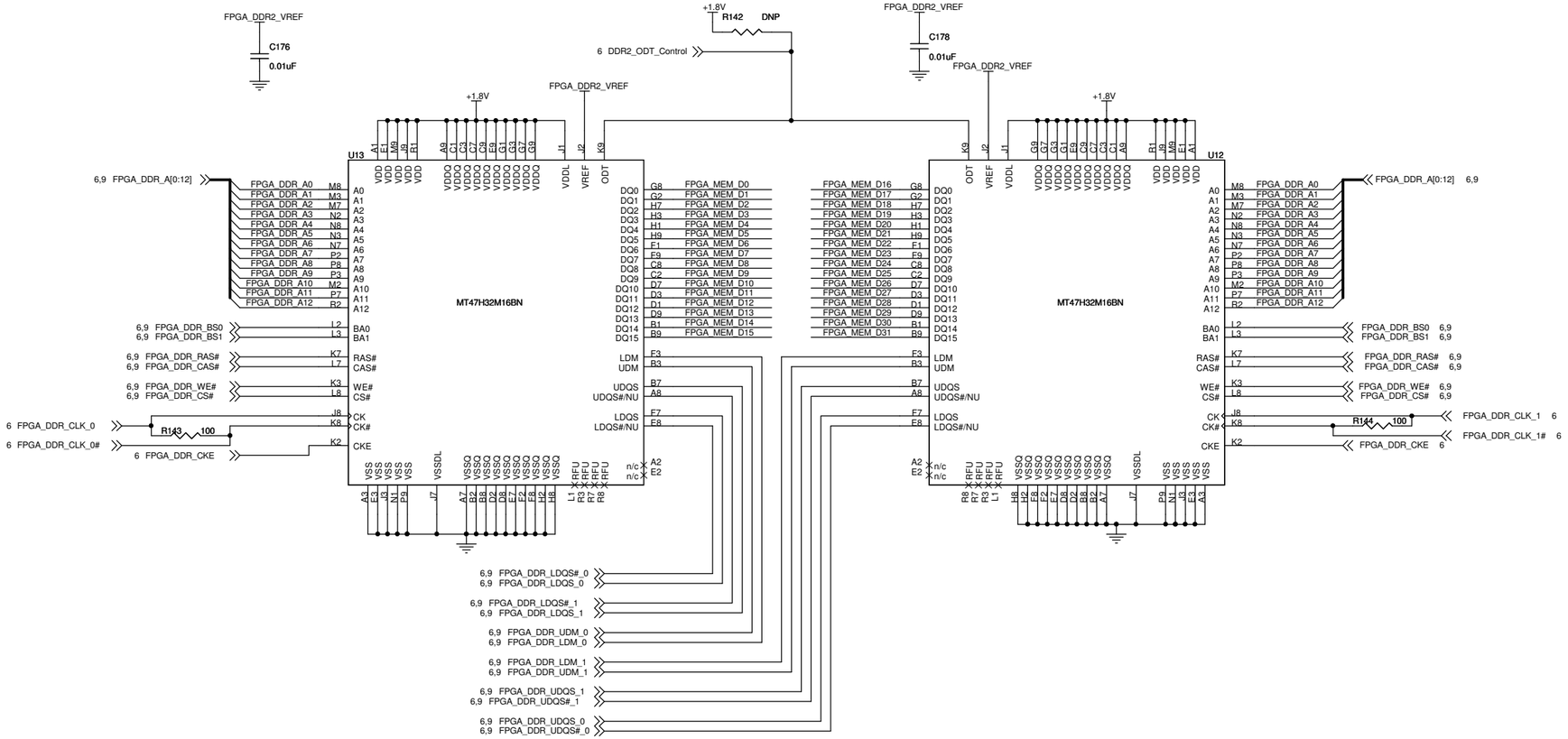
Title: Spartan-3A DSP Starter Board — Sheet 7 - FPGA Power

Size C | Document Number 0381257 | Rev 1

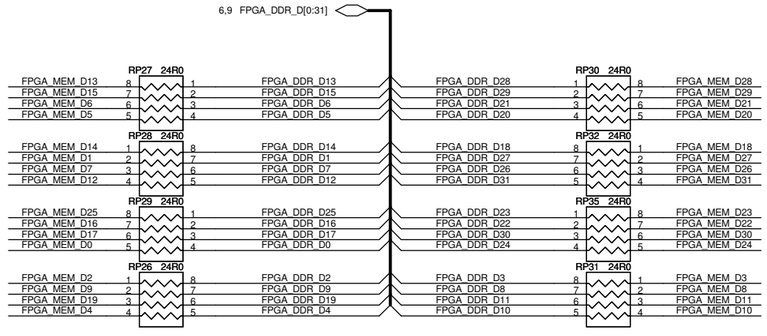
Date: Friday, September 21, 2007 | Sheet 7 of 17



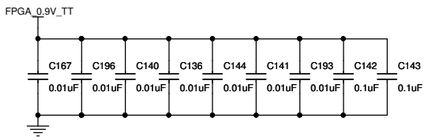


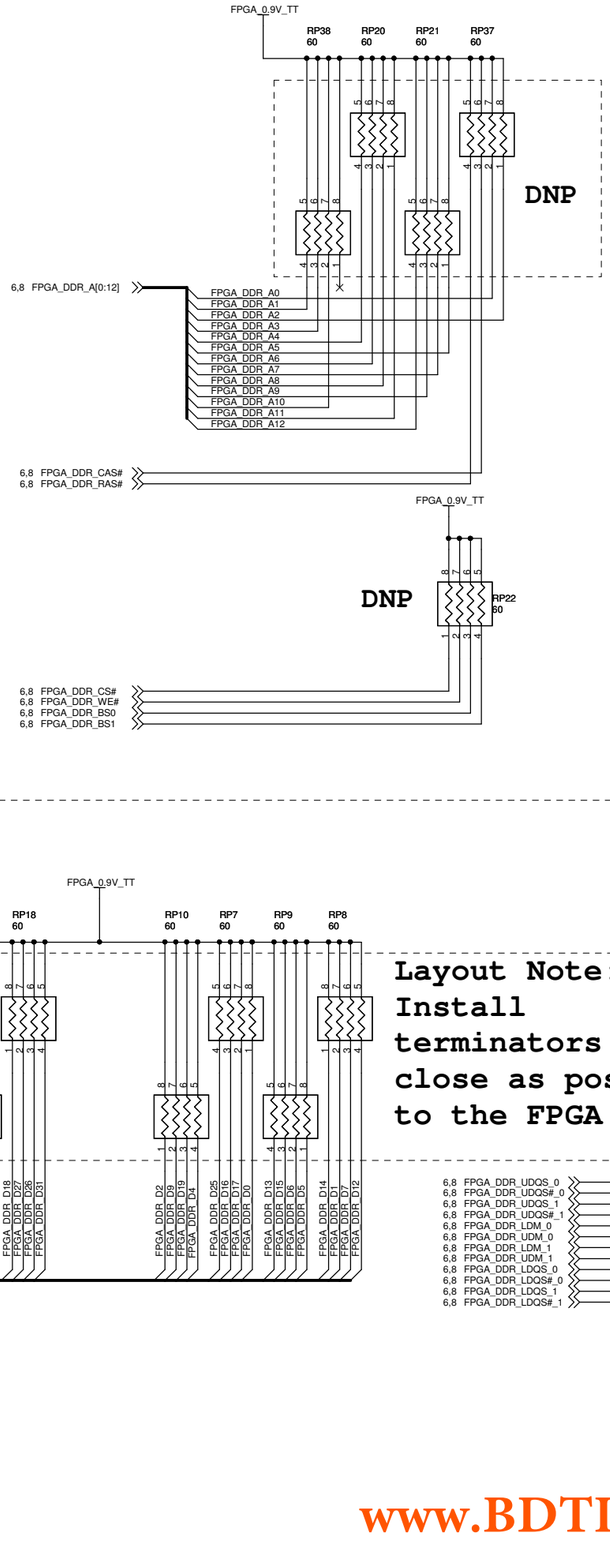


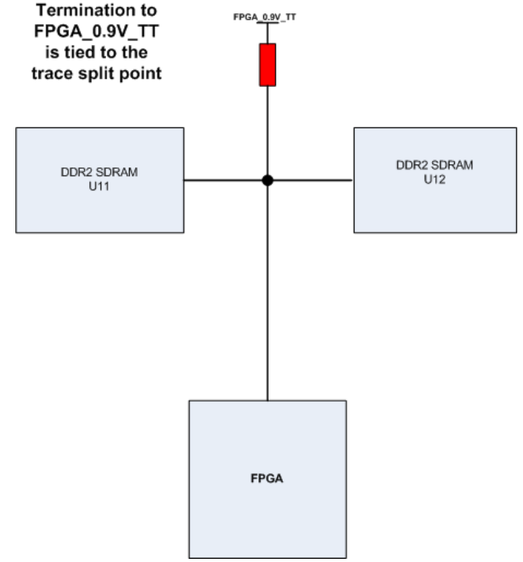
Place series terminations close to FPGA

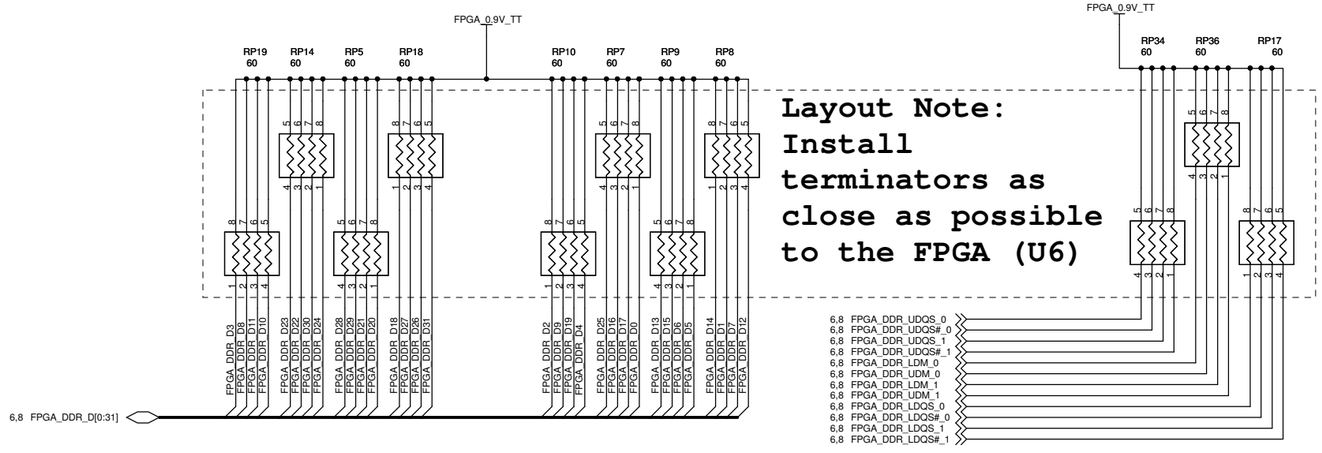


Avnet, Inc. *Engineering Services*			Copyright 2007
Title: Spartan-3A DSP Starter Board		Sheet 8 - DDR2 Memory	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 8 of 17		

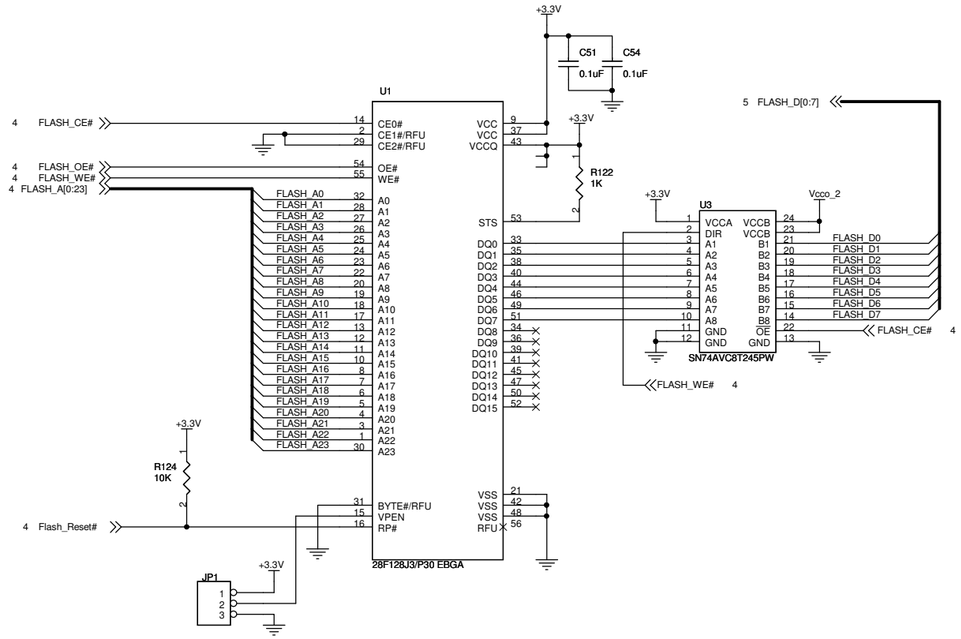




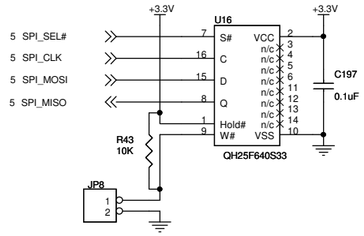




Avnet, Inc. *Engineering Services*		Copyright 2007
Title: Spartan-3A DSP Starter Board	Sheet 9 - DDR2 Termination	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 9 of 17	

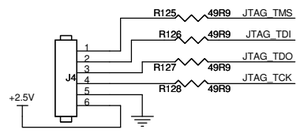


Default: JP1 1:2

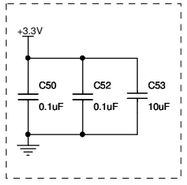


Default: JP8 No Jumper

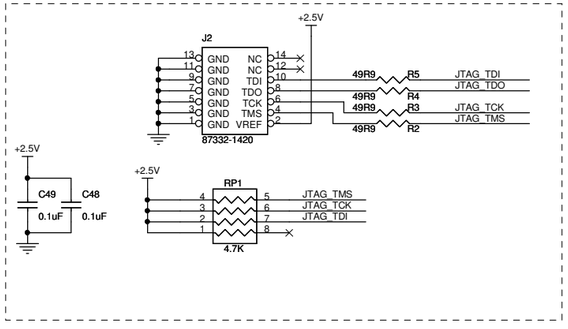
7 JTAG_TCK
7 JTAG_TMS
7 FPGA_TDO
7 FPGA_TDI

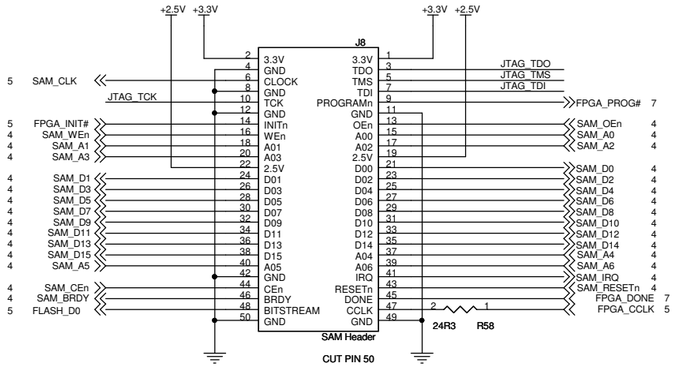


Layout Note: Place J4 and J2 close together



JTAG Parallel IV Connector





Avnet, Inc. *Engineering Services*			Copyright 2007
Title: Spartan-3A DSP Starter Board		Sheet 10 - Configuration/Flash Memory	
Size: C	Document Number: 0381257		Rev: 1
Date: Friday, September 21, 2007	Sheet 10 of 17		

6 GMII_TXD0
6 GMII_TXD1
6 GMII_TXD2
6 GMII_TXD3
6 GMII_TXD4
6 GMII_TXD5
6 GMII_TXD6
6 GMII_TXD7
6 GMII_TX_EN
6 GMII_TX_ER
6 GMII_GTX_CLK
R45 22
R44 22
R47 22
R46 22
R54 22
R53 22
R49 22
R48 22
R51 22
R50 22
R52 22
Place close to FPGA

6 GMII_TX_CLK
6 GMII_RXD0
6 GMII_RXD1
6 GMII_RXD2
6 GMII_RXD3
6 GMII_RXD4
6 GMII_RXD5
6 GMII_RXD6
6 GMII_RXD7
6 GMII_RX_DV
6 GMII_RX_ER
6 GMII_RX_CLK
6 GMII_CRS
R65 22
R70 22
R72 22
R76 22
R77 22
R82 22
R85 22
R87 22
R89 22
R90 22
R111 22
R68 22
R115 22
Place close to PHY

+2.5V
R120 1K
6 GMII_COL
R121 22
Place close to PHY

+2.5V
R116 1K
R62 100K DNP
6 GMII_MDC
6 GMII_MDIO
6 GBEINT#

6 GBE_MCLK
R61 22
Place close to PHY

+2.5V
R118 DNP
6 GBE_RST#
R119 1K

R60 10M
Y1
XTAL-25MHz
C44 22pF
C47 22pF

U22A DP83865DVH

TXD0/TX0 76
TXD1/TX1 75
TXD2/TX2 72
TXD3/TX3 71
TXD4 68
TXD5 67
TXD6 66
TXD7 65
TX_EN/TXEN_ER 62
TX_CLK/RGMII_SEL1 60
GTX_CLK/TCK 79
TX_ER 61
RXD0/RX0 56
RXD1/RX1 55
RXD2/RX2 52
RXD3/RX3 51
RXD4 50
RXD5 47
RXD6 46
RXD7 45
RX_DV/RCK 44
RX_ERXDV_ER 41
RX_CLK 57
COL/CLK_MAC_FREQ 39
CRS/RGMII_SEL0 40
MDC 81
MDIO 80
INTERRUPT 3
CLK_IN 86
CLK_OUT 87
CLK_TO_MAC 85
RESET 33
MDIX_EN 89
MAN_MDIX/TX_TCLK 6
MULTI_EN/TX_TRIG 94
NON_IEEE 1
MAC_CLK_EN/TX_SYN_CLK 88

MDIA_N 109
MDIA_P 108
MDIB_N 115
MDIB_P 114
MDIC_N 121
MDIC_P 120
MDID_N 127
MDID_P 126
PHY_ADDR4 95
PHY_ADDR3 18
PHY_ADDR2 17
PHY_ADDR1 14
LED_DUP/PHY_ADDR0 13
LED_ACT/SPD0 7
LED_LNK_10/SPD1 8
LED_LNK_100/DUPLEX 9
LED_LNK_1000/AN_EN 10
TCK 24
TMS 27
TDI 31
TDO 28
TRST 32

+2.5V
R69 49.9 1%
R67 49.9 1%
R75 49.9 1%
R71 49.9 1%
R84 49.9 1%
R81 49.9 1%
R88 49.9 1%
R86 49.9 1%

J9 1-6605833-1 LINK
SHIELD 11
VCC_CT 1
MX0_N 3
MX0_P 2
MX1_N 5
MX1_P 4
MX2_N 7
MX2_P 6
MX3_N 9
MX3_P 8
CH_GND 10
SHIELD 12
ACT
D1 13
D2 14
D3 15
D4 16

+2.5V
R114 10R0

RP25 4.7K

LNK10
LNK100
LNK1000

U26 74V1G04
U24 74V1G08
U25 74V1G08

JT6 0R
R59 1K
JT7 0R
Speed0

R117 1K

JT8 0R
LNK1000
D2 LED_GRN
R92 330
R91 1K
JT9 0R
Auto-Neg

JT10 0R
LNK100
D3 LED_GRN
R94 330
R93 1K
JT11 0R
Duplex

JT12 0R
LNK10
D4 LED_GRN
R96 330
R95 1K
JT13 0R
Speed1

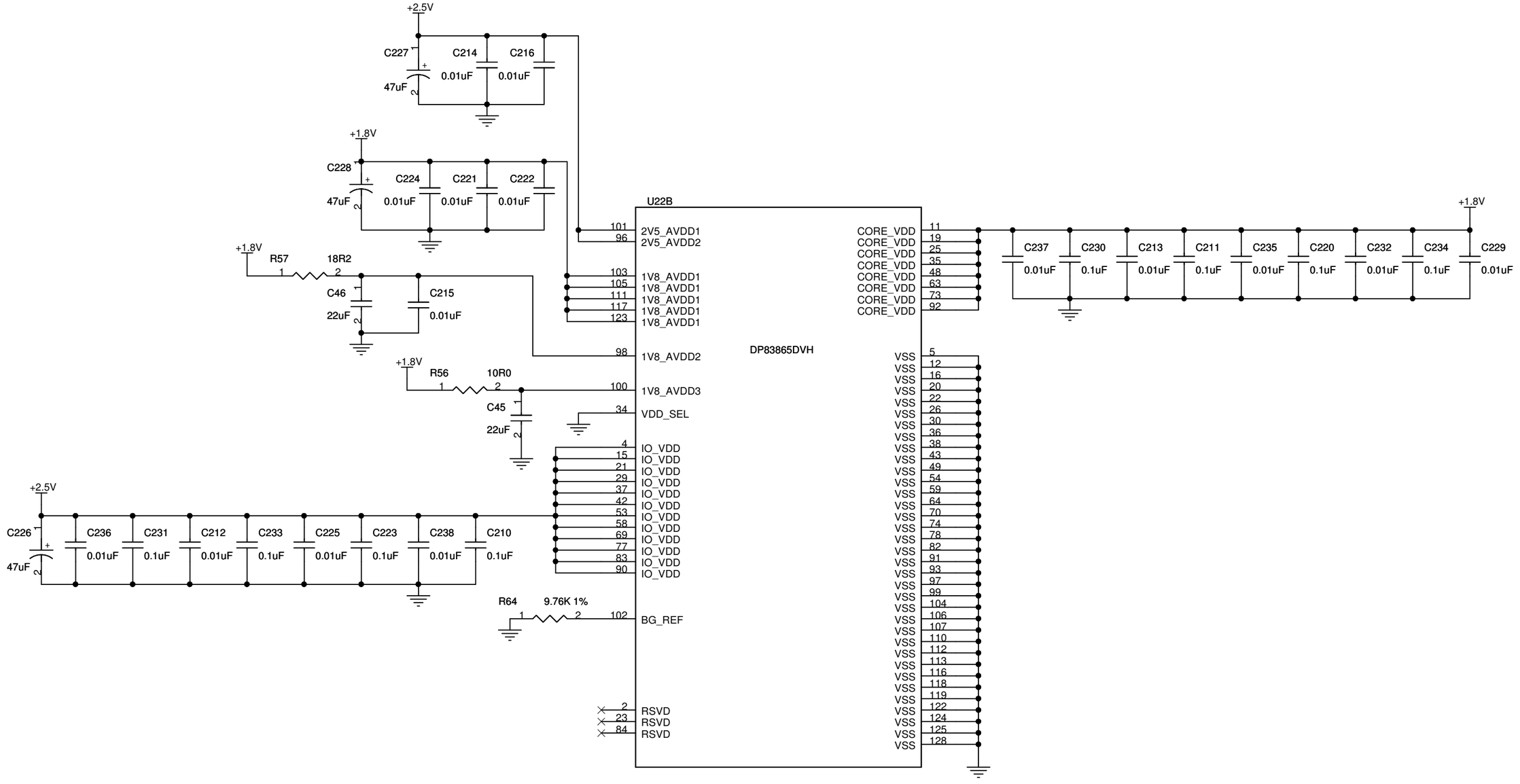
JT14 0R
DUPLEX
D5 LED_GRN
R98 330
R97 1K
JT15 0R
PHY ADDR0

JT1 1K
NON-IEEE
JT2 1K
MAN-MDIX
JT5 1K
MAC CLK-EN
JT3 1K
MULTI-EN
JT4 1K
MDIX-EN

Default position is 1-2
for all JTx jumpers

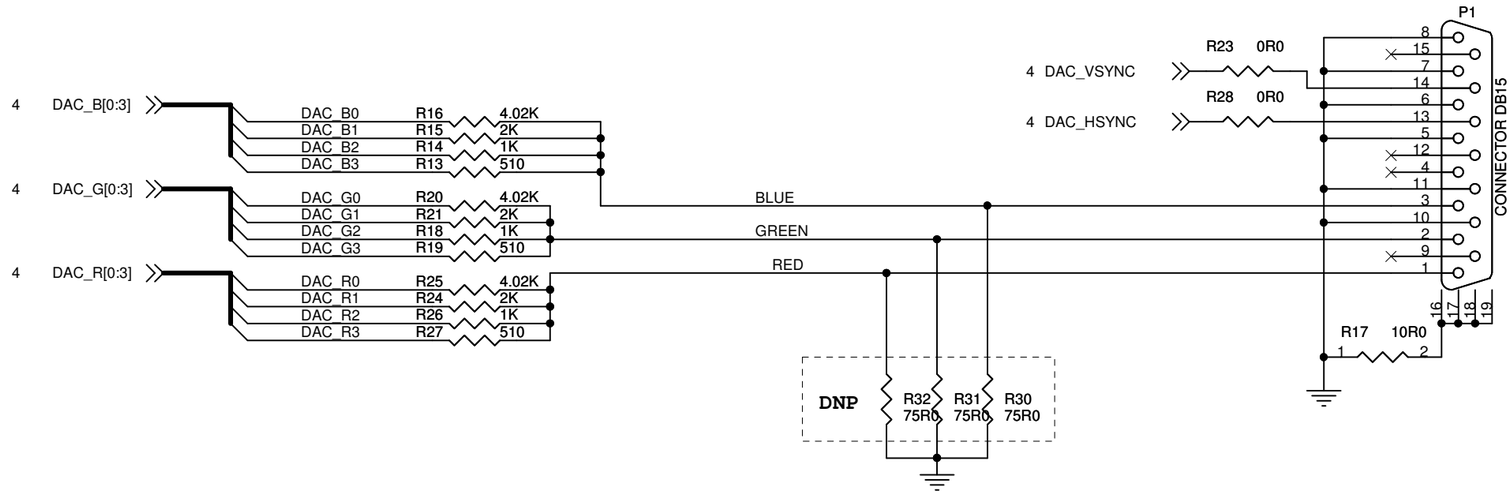
Avnet, Inc. Engineering Services

Title: Spartan-3A DSP Starter Board
Sheet 11 - 10/100/1000 PHY
Size C
Document Number 0381257
Rev 1
Date: Friday, September 21, 2007
Sheet 11 of 17

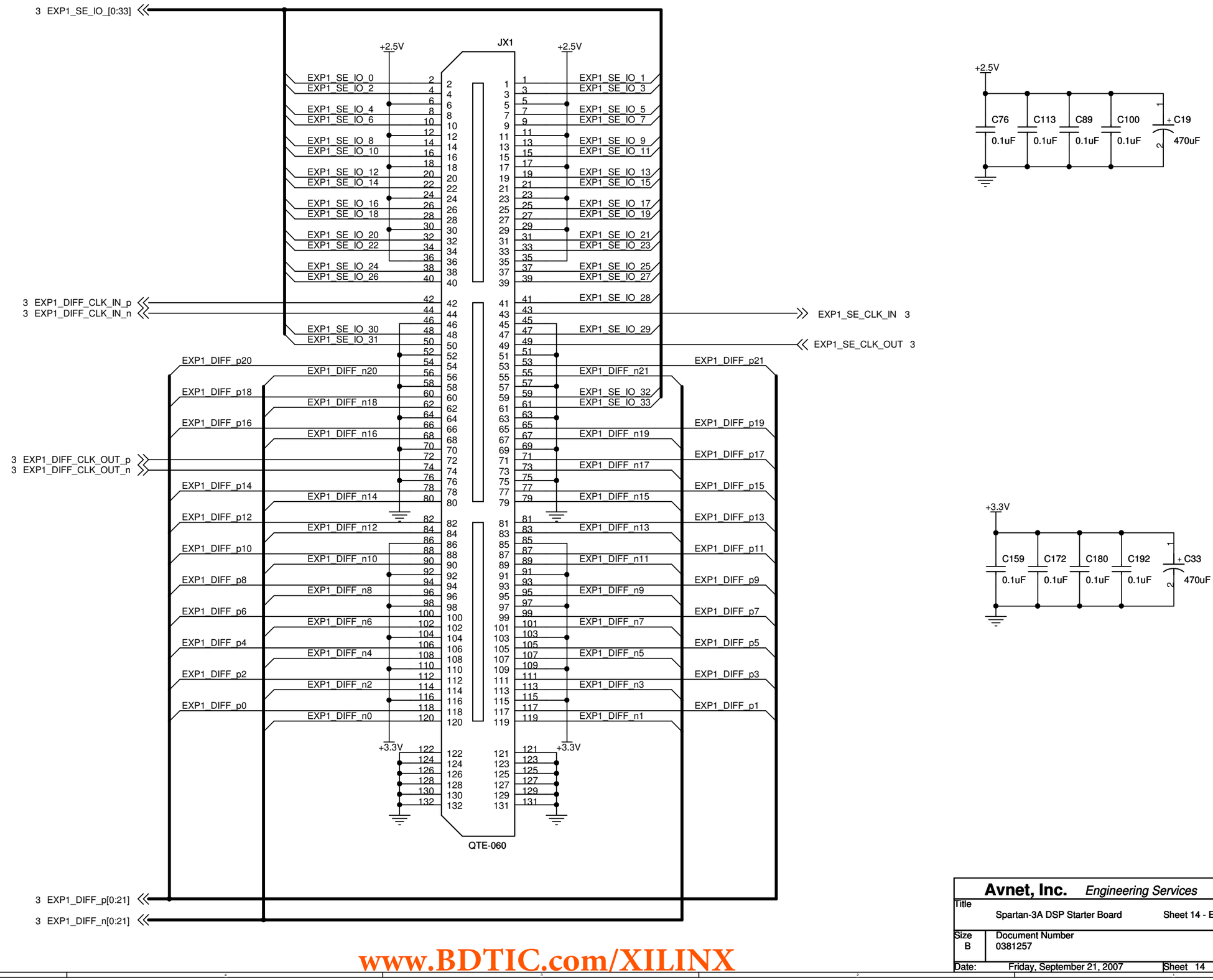


Avnet, Inc. *Engineering Services*

Title: Spartan-3A DSP Starter Board	Sheet 12 - PHY Power	
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 12 of 17	

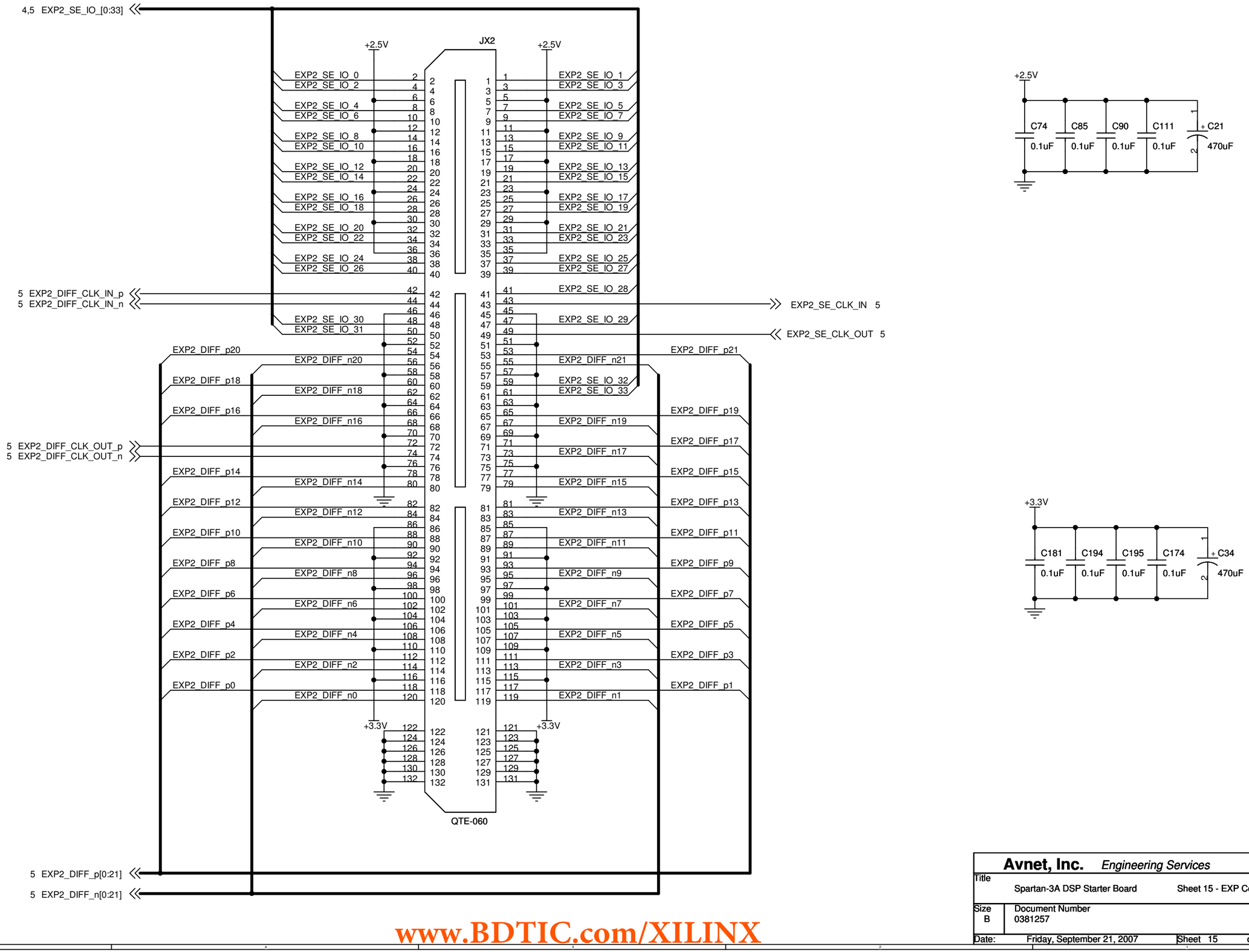


Avnet, Inc. *Engineering Services*		Copyright 2007
Title: Spartan-3A DSP Starter Board	Sheet 13 - DAC Out	
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 13 of 17	



Avnet, Inc. *Engineering Services*

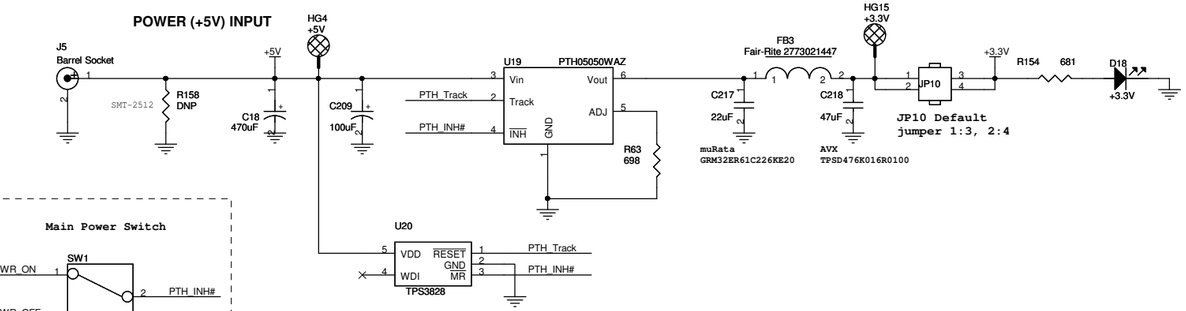
Title: Spartan-3A DSP Starter Board	Sheet 14 - EXP Connector (JX1)	
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 14 of 17	

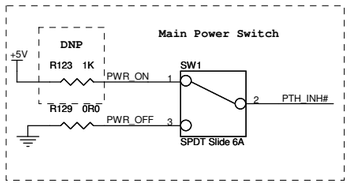


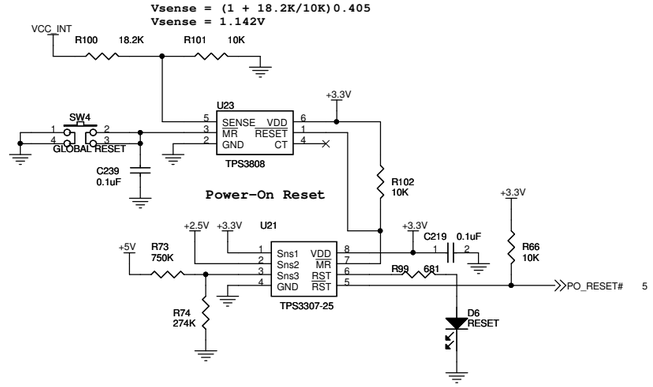
Avnet, Inc. *Engineering Services* Copyright 2007

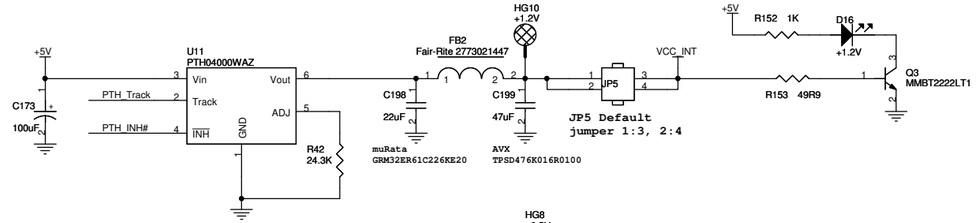
Title: Spartan-3A DSP Starter Board		Sheet 15 - EXP Connextor (JX2)
Size: B	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 15 of 17	

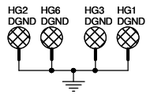
POWER (+5V) INPUT

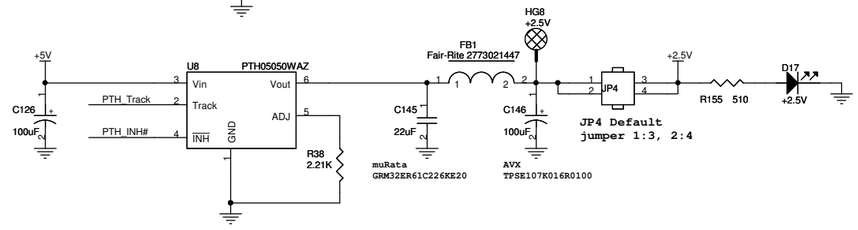


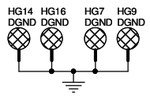


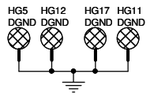


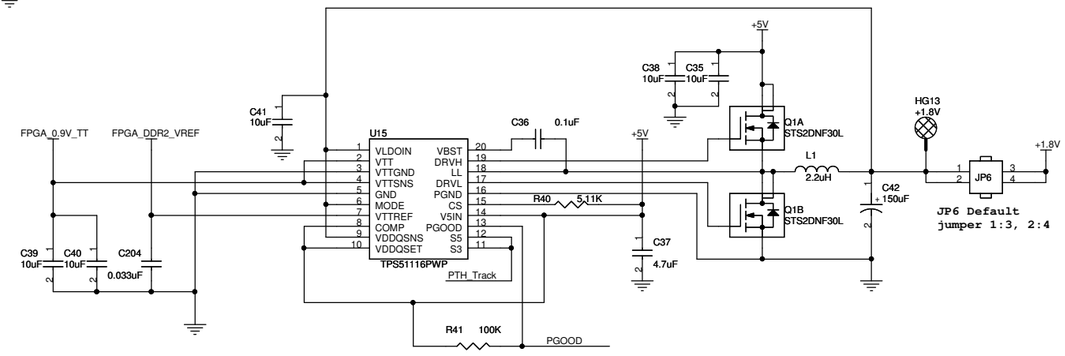












Avnet, Inc. *Engineering Services*		Copyright 2007
Title: Spartan-3A DSP Starter Board	Sheet 16 - Board Power	
Size: C	Document Number: 0381257	Rev: 1
Date: Friday, September 21, 2007	Sheet 16 of 17	

REV A	REV 1

ADDED POWER LEDS TO VCC_INT, +2.5V AND +3.3V RAILS
CONNECTED U20.3 TO PTH_INH# NET
ADDED A 2512 PKG LOAD RESISTOR TO +5V RAIL AT PWR JACK
ADDED PARALLEL TERMINATION TO SMA CLOCK INPUT
REMOVED LEVEL SHIFTER U14 & DIRECTLY CONNECTED SPI NETS TO U16
GROUNDED UNUSED I/O PINS ON TRANSCEIVERS U9, U17 & U18
CHANGED NAME OF PIN "V24" ON FPGA SYMBOL FROM "IP" TO "IO"

09/21/07: Updated Bank 2 of FPGA package by adding pin AA8 (IP_2) and changing pin AC22 from IP_2 (input only) to IO_2 (bidirectional)

Avnet, Inc. *Engineering Services*

Title: Spartan-3A DSP Starter Board — Sheet 17 - Revision History

Size: B | Document Number: 0381257 | Rev: 1

Date: Friday, September 21, 2007 | Sheet 17 of 17