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AXI4 Interconnect Paves the Way to Plug-and-Play IP

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In the past decade, the size and complexity of many FPGA designs exceeds the time and resources available to most design teams, making the use and reuse of Intellectual Property (IP) imperative. However, integrating numerous IP blocks acquired from both internal and external sources can be a daunting challenge that often extends, rather than shortens, design time. As today's designs integrate increasing amounts of functionality, it is vital that designers have access to proven, up-to-date IP from reliable sources.

Two key enablers, the creation of plug-and-play IP and the expansion of the ecosystem, have been significantly advanced with the release of the Advanced Microcontroller Bus Architecture (AMBA®4) AXI4 interconnect standard and its subsequent availability in Xilinx® ISE® Design Suite, version 12.3.

Benefits of a Common Interconnect Standard

The AXI4 specification represents a major evolutionary step in interconnect technology for on-chip system design. The AMBA 4 and AXI4 specifications, introduced in March, 2010, were designed by and for the industry, with contributions from 35 of the industry's leading OEM, EDA, and semiconductor vendors, including Xilinx. The result is an interconnect architecture suitable for FPGAs and ASICs.

The benefits to customers include:

- Increased productivity: The AXI4 specification eliminates the need for multiple legacy or custom interfaces to integrate IP from various sources. Because all IP shares a common interconnect, the designer can easily remove, add, or replace IP blocks within a design. When used in conjunction with IP repositories, security enhancements, and design tools, the AXI4 interconnect enables customers to realize the full value of plug-and-play FPGA design to achieve dramatic increases in productivity.
- Greater flexibility: The AXI4 specification accommodates a range of system requirements. It is inherently scalable, enabling system designers to optimize their designs for the highest possible F_{MAX}, maximum throughput, lower latency, smaller area, or some combination of those attributes. This flexibility enables customers to build the most compelling, optimized products for their markets.
- Greater IP availability: The AXI4 specification encourages and enables the Xilinx IP ecosystem and the ARM IP ecosystem to efficiently develop IP for use in Xilinx FPGAs and Extensible Processing Platforms. See www.xilinx.com/technology/roadmap/index.htm. As this occurs, Xilinx customers gain access to more IP from more sources, including IP created by experts in specific markets as well as sources for verification and test IP.

The AXI4 Interconnect

Released as part of the next-generation AMBA specification (AMBA 4), the AXI4 specification comprises three interconnect protocols that cover the variety of IP interconnect requirements encountered in FPGA and ASIC designs today:

- AXI4: A traditional single-address burst interconnect supporting up to 256 data beats per burst, the width of which is system dependent.
- AXI4-Lite: An area-efficient subset of the AXI4 protocol that only sends one data word per transaction.
- AXI4-Stream: A data-streaming interconnect that supports unidirectional, high-speed data transfers from master to slave with greatly reduced signaling. This interconnect efficiently accommodates the high-bandwidth streaming I/O requirements of multi-gigabit serial protocols and non-processor based IP, such as video and audio designs.

For more information about the AXI4 specification, see: www.xilinx.com/ipcenter/axi4.htm.

AXI4 Interconnect Creates Real Benefits in Real Designs

The AXI4 interconnect benefits (increased productivity, increased flexibility, and greater availability) are consistent across FPGA designs both with and without embedded processors. However, the ways in which these benefits combine and the measured impact of the AXI4 interconnect for these different types of designs are somewhat distinctive.

Processor-Based FPGA Designs

The demand for higher-performance electronic systems in every imaginable application has driven order-of-magnitude increases in I/O and memory speeds, and this trend is showing no signs of slowing down. System bandwidth must continue to scale to keep pace with performance advances in memory, I/O, and data volume. See Table 1.

Table 1: **Trend in Electronic Systems Requirements**

Requirement	Year 2000	Year 2010	Future
Memory	DDR2 - 266 Mb/s	DDR3 - 1,066 Mb/s	DDR3 - 2,133 Mb/s
Ethernet (Mb/s)	1 Gig E	10 GigE (XAUI)	40 Gig E
PCI/PCIe	66 MHz	5 Gb/s PCIe Gen2	8 Gb/s PCIe Gen 3
Video (Resolution)	VGA	1080p60	4K Displays

The most significant benefit the AXI4 interconnect brings to embedded processor designs is the ability to substantially increase performance.

The multi-port memory controller (MPMC) from Xilinx has played a critical role in the system performance of embedded FPGA designs. The MPMC manages the movement of data to and from the system's external memory and various peripherals at what was, heretofore, adequate performance levels (sufficient for the bandwidth requirements of Gigabit Ethernet, legacy video interfaces, etc.). The move to the AXI4 interconnect has created the opportunity to develop a new architecture that supports the higher bandwidth demanded by today's system interfaces and memories.

By leveraging the more efficient, higher-performance AXI4 interconnect block, AXI4 DMA IP, and memory controller, embedded designs see an increase anywhere from two to ten times the system bandwidth provided by the MPMC.

This means that FPGA-based embedded systems can support current as well as future high-performance DSP and connectivity requirements, including PCIe® Gen2 and Gen3, 10 to 40 Gigabit Ethernet, and high-definition video interfaces. Moreover, because of the scalable data bus width provided by the AXI4 interface specification, the performance of the AXI4 interconnect block and memory controller can continue to scale as needed. The Embedded Targeted Reference Design by Xilinx uses all three AXI4 interconnect protocols to accommodate a variety of interconnect requirements in the most efficient manner. See Figure 1.

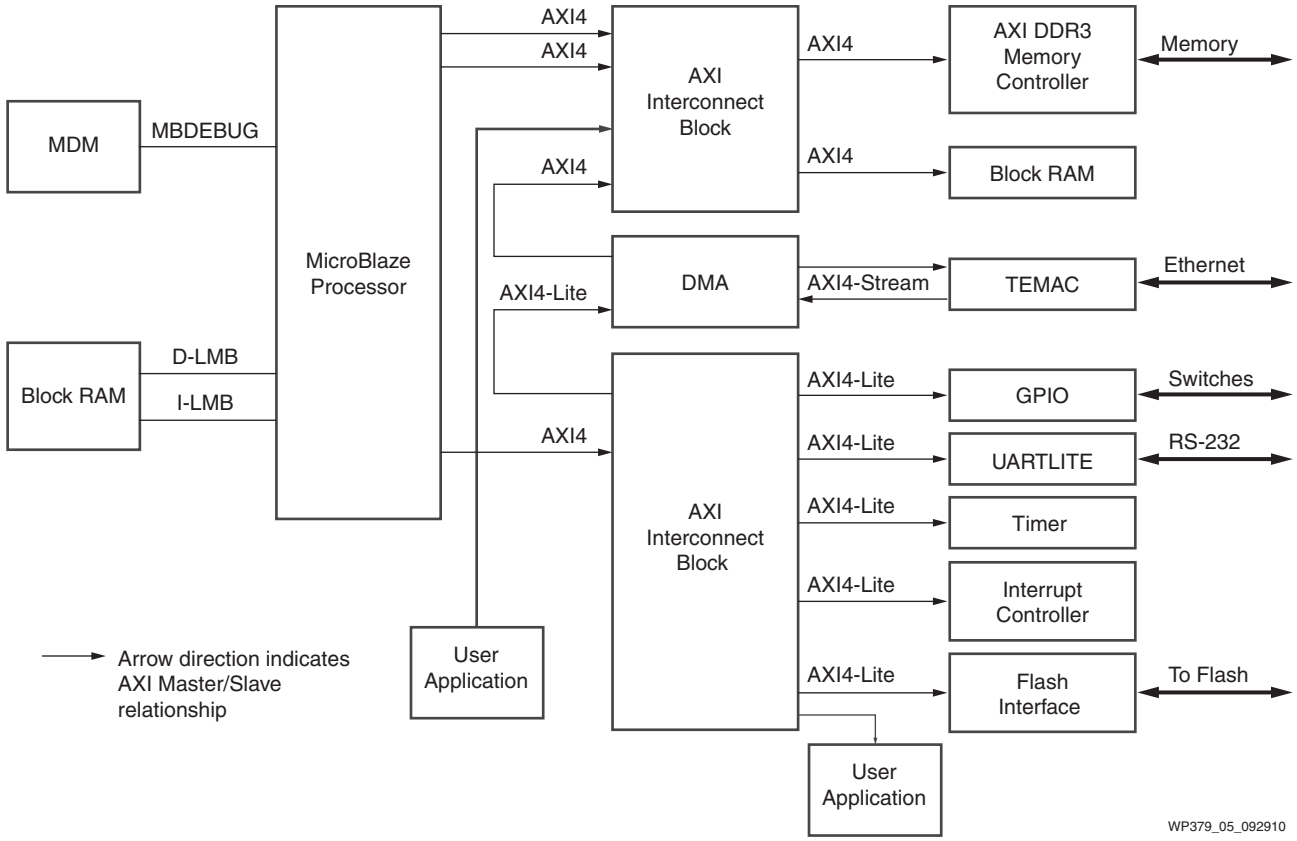

Figure 1: **Embedded Targeted Reference Design**

Using the new Embedded Targeted Reference Design, Xilinx conducted a benchmark study to demonstrate and validate the performance advantages afforded by the use of the AXI4 interconnect block and DMA as compared to the legacy MPMC/LocalLink DMA configuration. Part of the benchmark measures the burst Read/Write DMA performance, a key concern when streaming PCIe or Ethernet data to external memory or when performing high-speed data acquisition from multi-gigabit serial transceivers.(1)

Benchmark Results for Processor-Based Designs

The results of the AXI4 interconnect benchmark (Figure 2) demonstrated a 2X to 10X improvement in system bandwidth performance for embedded applications over MPMC/LocalLink DMA. These results are indicative of the significant advantages AXI4 interconnect affords. Systems using AXI4 interconnects run at higher clock frequencies than systems employing MPMC with traditional bus-based interconnect technologies. Also, AXI4 interconnects support data width up to 256 bits and higher, whereas the maximum data width for LocalLink is 32 bits.

1. The test setup used the ML605 board with a Virtex®-6 XC6VLX240T FPGA (highest speed grade) and employed a DDR3 64-bit interface running at 400 MHz. The burst length for the benchmark was 256 data beats.

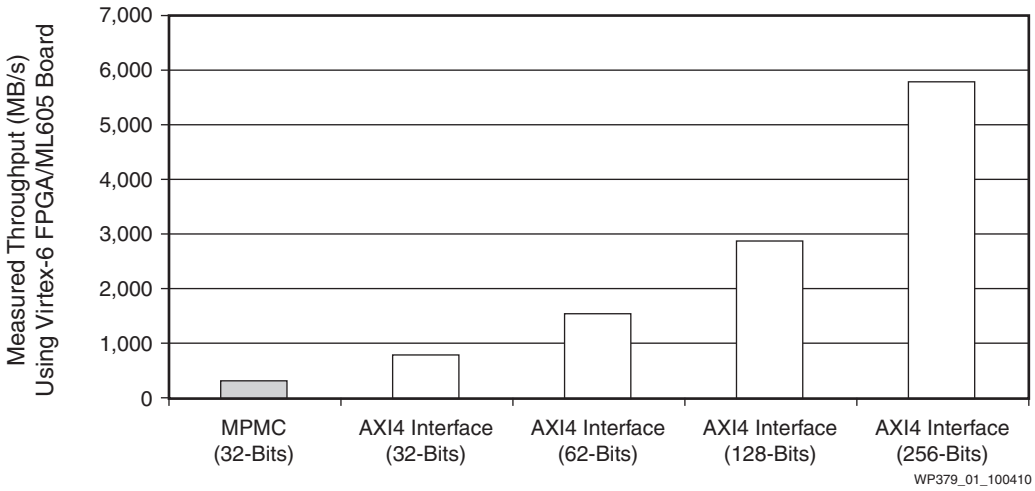

Figure 2: **AXI4 Interconnect versus MPMC/LocalLink System Bandwidth**

FPGA Designs without Embedded Processors

FPGAs have long been the device of choice for protocol bridging. In these designs, the key issues are latency, bandwidth, and sustainable (peak) data speeds. The Spartan-6 FPGA Connectivity Targeted Reference Design (see Figure 3) provides a design framework comprising IP blocks that have been upgraded to use the AXI4 interconnect: Ethernet, Memory Controller, and PCIe Packet DMA. In this configuration, the Targeted Reference Design provides a bridge between PCIe and Gigabit Ethernet. It uses AXI4-Stream interconnect to link the Xilinx PCI Express IP block to a PCIe Packet DMA IP block from Northwest Logic. (1)

1. Recognizing its value as a high-performance, burst-oriented interconnect architecture, Northwest Logic has adopted AXI4-Stream in their IP as the connection to the PCIe LogiCORE block. In this design, a small amount of custom logic serves as an adaptation layer between the PCIe Packet DMA IP block and Ethernet and memory controller blocks.

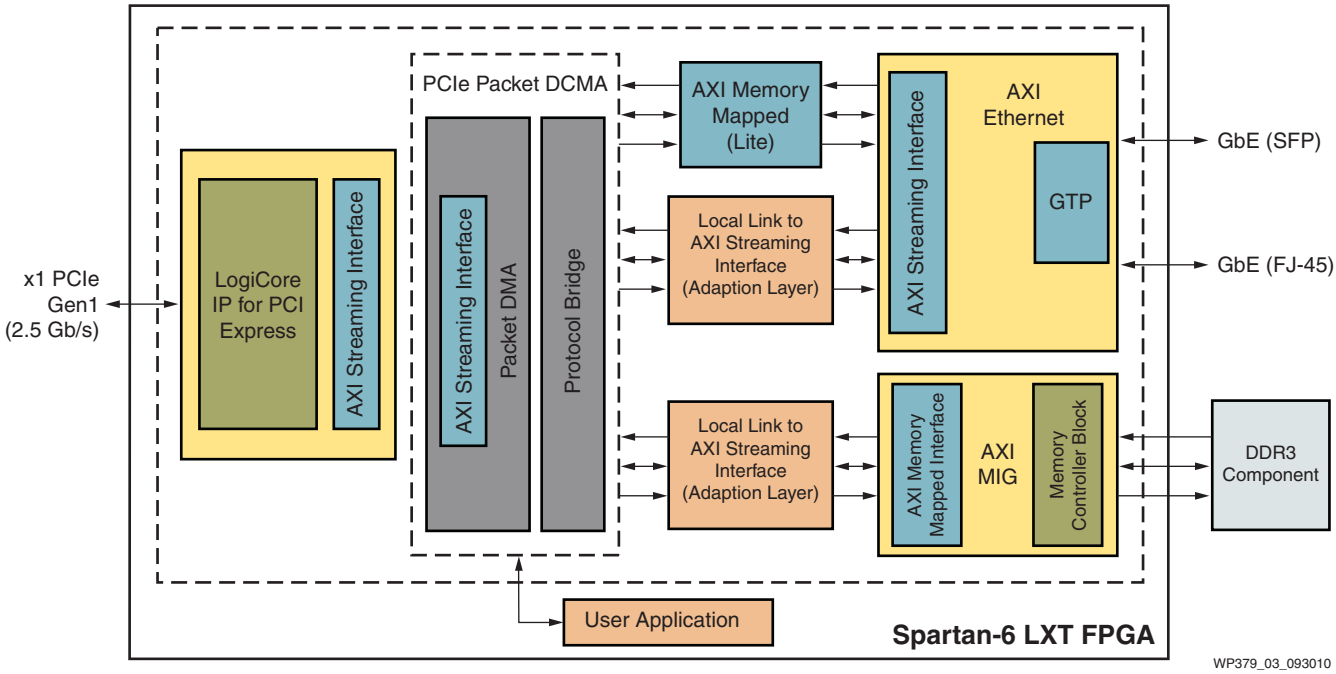

Figure 3: **Spartan-6 FPGA Connectivity Targeted Reference Design Using AXI4 Interconnect IP**

By leveraging the AXI4 interconnect standard to link the different IP blocks, this framework facilitates a true plug-and-play scenario in which the designer can accommodate alternative protocols by simply swapping another protocol IP block into the design (i.e., by replacing the Ethernet IP core with an Aurora high-speed serial chip-to-chip interface core).

The adoption of the AXI interconnect also significantly increases the number of plug-and-play IP blocks available to customers from a growing number of sources, including: the Xilinx IP portfolio, IP from members of the Xilinx alliance program, and AXI4-compliant IP suitable for use in FPGAs from the ARM Connected Community.

As performance requirements scale up to support higher bandwidth and peak efficiencies, the AXI4 interconnect also provides the ability to increase the data width (i.e., 32 bits, 64 bits, 128 bits, 256 bits) without changing the protocol controls.

One fundamental design challenge common to most high-performance connectivity systems is creating a memory interface that keeps pace with the highest performance protocol in the system. Memory bandwidth in complex systems is often oversubscribed by 2X or more, making arbitration an essential part of the memory controller function.

The Virtex-6 FPGA Connectivity Targeted Reference Design (Figure 4) uses a custom-designed 40 Gb/s memory controller optimized to a 50 Gb/s memory architecture. Using the AXI4 interconnect Memory Interface Generator (MIG), designers can create and/or modify the design of an AXI4 interconnect block, which provides the protocol translation, arbitration, and memory management functions.

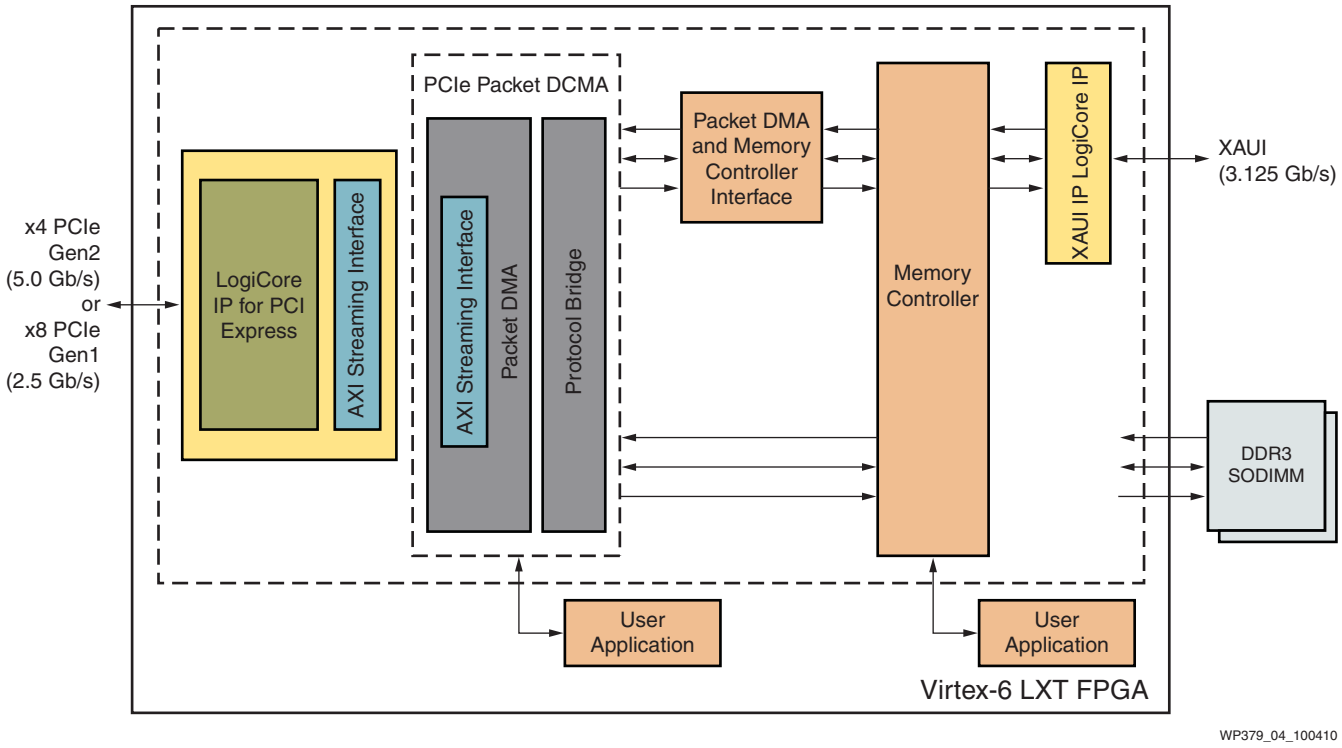

Figure 4: **Virtex-6 FPGA Connectivity Targeted Reference Design Using AXI4 Interconnect**

Complexity is a constant in DSP designs, so the ability to create AXI4-compliant blocks that plug and play with other system-level IP blocks reduces the plethora of interfaces commonly found in a DSP system to a single standard interconnect—saving hours of design time. Once mastered, DSP hardware designers can apply this knowledge to integrate system components such as memory controllers, analog interfaces, embedded systems, and IP. This enables DSP hardware designers, who often have varied FPGA design experience, to focus on value add hardware design of their algorithms. See Figure 5.

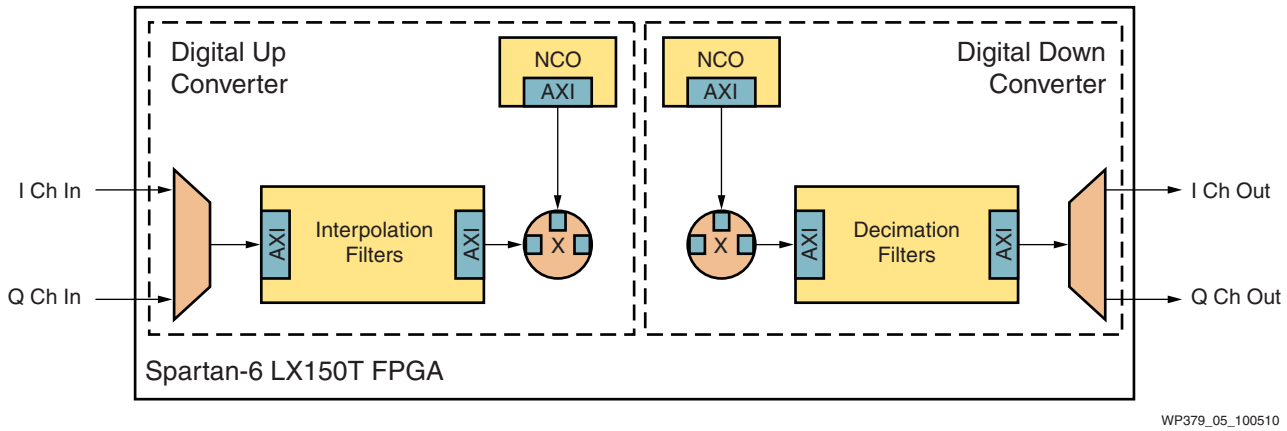

Figure 5: **Spartan-6 FPGA DSP Targeted Reference Design**

The Spartan-6 FPGA DSP targeted reference design is a digital up converter (DUC)/digital down converter (DDC) that includes interpolation filters, decimation filters, and a numerically controlled oscillator that generates a sine and cosine signal used for complex mixing. This design demonstrates the use of the AXI4-Stream

interconnect to both synchronize the internal dataflow through the DSP processing datapath as well as exist at the top-level of the DSP block.

The DSP design community has been quick to embrace high-level design methodologies that use modeling languages such as C/C++ and MATLAB®/Simulink® to generate DSP hardware blocks. These design flows deliver excellent results and are well suited for the algorithmic and highly datapath-oriented designs that typify DSP applications. The AXI4 interconnect structure provides a framework that enables these high-level design tools to more easily leverage existing design infrastructure provided through reference designs from Xilinx and third-party suppliers. The tools can automatically insert AXI4 interconnects onto the DSP blocks they generate, making the task of integrating with these reference designs predictable, familiar, and straightforward. High-level design tools, such as System Generator for DSP, support the creation and generation of DSP blocks from Simulink. These DSP blocks include both the AXI4 interconnect and the AXI4-Stream interconnect to achieve maximum performance and throughput as well as increased ease-of-use.

Benchmark Results for FPGA Designs without Processors

For high-performance designs without processors, it is key to have a low overhead interface that enables easy IP integration while enabling maximum performance. In these systems, memory performance is often the critical bottleneck. These designs until now have implemented memory interfaces using a Xilinx MIG Native Interface to maximize bandwidth. Designers typically have had to extend the design to include additional modules like multi-ports, arbitration logic, etc.

Benchmarked performance of a MIG native interface against an AXI4 interconnect based system (see Figure 6) shows that the throughput of AXI4 interconnect is comparable to MIG Native interface and enable near maximum throughput on the Virtex-6 FPGA ML605 platform when accessing memory through a DDR3 interface.

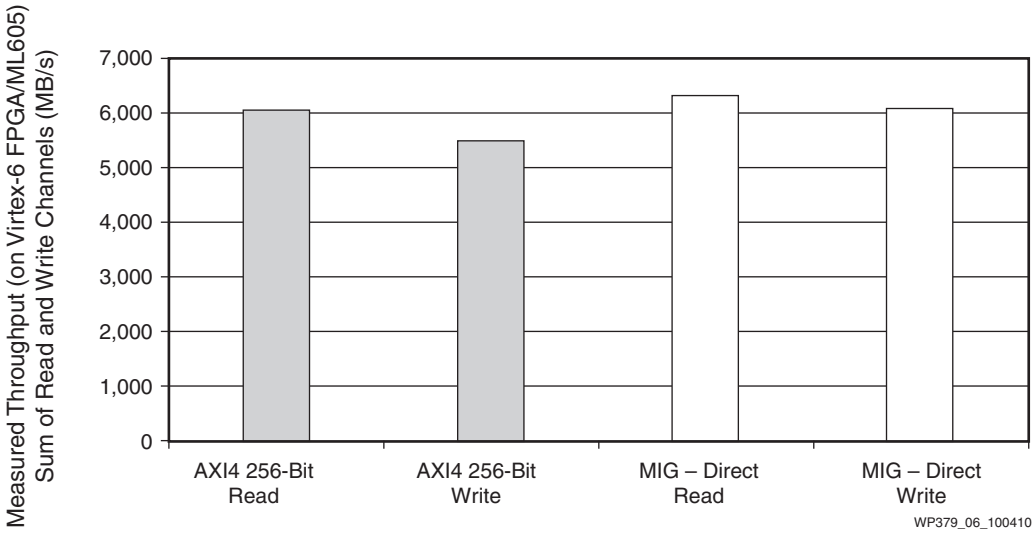

Figure 6: **Comparable Performance for Non-Embedded Applications Using an AXI4 Interconnect**

In addition to providing equivalent performance, the AXI4 interconnect offers additional advantages for non-embedded applications. The AXI4 interconnect

includes a cross-bar switch and supports multiple ports and multiple standard AXI4 interconnects-all unsupported by MIG Native interfaces (see Table 2).

Table 2: **Comparison of Functionality and Performance Using MIG (Native) Interface and the AXI4 Interconnect**

Design Criteria: Functionality and Performance	MIG (Native) Interface	AXI4 Interconnect
High-performance memory interface	✓	✓
Support for multiple ports with different clock domains		✓
Full cross-bar switch (arbitration)		✓
Support for industry-standard interface		✓

Conclusion

The value of the AXI4 interconnect has many facets, beginning with an immediate gain in productivity derived from a unified IP interconnect standard that supplants legacy and custom interconnect architectures. The three interconnect protocols developed for the AXI4 standard (AXI4, AXI4-Lite, and AXI4-Stream interfaces) provide the flexibility to optimize an FPGA design for performance, throughput, latency, or area. The long-term value of AXI4 interconnect is the impact that the creation of plug-and-play IP will have on the expansion and evolution of the IP ecosystem for Xilinx embedded, connectivity, and DSP FPGA designs.

References

The primary sources of information regarding the AXI4 IP interconnect standard include:

- AXI4 Landing Page:
  www.xilinx.com/ipcenter/axi4.htm

  This site includes the AXI4 Reference Guide that provides a comprehensive view of the use of AXI4 in Xilinx FPGA designs.
- The AMBA 4 specifications, including AXI4, AXI4-Lite, and AXI4-Stream:
  http://www.arm.com/products/system-ip/amba/amba-open-specifications.php

For more information, contact your local Xilinx sales representative or distributor.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/05/10	1.0	Initial Xilinx release.

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