Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VFX20CES2/3 and XC4VFX60CES2/3 devices. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VFX20CES2/3 and XC4VFX60CES2/3 devices as shown in Table 1.

Table 1: XC4VFX20 and XC4VFX60 Devices Affected by These Errata

<table>
<thead>
<tr>
<th>Devices</th>
<th>XC4VFX20CES2</th>
<th>XC4VFX20CES3</th>
<th>XC4VFX60CES2</th>
<th>XC4VFX60CES3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XC4VFX20CES3L</td>
<td>XC4VFX60CES2L2(1)</td>
<td>XC4VFX60CES3L</td>
<td></td>
</tr>
<tr>
<td></td>
<td>XC4VFX20CES3R</td>
<td>XC4VFX60CES2R2(1)</td>
<td>XC4VFX60CES3R</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XC4VFX60CES2V2(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XC4VFX60CES3L2(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XC4VFX60CES3R2(1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XC4VFX60CES3V2(1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

JTAG ID (Revision Code) for all devices(2): 0h, Bh, Dh, or Fh

Packages: All

Speed Grades: -10, -11, -12

Notes:
1. CES3L2, CES3R2, and CES3V2 devices require a different Calibration Block version. Refer to the Calibration Block section in this document.

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST_EMPTY_OFFSET or ALMOST_FULL_OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (down-loadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

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DSP48

**CarryIn Input Register**

The CarryIn input register from fabric is not supported (that is, the attribute CARRYINREG = 1).

**Workaround**

Use CLB register to replace CarryIn Input Register, and set attribute CARRYINREG = 0.

**Symmetric Rounding Logic**

The DSP48 element supports five different modes of symmetric rounding. All four non-pipelined rounding modes are fully supported. Only the pipelined Round (A x B) mode (that is, when CarryInSel[1:0] = 11) is not supported.

**Workaround**

Perform the equivalent logic for carry in a CLB, and connect the carry to the CarryIn input of the DSP48 slice using CarryInSel[1:0] = 00 (set attribute CARRYINREG = 0)

**DCM**

1. The DCM attribute CLKOUT_PHASE_SHIFT set to the value VARIABLE_CENTER is not supported.
2. If the only clock outputs used from a DCM are CLKFX and/or CLKFX180, and the input clock frequency (CLKIN) is outside of the CLKIN_FREQ_DLL_(HF or LF)_(MS or MR)_MIN/MAX range, then use the macro in answer record 20529 to properly generate the LOCKED signal.
3. For source-synchronous applications, it is best to use the ChipSync™ features for the highest performance and lowest skew. If the DCM must be used, follow the guidelines outlined in answer record 20529 to achieve a CLKIN_CLKFB_PHASE specification of ±300 ps.

**TCONFIG, DCM_INPUT_CLOCK_STOP, and DCM_RESET Requirements**

The following time requirements detailed in the Virtex-4 data sheet apply to the devices listed in this errata:

- TCONFIG – the time to configure devices after VCCINT is applied.
- DCM_INPUT_CLOCK_STOP – the maximum duration of time where CLKIN and CLKFB can be stopped.
- DCM_RESET – the maximum time to reset the DCM.

**Workaround**

Use design solution in answer record 21127.

**FRAME_ECC**

FRAME_ECC readback of unused configuration bits in I/O IDELAY frames might indicate readback errors. These are false errors and can be ignored because they have no functional impact.

**Workaround**

The reference design described in XAPP714 can be used to eliminate this error indication.

**Processor Block**

**Frequency Performance**

1) The PPC405 processor core maximum operating frequency is 300 MHz for -10 speed grade and 350 MHz for -11 speed grade.

**Workaround**

Compile code with the Xilinx provided Gnu compiler to achieve full frequency (350 MHz for -10 speed grade; 400 MHz -11 speed grade). For details, see answer record 21075.

2) When using the APU controller interface, the maximum operating frequency of the processor block is 275 MHz for -10 speed grade and 300 MHz for -11 speed grade.

For other processor block errata and operational guidelines, please refer to answer record 20658.
RocketIO™ Multi-Gigabit Serial Transceivers

This section provides a detailed description of the Virtex-4 RocketIO™ transceiver issues known at the release time of this document.

**Unavailable Pins On CES2 Devices**

The RocketIO serial transceiver pins listed in Table 2 are not available. All other RocketIO transceiver pins are available for use. This specific table does not apply to CES3 devices.

<table>
<thead>
<tr>
<th>Device - Package</th>
<th>MGT Name</th>
<th>Software Location</th>
<th>Pin Name</th>
<th>Pin Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC4VFX20CES2 – FF672</td>
<td>MGT110A</td>
<td>GT11_X1Y1</td>
<td>RXPPADA_110</td>
<td>AC1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RXNPPADA_110</td>
<td>AD1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TXPPADA_110</td>
<td>AF2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TXNPPADA_110</td>
<td>AF3</td>
</tr>
<tr>
<td>XC4VFX60CES2 – FF672</td>
<td>MGT110A</td>
<td>GT11_X1Y3</td>
<td>RXPPADA_110</td>
<td>AC1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RXNPPADA_110</td>
<td>AD1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TXPPADA_110</td>
<td>AF1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TXNPPADA_110</td>
<td>AG1</td>
</tr>
</tbody>
</table>

**Available Transceivers on the Left or Right Side**

Some Virtex-4 devices are available with reduced transceiver counts. RocketIO serial transceivers are available on either the left or the right side of the die. The device order numbers have an L or an R after the CES designation to indicate the left or right side of the die. When viewed from the top of a flip-chip packaged device, the MGTs and their pin locations are reversed. In other words, the left-side MGT on the die is a right-side MGT when viewed from top of the package. Table 3 shows the available left or right side transceivers for the FF672 package devices. Table 4 shows the available left or right side transceivers for the FF1152 package devices.
### Available Left or Right Side Transceivers -FF672 Package

<table>
<thead>
<tr>
<th>MGT Name</th>
<th>Software Location</th>
<th>Pin Name</th>
<th>Pin Location</th>
<th>Software Location</th>
<th>Pin Name</th>
<th>Pin Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>102_A</td>
<td>GT11_X0Y3</td>
<td>RXPPADA_102</td>
<td>A19</td>
<td>GT11_X0Y7</td>
<td>RXPPADA_102</td>
<td>A19</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_102</td>
<td>A20</td>
<td></td>
<td>RXNPADA_102</td>
<td>A20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_102</td>
<td>A22</td>
<td></td>
<td>TXPPADA_102</td>
<td>A22</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_102</td>
<td>A23</td>
<td></td>
<td>TXNPADA_102</td>
<td>A23</td>
</tr>
<tr>
<td>102_B</td>
<td>GT11_X0Y2</td>
<td>RXPPADB_102</td>
<td>C26</td>
<td>GT11_X0Y6</td>
<td>RXPPADB_102</td>
<td>C26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_102</td>
<td>D26</td>
<td></td>
<td>RXNPADB_102</td>
<td>D26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_102</td>
<td>A24</td>
<td></td>
<td>TXPPADB_102</td>
<td>A24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_102</td>
<td>A25</td>
<td></td>
<td>TXNPADB_102</td>
<td>A25</td>
</tr>
<tr>
<td>103_A</td>
<td>GT11_X0Y5</td>
<td>RXPPADA_103</td>
<td>J26</td>
<td></td>
<td>RXPPADA_103</td>
<td>J26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_103</td>
<td>K26</td>
<td></td>
<td>RXNPADA_103</td>
<td>K26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_103</td>
<td>M26</td>
<td></td>
<td>TXPPADA_103</td>
<td>M26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_103</td>
<td>N26</td>
<td></td>
<td>TXNPADA_103</td>
<td>N26</td>
</tr>
<tr>
<td>103_B</td>
<td>GT11_X0Y4</td>
<td>RXPPADB_103</td>
<td>U26</td>
<td></td>
<td>RXPPADB_103</td>
<td>U26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_103</td>
<td>V26</td>
<td></td>
<td>RXNPADB_103</td>
<td>V26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_103</td>
<td>P26</td>
<td></td>
<td>TXPPADB_103</td>
<td>P26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_103</td>
<td>R26</td>
<td></td>
<td>TXNPADB_103</td>
<td>R26</td>
</tr>
<tr>
<td>105_A</td>
<td>GT11_X0Y1</td>
<td>RXPPADA_105</td>
<td>W26</td>
<td>GT11_X0Y3</td>
<td>RXPPADA_105</td>
<td>W26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_105</td>
<td>Y26</td>
<td></td>
<td>RXNPADA_105</td>
<td>Y26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_105</td>
<td>AB26</td>
<td></td>
<td>TXPPADA_105</td>
<td>AB26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_105</td>
<td>AC26</td>
<td></td>
<td>TXNPADA_105</td>
<td>AC26</td>
</tr>
<tr>
<td>105_B</td>
<td>GT11_X0Y0</td>
<td>RXPPADB_105</td>
<td>AF24</td>
<td>GT11_X0Y2</td>
<td>RXPPADB_105</td>
<td>AF24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_105</td>
<td>AF23</td>
<td></td>
<td>RXNPADB_105</td>
<td>AF23</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_105</td>
<td>AD26</td>
<td></td>
<td>TXPPADB_105</td>
<td>AD26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_105</td>
<td>AE26</td>
<td></td>
<td>TXNPADB_105</td>
<td>AE26</td>
</tr>
<tr>
<td>106_A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>106_B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 3: Available Left or Right Side Transceivers -FF672 Package (Continued)

<table>
<thead>
<tr>
<th>MGT Name</th>
<th>Xilinx 4VFX20 FF672</th>
<th>Xilinx 4VFX60 FF672</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Software Location</td>
<td>Pin Name</td>
</tr>
<tr>
<td>113_A</td>
<td>GT11_X1Y3</td>
<td>RXPPADA_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_113</td>
</tr>
<tr>
<td>113_B</td>
<td>GT11_X1Y2</td>
<td>RXPPADDB_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADDB_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADDB_113</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADDB_113</td>
</tr>
<tr>
<td>112_A</td>
<td>GT11_X1Y5</td>
<td>RXPPADA_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_112</td>
</tr>
<tr>
<td>112_B</td>
<td>GT11_X1Y4</td>
<td>RXPPADDB_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADDB_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADDB_112</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADDB_112</td>
</tr>
<tr>
<td>110_A</td>
<td>GT11_X1Y1 (1)</td>
<td>RXPPADA_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_110</td>
</tr>
<tr>
<td>110_B</td>
<td>GT11_X1Y0</td>
<td>RXPPADDB_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADDB_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADDB_110</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADDB_110</td>
</tr>
<tr>
<td>109_A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>109_B</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. This location is not supported in Xilinx 4VFX20 and Xilinx 4VFX60 CES2R devices.
Table 4: Available Left or Right Side Transceivers -FF1152 Package

<table>
<thead>
<tr>
<th>MGT Name</th>
<th>Software Location</th>
<th>Pin Name</th>
<th>Pin Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>102_A</td>
<td>GT11_X0Y7</td>
<td>RXPPADA_102</td>
<td>A31</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_102</td>
<td>A32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_102</td>
<td>D34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_102</td>
<td>E34</td>
</tr>
<tr>
<td>102_B</td>
<td>GT11_X0Y6</td>
<td>RXPPADB_102</td>
<td>J34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_102</td>
<td>K34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_102</td>
<td>F34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_102</td>
<td>G34</td>
</tr>
<tr>
<td>103_A</td>
<td>GT11_X0Y5</td>
<td>RXPPADA_103</td>
<td>R34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_103</td>
<td>T34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_103</td>
<td>V34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_103</td>
<td>W34</td>
</tr>
<tr>
<td>103_B</td>
<td>GT11_X0Y4</td>
<td>RXPPADB_103</td>
<td>AC34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_103</td>
<td>AD34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_103</td>
<td>Y34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_103</td>
<td>AA34</td>
</tr>
<tr>
<td>105_A</td>
<td>GT11_X0Y3</td>
<td>RXPPADA_105</td>
<td>AF34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_105</td>
<td>AG34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_105</td>
<td>AJ34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_105</td>
<td>AK34</td>
</tr>
<tr>
<td>105_B</td>
<td>GT11_X0Y2</td>
<td>RXPPADB_105</td>
<td>AP32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_105</td>
<td>AP31</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_105</td>
<td>AL34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_105</td>
<td>AM34</td>
</tr>
<tr>
<td>106_A</td>
<td>GT11_X0Y1</td>
<td>RXPPADA_106</td>
<td>AP26</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_106</td>
<td>AP25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_106</td>
<td>AP23</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADA_106</td>
<td>AP22</td>
</tr>
<tr>
<td>106_B</td>
<td>GT11_X0Y0</td>
<td>RXPPADB_106</td>
<td>AP18</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_106</td>
<td>AP17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_106</td>
<td>AP21</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPADB_106</td>
<td>AP20</td>
</tr>
</tbody>
</table>
### Right-side MGTs:
- XC4VFX60CES2R2
- XC4VFX60CES3R
- XC4VFX60CES3R2

<table>
<thead>
<tr>
<th>MGT Name</th>
<th>Software Location</th>
<th>Pin Name</th>
<th>Pin Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>113_A</td>
<td>GT11_X1Y7</td>
<td>RXPPADA_113</td>
<td>A7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_113</td>
<td>A6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_113</td>
<td>A4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_113</td>
<td>A3</td>
</tr>
<tr>
<td>113_B</td>
<td>GT11_X1Y6</td>
<td>RXPPADB_113</td>
<td>F1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_113</td>
<td>G1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_113</td>
<td>C1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_113</td>
<td>D1</td>
</tr>
<tr>
<td>112_A</td>
<td>GT11_X1Y5</td>
<td>RXPPADA_112</td>
<td>M1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_112</td>
<td>N1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_112</td>
<td>R1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_112</td>
<td>T1</td>
</tr>
<tr>
<td>112_B</td>
<td>GT11_X1Y4</td>
<td>RXPPADB_112</td>
<td>Y1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_112</td>
<td>AA1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_112</td>
<td>U1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_112</td>
<td>V1</td>
</tr>
<tr>
<td>110_A</td>
<td>GT11_X1Y3 (1)</td>
<td>RXPPADA_110</td>
<td>AC1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_110</td>
<td>AD1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_110</td>
<td>AF1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_110</td>
<td>AG1</td>
</tr>
<tr>
<td>110_B</td>
<td>GT11_X1Y2</td>
<td>RXPPADB_110</td>
<td>AL1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_110</td>
<td>AM1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_110</td>
<td>AH1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_110</td>
<td>AJ1</td>
</tr>
<tr>
<td>109_A</td>
<td>GT11_X1Y1</td>
<td>RXPPADA_109</td>
<td>AP6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADA_109</td>
<td>AP7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADA_109</td>
<td>AP9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_109</td>
<td>AP10</td>
</tr>
<tr>
<td>109_B</td>
<td>GT11_X1Y0</td>
<td>RXPPADB_109</td>
<td>AP14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RXNPADB_109</td>
<td>AP15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXPPADB_109</td>
<td>AP11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TXNPA_D_109</td>
<td>AP12</td>
</tr>
</tbody>
</table>

#### Notes:
1. This location is not supported in XC4VFX60 CES2R devices.
**Analog Voltage Supply Values**

AVCCAUXTX must be set to 1.1V ± 3%.

AVCCAUXRX (both A and B) must be set to 1.1V ± 3%.

For additional information on recommended regulators, see Xilinx answer record 21739.

**Analog Receiver Range**

The receiver is tested at 622 Mb/s and 1.25 Gb/s using the digital CDR mode, and at 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s using the analog CDR mode. Operation above 3.125 Gb/s is not supported in the devices covered by this errata (Table 1).

**8B/10B Encoding**

Data transmitted/received with the devices covered by this errata (Table 1) must be 8B/10B encoded when using the analog CDR mode for 1.25 Gb/s, 2.5 Gb/s, and 3.125 Gb/s rates.

**Total Jitter Generation**

At MGTCCLK frequencies of 156 MHz and below, the transceivers can exhibit total wide-band jitter generation greater than 0.35UI.

**Calibration Block**

A programmable Calibration block, written in Verilog and VHDL, is available from Xilinx. This block must be used with these devices. See answer record 22477 for details on obtaining this block.

**Attributes**

Certain attribute settings need to be changed from the ISE software 7.1i SP4 default settings. See Xilinx answer record 21672 for the most up to date attribute setting details.

**Temperature Range**

The devices covered by this errata (Table 1) are certified for use at 25°C junction to 85°C junction temperature. Junction temperatures below 25°C are not supported.

**32-Bit Comma Detection (SONET Alignment)**

Receive data alignment is not maintained when the ENPCOMMAALIGN fabric port is deasserted (pulled Low) while operating with the 32-bit SONET aligner enabled. SONET alignment (A1A1A2A2) is enabled by setting the attribute COMMA32 = TRUE. This errata does not affect the normal byte alignment block. This block does maintain alignment on deassertion of ENPCOMMAALIGN.

**Internal Clock Divider Restriction**

TXUSRCLK must be sourced from the fabric for 1-byte and 2-byte interface modes on both MGTA and MGTB. Although the internal clock divider (divide by 2 or 4) can be used to internally generate TXUSRCLK, the TXUSRCLK2 divider cannot be used in the transmitter of MGTA or MGTB for 1-byte and 2-byte interface modes.

**8B/10B Encoder TXKERR Port**

The TXKERR output port incorrectly indicates the correctness of K-characters on the transmit data bus. It indicates invalid K-characters as valid and valid K-characters as invalid. The output of this port should be ignored.

**Static Operating Behavior**

Under certain and specific conditions, transceivers might cease to correctly transmit or receive data when all three of the following conditions are met:

1. Power has been applied to the FPGA.
2. Transitions are not occurring in the transmit and/or the receive direction.
3. Conditions (1) and (2) persist for more than 400 cumulative hours at 85°C Tj or more than 2,000 cumulative hours at 60°C Tj.

To view detailed information on this topic, see Xilinx answer record 22471.
Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact the Xilinx technical support for SP4 support. Updates are available on the following web page:
  
  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

  The Stepping should be set to ES in the constraint file (UCF file):

  CONFIG STEPPING = “ES”;

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:
  
  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

Examples of package markings for the devices listed in Table 1 appear in Figure 1 and Figure 2.

Figure 1: Example XC4VFX60CES2 Package Marking
Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support:
http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative:
http://www.xilinx.com/company/contact.htm.

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If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at:

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)
Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04/25/05</td>
<td>1.0</td>
<td>Initial release.</td>
</tr>
<tr>
<td>06/23/05</td>
<td>1.1</td>
<td>Revised designation of devices from CES to CES2. Change the Design Software Requirements to ISE7.1i (SP3). Corrected the RocketIO software table to GT11. Added FRAME_ECC errata information.</td>
</tr>
<tr>
<td>07/06/05</td>
<td>1.2</td>
<td>Added a new section, Analog Voltage Supply Values, and made text changes.</td>
</tr>
<tr>
<td>08/22/05</td>
<td>1.3</td>
<td>Revised information under the Analog Receiver Range heading, added the 8B/10B Encoding and Temperature Range sections, and removed the PCS HCLKOUT Output section. Updated the Design Software Requirements to require speed specification 1.57 and ISE7.1i (SP4) software.</td>
</tr>
<tr>
<td>10/11/05</td>
<td>1.4</td>
<td>Added CES3 device functionality. Revised Analog Receiver Range and 8B/10B Encoding sections. Added Internal Clock Divider Restriction and 32-Bit Comma Detection (SONET Alignment) errata.</td>
</tr>
</tbody>
</table>
| 04/05/06   | 1.5     | • Updated Table 1, Table 3, and Table 4.  
• Added the FIFO16 errata.  
• Replaced the LVTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations section.  
• Removed System Monitor errata because it is no longer in the Virtex-4 data sheet. Added Available Transceivers on the Left or Right Side section.  
• Added TCONFG, DCM_INPUT_CLOCK_STOP, and DCM_RESET Requirements, Static Operating Behavior, and 8B/10B Encoder TXKERR Port sections.  
• Updated the Analog Voltage Supply Values and the Attributes sections. |
| 10/24/07   | 1.6     | Updated JTAG information in Table 1 and added Note 2. Updated copyright and legal disclaimer. |

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