Introduction

This document provides the design specification for the Microprocessor Debug Module (MDM), which enables JTAG-based debugging of one or more MicroBlaze™ processors and/or PowerPC™ 405 processors.

Features

The most significant features of the MDM are:

- Support for JTAG-based software debug tools
- Support for debugging a configurable number of MicroBlaze/PowerPC 405 processors
- Support for synchronized control of multiple processors - stop and single step
- Support for a JTAG based UART with an OPB interface
- Based on BSCAN logic in Xilinx FPGAs
- Supports connection to Chipscope™ ICON core through unused BSCAN signals
- Support of one master FSL port for fast download

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Spartan-3E, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	opb_mdm	v2.00a
Resources Used		
	Min	Max
Slices	67	188
LUTs	45	292
FFs	79	204
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 6.2i or higher	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The Microprocessor Debug Module (MDM) enables JTAG-based debugging of one or more MicroBlaze processors and/or PowerPC 405 processors. The block diagram of the module is shown in Figure 1.
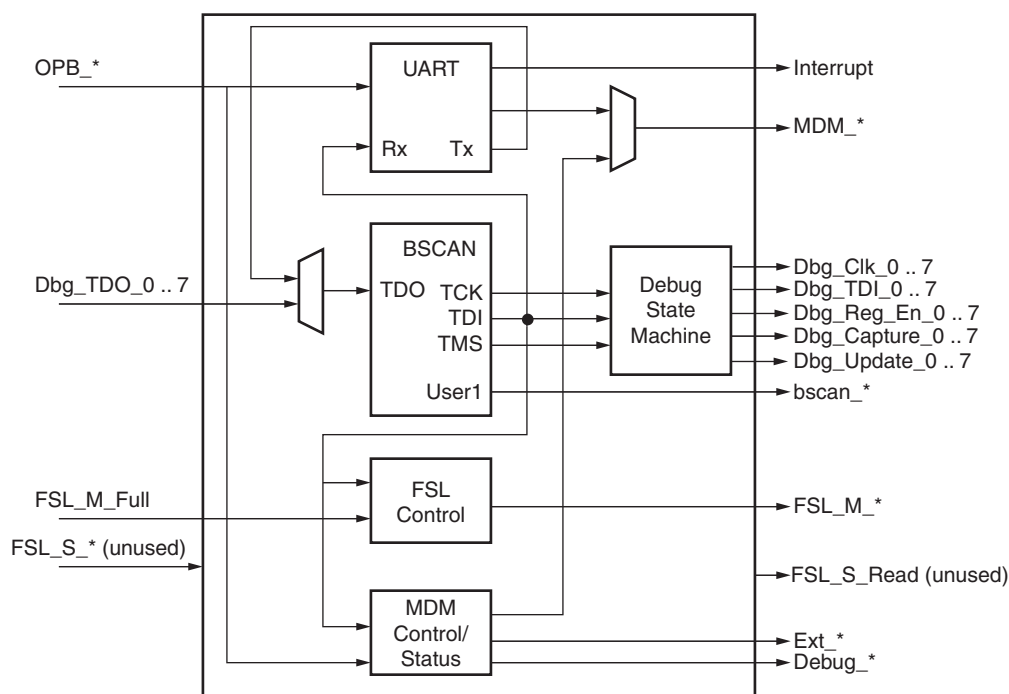

Figure 1: **Microprocessor Debug Module (MDM) Block Diagram**

OPB MDM I/O Signals

The I/O signals for the Microprocessor Debug Module (MDM) are listed and described in Table 1.

Table 1: **OPB_MDM I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
OPB_Clk	OPB	I		OPB clock for UART interface
OPB_Rst	OPB	I		OPB Reset for UART interface
Interrupt	Interrupt	O	0	Interrupt output from UART interface
Debug_SYS_Rst	Reset	O	0	Reset output to Microprocessor and OPB bus
Debug_Rst	Reset	O	0	Reset output to Microprocessor
Ext_BRK	Break	O	0	External Break signal to Microprocessor
Ext_NM_BRK	Break	O	0	Non-Maskable External Break signal
OPB_ABus[0:31]	OPB	I		OPB Address Bus
OPB_BE[4]	OPB	I		OPB Byte Enable
OPB_RNW	OPB	I		OPB Read Not Write

Table 1: **OPB_MDM I/O Signals** *(Contd)*

Signal Name	Interface	I/O	Initial State	Description
OPB_select	OPB	I		OPB Select
OPB_seqAddr	OPB	I		OPB Sequential Address
OPB_DBus[0:31]	OPB	I		OPB Data Bus
MDM_DBus	OPB	O	0	MDM (slave) Data Bus
MDM_errAck	OPB	O	0	MDM (slave) Error Ack
MDM_retry	OPB	O	0	MDM (slave) Retry
MDM_toutSup	OPB	O	0	MDM (slave) Timeout Suppress
MDM_xferAck	OPB	O	0	MDM (slave) Transfer Acknowledge
Dbg_Clk_0 .. 7	Debug 0..7	O	0	MDM-Microprocessor debug clock
Dbg_TDI_0 .. 7	Debug 0..7	O	0	MDM-Microprocessor debug TDI
Dbg_TDO_0 .. 7	Debug 0..7	I		Microprocessor-MDM debug TDO
Dbg_Reg_En_0 .. 7 [0:4]	Debug 0..7	O	0	MDM-Microprocessor debug register enable
Dbg_Capture_0 .. 7	Debug 0..7	O	0	MDM-Microprocessor debug Capture
Dbg_Update_0 .. 7	Debug 0..7	O	0	MDM-Microprocessor debug Update
FSL0_M_Clk	FSL	O	0	Master FSL port clock
FSL0_M_Write	FSL	O	0	Master FSL port write signal
FSL0_M_Data[0:31]	FSL	O	0	Master FSL port data signals
FSL0_M_Control	FSL	O	0	Master FSL port control signal
FSL0_M_Full	FSL	I		Master FSL port full signal
FSL0_S_Clk	FSL	O	0	Read FSL port clock (not used)
FSL0_S_Read	FSL	O	0	Read FSL port write signal (not used)
FSL0_S_Data[0:31]	FSL	I		Read FSL port data signals (not used)
FSL0_S_Control	FSL	I		Read FSL port control signal (not used)
FSL0_S_Exists	FSL	I		Read FSL port full signal (not used)
bscan_tdi	ICON	O	0	Connection to Chipscope ICON core
bscan_reset	ICON	O	0	Connection to Chipscope ICON core
bscan_shift	ICON	O	0	Connection to Chipscope ICON core
bscan_update	ICON	O	0	Connection to Chipscope ICON core
bscan_capture	ICON	O	0	Connection to Chipscope ICON core
bscan_sel1	ICON	O	0	Connection to Chipscope ICON core
bscan_drck1	ICON	O	0	Connection to Chipscope ICON core
bscan_tdo1	ICON	I		Connection to Chipscope ICON core

MDM Design Parameters

Table 2 lists and describes the features that can be parameterized in the Microprocessor Debug Module.

Table 2: **OPB_MDM Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	Tool Assigned	VHDL Type
C_BASEADDR	Base address for peripheral on OPB bus	0x00000000 to 0xffffffff C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.	0xffffffff	Yes	std_logic_ vector
C_HIGHADDR	Highest OPB address within peripherals address range	0x00000000 to 0xffffffff	0x00000 000	Yes	std_logic_ vector
C_OPB_DWIDTH	OPB bus data width	32	32	fixed	integer
C_OPB_AWIDTH	OPB bus address width	32	32	fixed	integer
C_FAMILY	Target architecture family	spartan2, spartan2e, spartan3, virtex, virtexe, virtex2, qvirtex2, qrvirtex2, virtex2p, virtex4	virtex2	Yes	string
C_MB_DBG_ PORTS	Number of processor ports that are interfaced with the MDM. The default is 1. For multiple connections, the debug signals for each processor must be explicitly connected to the MDM.	0-8	1	1	integer

Table 2: **OPB_MDM Design Parameters** *(Contd)*

Parameter Name	Feature/Description	Allowable Values	Default Value	Tool Assigned	VHDL Type
C_USE_UART	Enables the UART interface on the OPB bus. The UART signals over the JTAG port to the Xilinx Microprocessor Debug (XMD) tool.	0,1	1	1	integer
C_UART_WIDTH	Specifies the width of the FIFOs on the UART. When the width is 8, this UART behaves in a manner similar to the OPB_UARTLITE or the OPB_JTAGUART core	8,16,32	32	32	integer
C_WRITE_FSL_P ORTS	Specifies the number of write FSL ports that is implemented. This FSL port can be used for fast download from XMD.	0,1	0	0	integer

Allowable Parameter Combinations

There are currently no restrictions on parameter combinations for this core.

Parameter - Port Dependencies

The core has no parameter-port dependencies.

OPB MDM Register Description

The OPB MDM registers are listed and described in Table 3.

Table 3: **OPB MDM Registers**

Register Name	Size	Address Offset	Initial State	Description
Rx_FIFO	C_UART_WIDTH	0	0	JTAG UART receive data
Tx_FIFO	C_UART_WIDTH	4	0	JTAG UART transmit data
Status_reg	8	8	0x04	Read only bit 7 rx_Data_Present bit 6 rx_Buffer_Full bit 5 tx_Buffer_Empty bit 4 tx_Buffer_Full bit 3 enable_interrupts
Ctrl_reg	8	C	0x03	Write only bit 3 enable_interrupts bit 5 Clear Ext BRK signal bit 6 Reset_RX_FIFO bit 7 Reset_TX_FIFO

OPB MDM Interrupt Descriptions

If the interrupt enable register bit in the control register is set, the UART will raise the interrupt signal in the cycle when the TX FIFO goes empty, or in every cycle where the RX FIFO has data available.

Design Implementation

Design Tools

The OPB MDM design is handwritten.

XST is the synthesis tool used for synthesizing the OPB MDM. The EDIF netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The intended target technology is an FPGA in one of the following families: Virtex, Virtex-E, Spartan-II, Spartan-IIE, Spartan-3, Virtex-II, QPro Virtex-II, QPro-R Virtex-II, Virtex-II Pro, or Virtex-4.

Device Utilization and Performance Benchmarks

Not available.

Specification Exceptions

Not applicable.

Reference Documents

The MDM core is intended to be used with the EDK XMD tool. For more information on how to debug using MDM and XMD, see the G111 Embedded System Tools Guide.

Revision History

Date	Version	Revision
2/12/03	1.0	Initial Xilinx release.
3/26/03	1.1	Brought unused BSCAN signals out for Chipscope ICON usage.
12/19/03	1.2	Added LogiCORE Facts table. Reformatted to current Xilinx template, Added Write FSL Port feature
1/15/04	1.3	Updated copyright to 2004. Updated trademarks.
8/10/04	1.4	Updated format. Corrected parameter and signal interface. Added block diagram.
8/13/04	1.5	Updated for EDK 6.3; reviewed and corrected trademark usage.
4/02/05	1.6	Updated for EDK 7.1 SP1. Added Virtex-4 to supported architecture list
9/26/05	1.7	Converted to new DS template; updated figure to Xilinx graphic standards; updated hyperlinks and cross references.
12/2/05	1.8	Added Spartan-3E to supported device families listing.