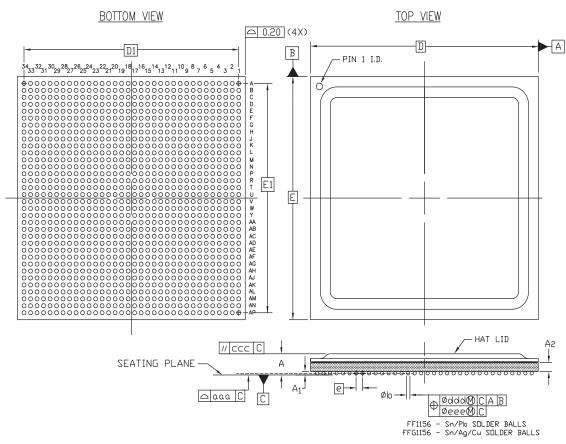
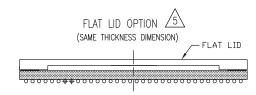


1156 Ball Flip-Chip BGA (FF1156/FFG1156) Package for Virtex-6 FPGAs

PK401 (v1.0) January 7, 2010



S Y M B	MILLIMETERS			N D T F
L	MIN.	N□M.	MAX.	Ė
Α	2.70	~	3,50	
A ₁	0.40	0,50	0.60	
Α ₂	0.90	*	1,50	
D/E	35.00 BASIC			
D1/E1	33.00 REF			
е	1.00 BASIC			
Øb	0.50	0.60	0.70	4
aaa	*	*	0.20	
ccc	*	*	0.35	
ddd	*	*	0.30	
eee	*	*	0.10	
М		34		2



NOTES:

- 1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
- 2. SYMBOL 'M' IS THE BALL MATRIX SIZE
- 3. CONFORMS TO JEDEC MS-034-AAR-1
- 4. ACTUAL SOLDER BALL COUNT = 1156
- FLAT LID WILL BE USED ONLY FOR THE FOLLOWING DEVICES, XC6VSX475T, XC6VSX315T, and XC6VLX365T
- 6. THIS PACKAGE IS ONLY USED FOR VIRTEX[®]−6 FPGAS REFER TO PK384 FOR THE MECHANICAL DRAWING OF THE FF1156 PACKAGE USED BY VIRTEX-5 FPGAS

pk401_01_121009

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Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
01/07/10	1.0	Initial Xilinx release.

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