ANALOG DEVICES

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APPLICATION NOTE

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Understanding and Preventing Latch-Up in CMOS DACs

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INTRODUCTION

Many designers now use analog and digital CMOS ICs in their designs to conserve power and increase board functionality. An extensive range of CMOS logic, A-to-D converters, D-to-A converters and op amps are currently available; however, some engineers using these devices for the first time are either unaware of, or are intimidated by the tendencies of some junction isolated CMOS ICs to latch up under certain conditions. Latch-up is defined as the generation of a low impedance path between the power supply rails by the triggering of a parasitic four-layer bipolar structure commonly referred to as an SCR (Silicon Controlled Rectifier). This parasitic SCR is inherent in all CMOS input and output circuitry, and applies to both analog and digital integrated circuits. This application note examines the mechanisms that cause SCR action in CMOS integrated circuits, discusses the pitfalls that are commonly encountered in circuit design that can lead to latch-up, and finally presents techniques to eliminate it. The reader can skip the sections on theory if desired and proceed straight to the sections on Identifying the Causes of Latch-up, and Latch-up Prevention Techniques.

SCR OPERATION

Prior to discussing latch-up in CMOS ICs, it is useful to review the basic theory of SCR operation to gain an understanding of the underlying mechanisms that cause latch-up. An SCR has the PNPN structure and characteristics shown in Figures 1 and 2, respectively. The SCR is a normally-off device that looks like a reverse-biased diode until triggered. Then it latches and conducts a high current until the current falls below a minimum holding value. The four-layer SCR can be modelled with two bipolar transistors, one NPN and one PNP, connected as shown in Figure 3. The resulting device has three main terminals – an anode, a cathode and a gate, plus a secondary gate which is connected to the base region of the PNP transistor. Conduction of current through the SCR is initiated by injecting sufficient current into the base of Q_2 to turn it on. When this is done, Q_2 draws collector current through the base-emitter junction of Q_1. Consequently, Q_1 turns on, which causes additional current to be injected into Q_2's base. This in turn causes Q_2 to turn on even harder, thus supplying more base current to Q_1. The positive feedback arrangement formed by Q_1 and Q_2 sustains SCR conduction even when the gate current is removed altogether. Once triggered, the device will remain in this low impedance state indefinitely until one of two things happen: if the voltage applied across the SCR is reduced to the point where Q_1 or Q_2's emitter-base junction turns off, then Q_1 or Q_2 will cease to conduct because it has no base current and the SCR will turn off; alternatively if the current through the SCR is reduced below the minimum holding current required to sustain conduction, it will also turn off.

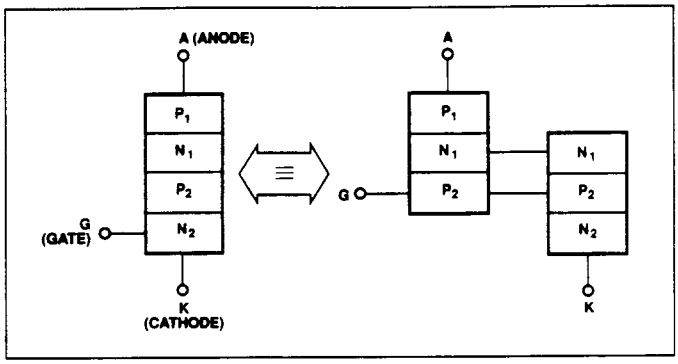

FIGURE 1: *An SCR has a four-layer structure as shown, but can also be thought of as two bipolar transistors merged together.*

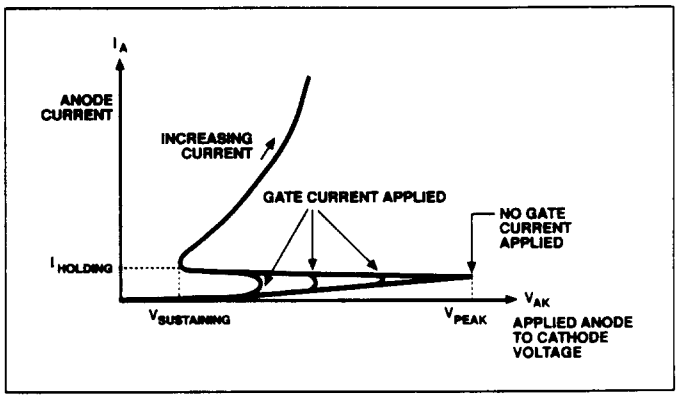

FIGURE 2: *The typical characteristics of an SCR indicate that once triggered, the device conducts a high current generally limited only by the power supply and load.*

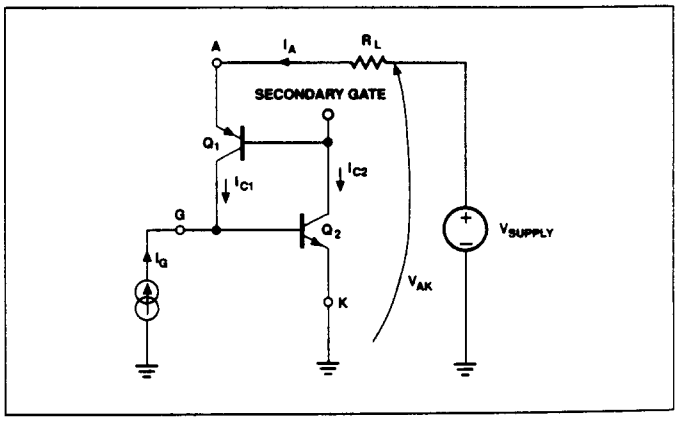

FIGURE 3: *The bipolar transistor model of an SCR shows the positive feedback loop formed when the collectors of Q_1 and Q_2 feed the base terminals of each other.*

There are three ways in which the SCR can be triggered into a conducting state. The first and most direct way is to externally inject a sufficiently large current into either of the gate terminals.

A second and less obvious way is to increase the applied anode to cathode voltage (V_{AK}) until avalanche breakdown occurs in the N_1-P_2 junction. This effectively causes current injection into the gate region of the SCR and will cause it to latch on and continue conducting even when the applied voltage is reduced below the peak sustaining voltage of the device. The third way to trigger the device is to apply a sufficiently high $\Delta V_{AK}/\Delta t$, or slew rate.so that current is injected into the gate region through the depletion layer capacitance of the N_1-P_2 junction. Although the junction depletion region capacitance decreases with increasing V_{AK}, thus reducing the amount of current injected, high enough slew rates can still cause sufficient current injection into the gate region to make the SCR latch on.

It should be noted that the effects of breakdown voltage and $\Delta V_{AK}/\Delta t$ on the trigger point of the SCR are intensified by the presence of any gate current flow. That is to say that the peak sustaining voltage and the maximum allowable slew rate both decrease as the applied gate current increases. These effects are often noticeable in CMOS ICs that are prone to latch up.

DIGITAL INPUT AND OUTPUT RELATED SCR STRUCTURES IN CMOS DACs

A typical unbuffered CMOS inverter is shown in Figure 4 for simplicity, and contains one N-channel MOSFET with its source and body tied to DGND, and one P-channel MOSFET with its source and body tied to V_{DD}. This input and output structure, while shown together in an inverter for convenience, is characteristic of all the digital inputs and outputs on PMI's CMOS DACs. The diodes shown from the output terminal to DGND and V_{DD} are body diodes inherent in the construction of the MOSFETs themselves,

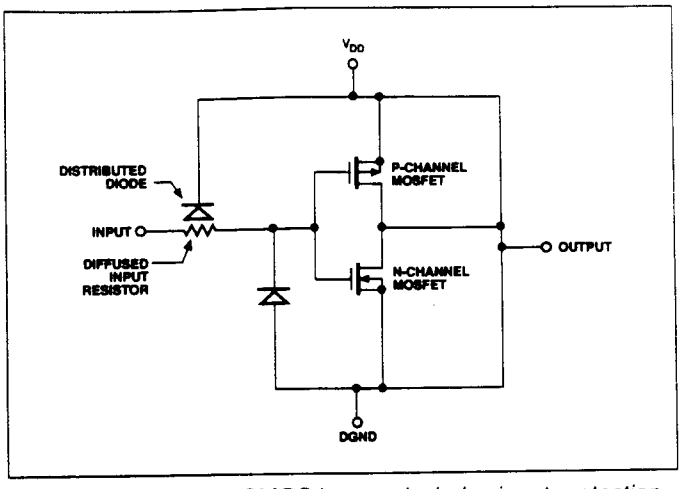

FIGURE 4: *A simple CMOS inverter includes input protection diodes to improve the ESD sensitivity of the device. The output diodes are formed because the bodies of the MOSFETs are electrically connected to V_{DD} and DGND.*

while the input resistor, input diode to DGND and the distributed diode to V_{DD} are deliberately included to clamp the gates at the power supply rails. This input protection circuitry greatly reduces the sensitivity of the MOSFET gates to electrostatic discharge (ESD) damage due to oxide rupture, and is now common on almost all CMOS integrated circuits.

Forward biasing any one of the four diodes shown in Figure 4 can lead to SCR action if the current through them is high enough. Figure 5 depicts a cross sectional view of the CMOS inverter, showing how the N- and P-channel MOSFETs are fabricated. The P-channel device is formed directly in the N– type substrate, while the N-channel device sits in a P– type well. A parasitic four-layer

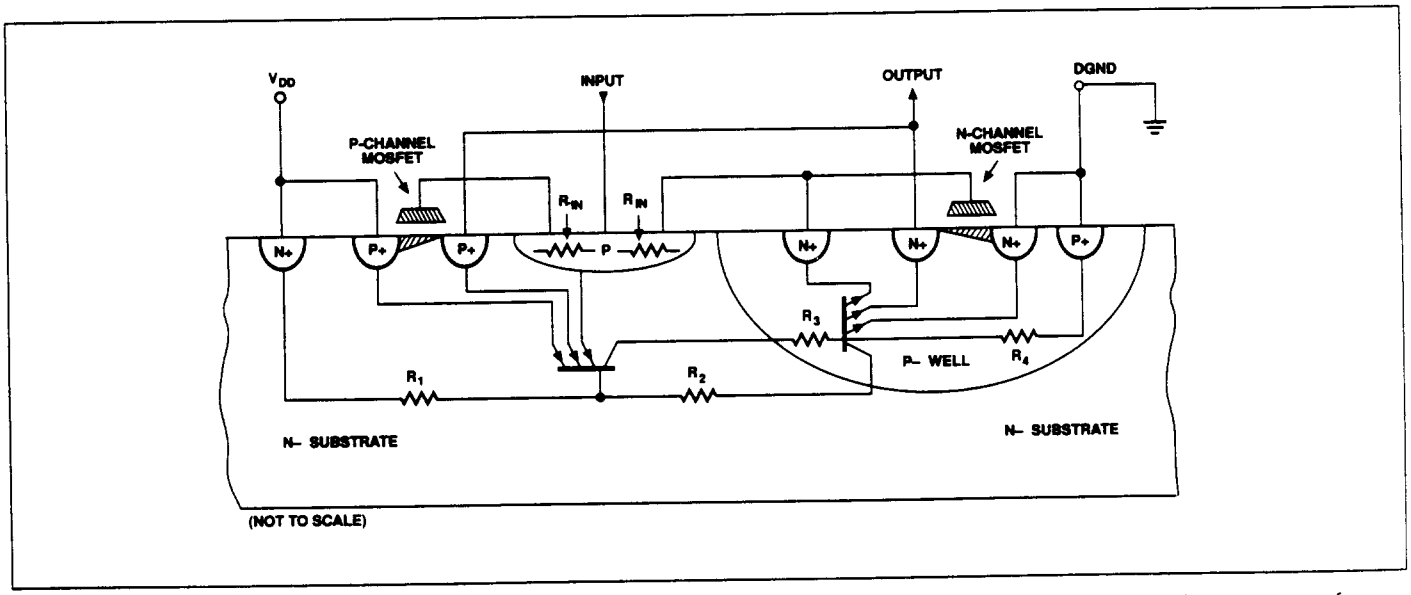

FIGURE 5: *This cross sectional view of a simple CMOS inverter with its input protection diodes clearly shows the presence of parasitic PNP and NPN transistors.*

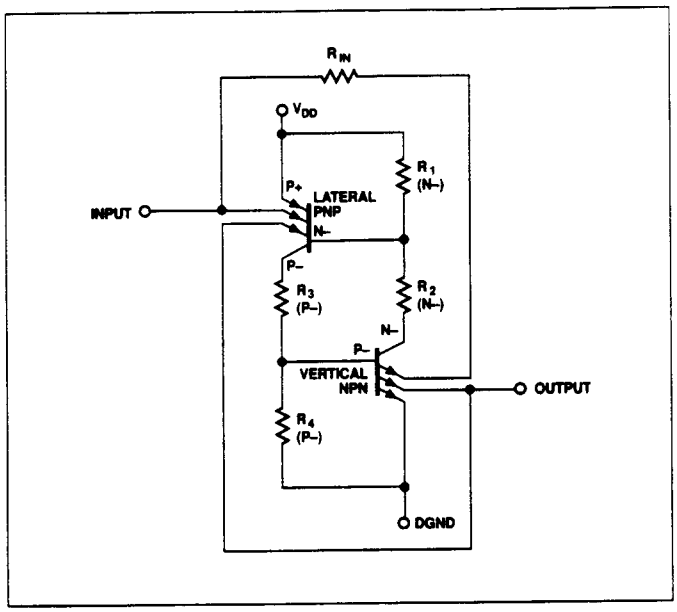

FIGURE 6: *Rearranging the parasitic bipolar transistors shown in Figure 5, gives the easily recognizable circuit of an SCR.*

SCR, shown schematically in Figure 6, is formed when the N and P-channel MOSFETs are located in close proximity to each other. The multi-emitter vertical-NPN transistor results from the fabrication of the N-channel MOSFET in the P– well, and the multi-emitter lateral-PNP transistor results from the fabrication of the P-channel MOSFET in the N– substrate. Fortunately, the PNP transistor has a wide base region and consequently a low current gain, β_F, usually much less than one. Thus, it typically takes hundreds of milliamps of current to trigger SCR action. Notice that the parasitic SCR is connected directly across the power supply rails of the CMOS device, and when triggered, presents a low impedance path that will cause excessive current to flow. This condition is potentially destructive if allowed to persist, since it will result in permanent damage to the bond wires or chip metallization due to localized overheating.

In a CMOS DAC no explicit gate terminal is available, but triggering the parasitic SCR can still be accomplished in a number of ways. The most common cause is when the input voltage exceeds V_{DD} by about 0.3 to 0.7 volts. Then the parasitic PNP transistor's emitter-base junction turns on, thus causing SCR action. The input undervoltage situation is different, however, because there is an input resistor in series with the protection diode connected to DGND. The input can thus be swung further below DGND (usually by as much as 2-3 volts) before the diode will conduct. This means that under normal operating conditions, there is more of a margin of protection against input undervoltage than input overvoltage. Similarly, if the output terminal is allowed to exceed V_{DD} by about 0.3 to 0.7 volts, then conduction of the lateral-PNP transistor initiates SCR action. Finally, pulling the output below DGND by more than 0.3 to 0.7 volts causes the vertical-NPN transistor's emitter-base junction to turn on and also causes the SCR to trigger.

ANALOG GROUND AND OUTPUT RELATED SCR STRUCTURES IN CMOS DACs

There are two other ways in which latch-up can be triggered in a CMOS DAC, in addition to the digital input/output overvoltage situation already mentioned. CMOS DACs such as those manufactured by PMI include analog circuitry on the same chip as the digital logic, as shown in Figure 7. Currents flowing from the thin-film resistor R-2R ladder network are switched either to AGND or I_{OUT} (a summing node) using N-channel transistors. These are contained in an isolated P– well, and have one drain connection and two sources. This second P– well is connected to analog ground and *not* digital ground.

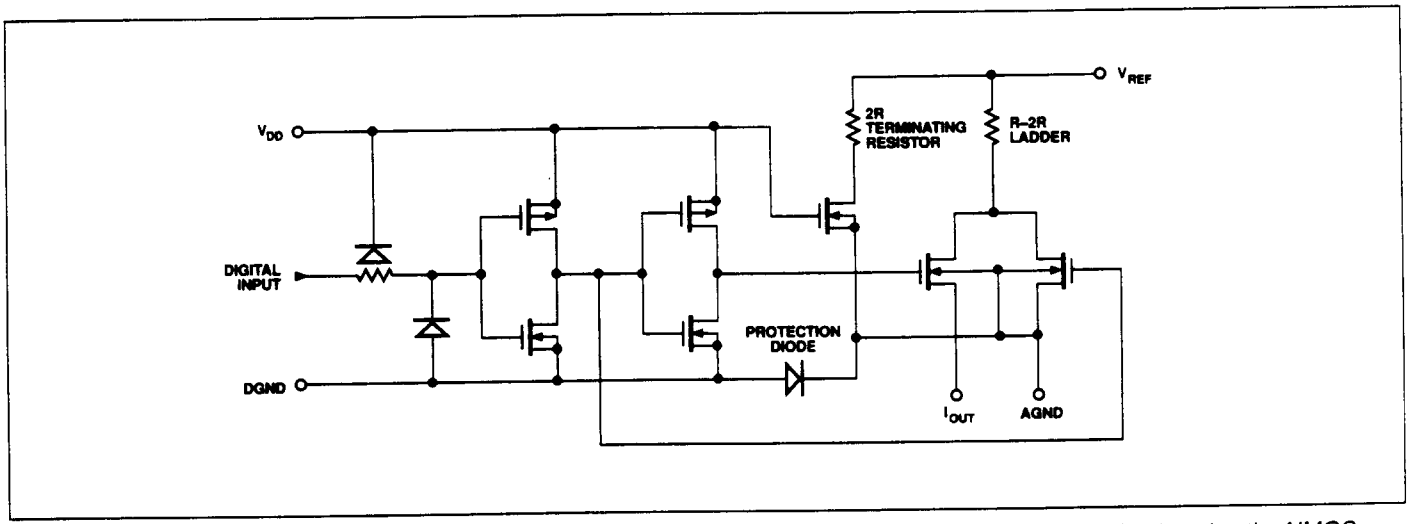

FIGURE 7: *This simplified diagram of a CMOS DAC with a thin film R-2R ladder shows the digital input circuitry plus the NMOS current switches. A protection diode is included to improve the ESD tolerance.*

Figure 8 shows how an additional parasitic SCR structure is formed by the NMOS current switches. If the I_{OUT} terminal is pulled below AGND by more than 0.3 to 0.7 volts then the parasitic NPN transistor associated with the analog P– well is turned on. This may result in SCR latch-up when the power supplies are turned on and sufficient current is flowing out of I_{OUT}.

Note that an additional clamping diode is included from DGND to AGND as shown in Figure 9, being formed by an N+ diffusion in a separate P– well. The purpose of this diode clamp is to reduce the ESD sensitivity of N-channel current switches. However, the protection diode from DGND to AGND adds another parasitic SCR to the device structure. If DGND is allowed to exceed AGND by more than 0.3 to 0.7 volts, then the parasitic NPN transistor is forward biased, and the probability that the device will latch up when the power is turned on is high. Both of these situations should be avoided.

IDENTIFYING THE CAUSES OF LATCH-UP

Now that the mechanism of SCR latch-up has been understood, potentially dangerous situations can be identified that could cause catastrophic failure of a CMOS IC. A list of latch-up inducing conditions to be avoided is an important checklist for system designers. The following guidelines should be followed for all designs using CMOS ICs.

1. Digital inputs should not be allowed to exceed V_{DD} by more than 0.3 volts at any time. This includes a power-down situation when V_{DD} = zero.

2. Digital inputs should also not be allowed to go below DGND by more than about 2 to 3 volts (many data sheets usually give –0.3 volts as the maximum limit, however).

3. Digital outputs also should not be allowed to exceed V_{DD} or DGND by more than ±0.3 volts at any time.

4. For a CMOS DAC, DGND should not be allowed to exceed AGND by more than 0.3 volts.

5. For a CMOS DAC also, I_{OUT} should, in general, not be allowed to fall below AGND by more than 0.3 volts. Some DACs can tolerate significant I_{OUT} current flow, however, without any danger of latch-up.

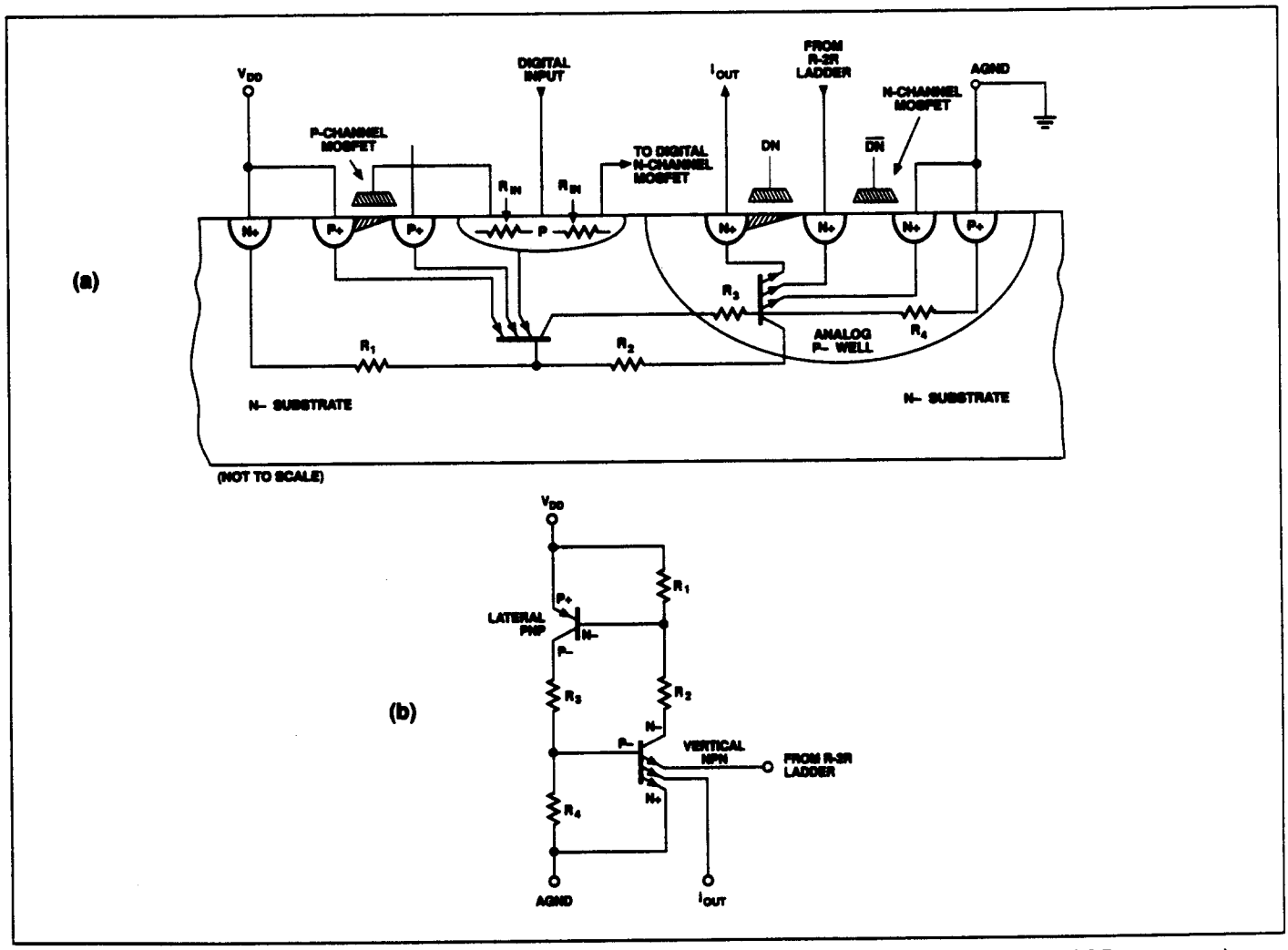

FIGURE 8: *The NMOS current steering transistors of a CMOS DAC shown in (a) form an additional parasitic SCR structure shown in (b) that can cause latch-up when I_{OUT} is pulled more than a base-emitter drop below AGND.*

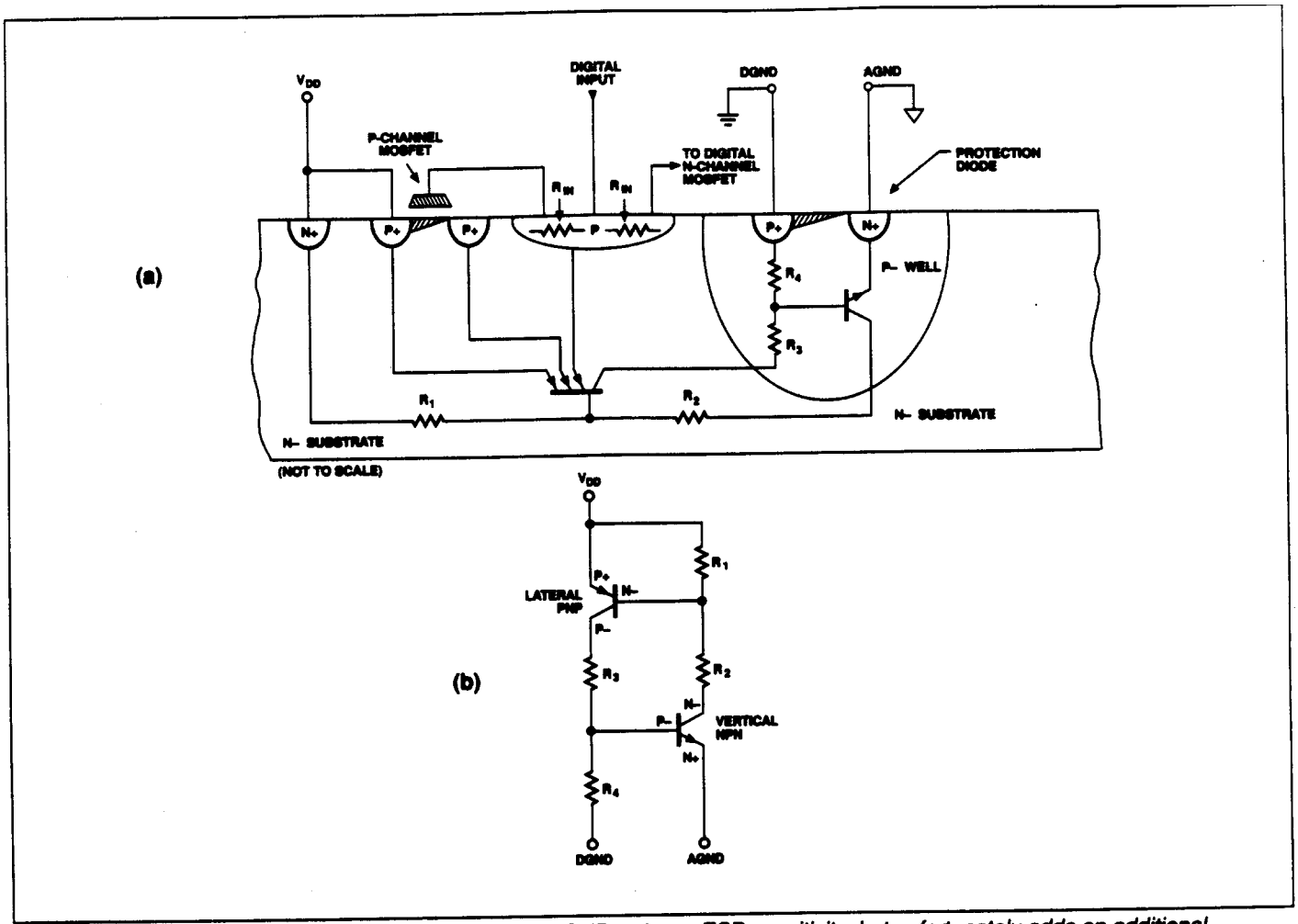

FIGURE 9: *A clamp diode shown in (a) from DGND to AGND reduces ESD sensitivity, but unfortunately adds an additional parasitic SCR to the DAC structure as shown in (b).*

Even a normally benign system design can sometimes unknowingly violate one or more of the aforementioned rules. Consider the case where a CMOS logic IC, with its power supply at zero volts (i.e., turned off), has its inputs driven by another logic IC that is powered from a different power supply. Here the upper input protection diodes of the IC being driven are forward biased, and if enough current flows through them then SCR action can occur. This situation is more common than most engineers would care to admit. It is especially noticeable in large systems that use local on-card regulators to power the ICs on board, but distribute signals amongst many boards through a backplane interconnection scheme. When raw power is applied to all boards, some of the on-card regulators start up before others, thus allowing signals to be applied to ICs on boards that have not yet powered up. Figure 10 shows how this can happen. This violates rule No.1 and could definitely cause some devices to latch up and conduct high currents after their power supplies came up to the normal operating voltages.

Other problems can occur even on single board systems that use multiple power supplies for the analog and digital circuitry.

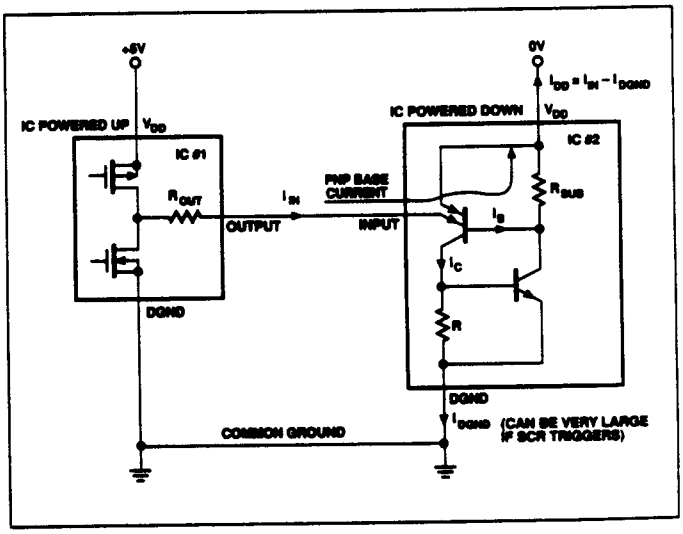

FIGURE 10: *When an unpowered CMOS IC has any inputs driven more than +0.3 to +0.7 volts above DGND, the parasitic PNP transistor will begin to conduct. Note that before the SCR triggers, the base current for the lateral-PNP transistor flows out of the V_{DD} pin of IC #2.*

Consider a CMOS DAC that is powered from a +12 volt supply, but is driven by on board +5 volt CMOS logic. If the +12 volt supply comes up before the +5 volt supply, then there will be no forward biasing of the digital input protection diodes on the DAC, and latch-up will not occur. On the other hand, if the +5 volt supply comes up first and one or more of the digital inputs to the DAC are high, then the upper input protection diodes are forward biased and latch-up will probably occur if there is enough current flowing into these inputs. With more and more data acquisition and analog output boards being designed for personal computers, the lack of a guaranteed turn-on sequence for the +5 volt and ±12 volt supplies that most PCs typically use can be a hazardous situation. Indeed, improper power supply sequencing is the cause of almost all cases of latch-up in CMOS ICs no matter what they are – logic devices, DACs or op amps.

Additional problems can also be encountered when CMOS logic outputs are used to drive highly reactive loads or unterminated transmission lines. Either of these can cause sufficient overshoot and undershoot to forward bias the parasitic input or output diodes, and can also lead to latch-up induced failures, if there is sufficient current flow for the time duration of the ringing.

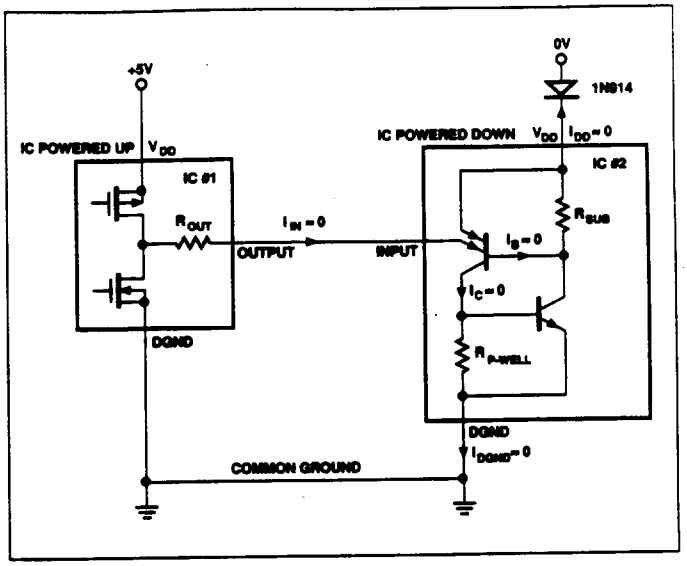

FIGURE 11: *Adding an inexpensive silicon diode in series with the V_{DD} pin of the unpowered IC, effectively prevents the parasitic lateral-PNP transistor's base current from flowing and inhibits SCR action.*

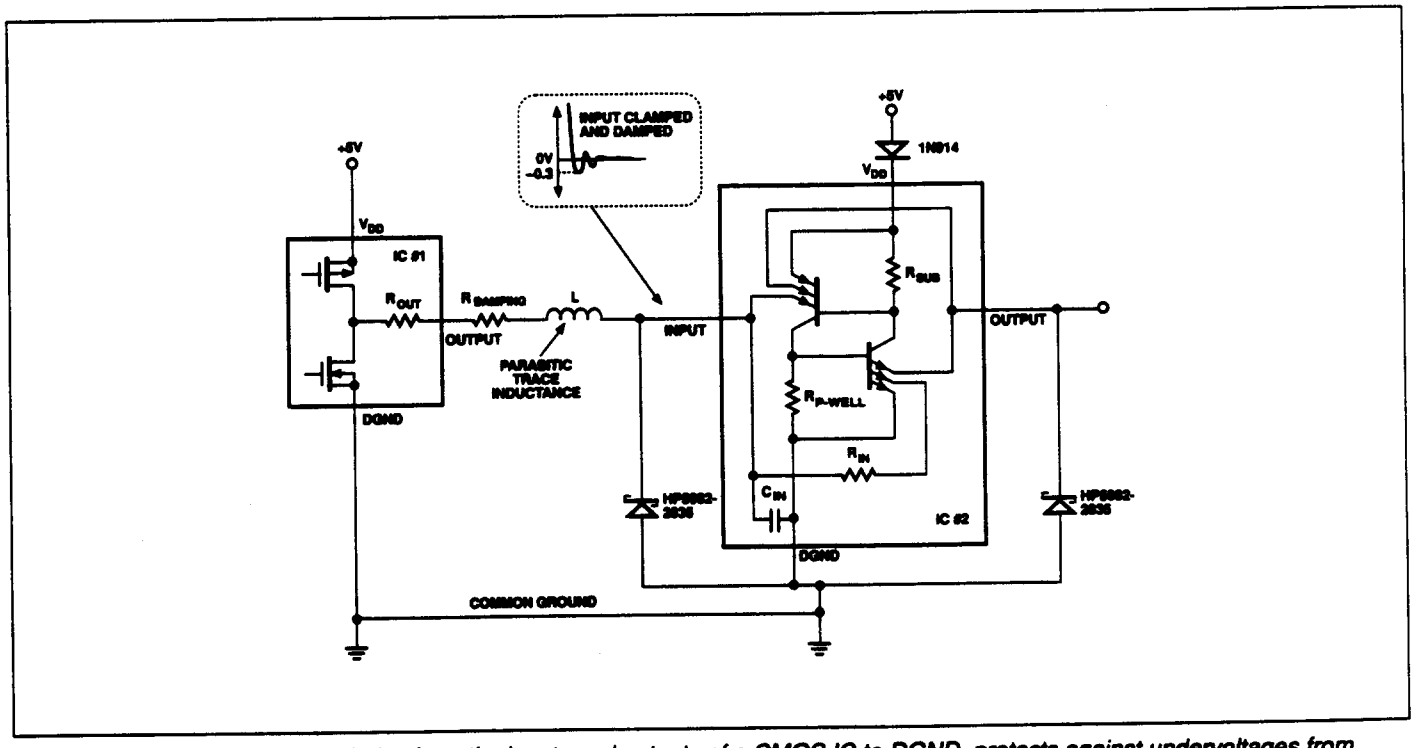

FIGURE 12: *Adding Schottky diodes from the inputs and outputs of a CMOS IC to DGND, protects against undervoltages from causing conduction of the parasitic NPN, thus inhibiting SCR action. The series damping resistor makes ringing due to long PC board traces die out more quickly.*

Fortunately, latch-up problems with modern CMOS ICs are becoming rarer and rarer due to special design techniques that are being incorporated to raise the required input or output current trigger levels to very high values (hundreds of milliamps). However, rugged ICs are still no substitute for good design practice.

LATCH-UP PREVENTION TECHNIQUES

The following recommendations should be implemented in general, for all CMOS designs that violate one or more of the previously discussed rules:

1. If the digital inputs or outputs of a device can go beyond V_{DD} at any time, a diode (such as a 1N914) connected in series with V_{DD} will prevent SCR action and subsequent latch-up. This works, because the diode prevents the base current of the parasitic lateral-PNP transistor from flowing out of the V_{DD} pin, thus prohibiting SCR triggering. This is shown in Figure 11.

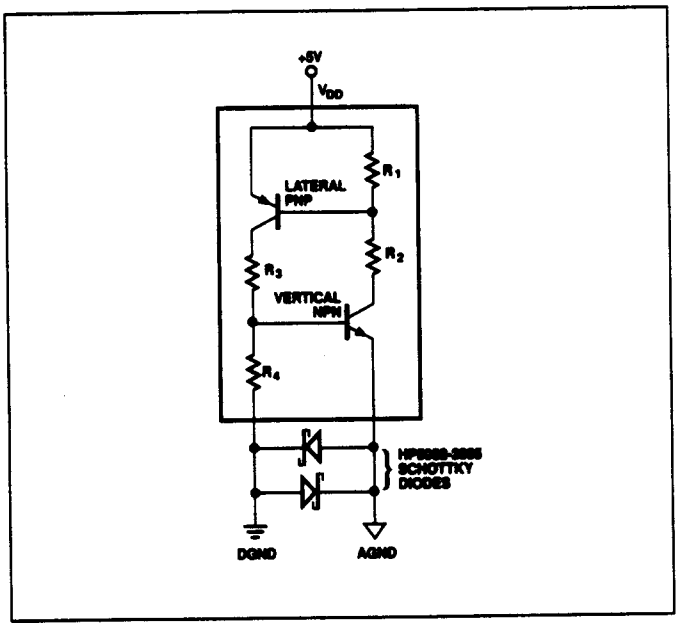

FIGURE 13: *Connecting Schottky diodes between DGND and AGND prevents conduction of the parasitic NPN transistor, and helps to minimize injected noise from DGND to the analog output.*

2. If the digital inputs or outputs of a device can go below DGND at any time, a Schottky diode (such as an HP5082-2835) connected from those inputs or outputs to DGND will effectively clamp negative excursions at –0.3 to –0.4 volts. This prevents the emitter-base junction of the parasitic NPN transistor from being turned on, and also prevents SCR triggering. Figure 12 shows the connections for the Schottky diodes.

3. If the DGND potential can occasionally exceed AGND by more than 0.3 volts, a Schottky diode placed between the two pins of the device will prevent conduction of the associated parasitic NPN transistor. This provides additional protection against latch-up as shown in Figure 13. An extra diode connected in inverse parallel with the one just mentioned provides clamping of DGND to AGND in the other direction and will help to minimize digital noise from being injected into the DAC.

4. In circuits where the I_{OUT} pin of a CMOS DAC can be pulled below AGND, another Schottky diode clamp between these two terminals will prevent sensitive ICs from latching up. This condition sometimes occurs with high-speed bipolar operational amplifiers that are used as current-to-voltage converters following the DAC. During power-up or power-down transitions, the op amp's inverting input presents a low impedance from I_{OUT} to the negative supply rail. An unprotected DAC may not be reliable without the requisite Schottky diode clamp to AGND.

5. Finally, in designs that have long digital PC board traces between components and are prone to inductive ringing problems, a series damping resistor of 10–100Ω often will be beneficial. This resistor increases the damping factor of the equivalent series RLC network and causes the ringing to decay more quickly. This will help to prevent conduction of the input or output protection diodes.

Keeping these relatively simple and inexpensive procedures in mind when designing with CMOS ICs will prevent commonly encountered problems due to latch-up, resulting in trouble-free operation. The old proverb that says, "An ounce of prevention is worth a pound of cure," is very appropriate here.