ANALOG DEVICES

AN-277
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Applications of the AD537 IC Voltage-to-Frequency Converter

by Barrie Gilbert and Doug Grant

I INTRODUCTION

Product Description

The AD537 is a monolithic voltage-to-frequency converter combining simplicity of use in standard applications with an unusual degree of flexibility and versatility. Designed for either single- or dual-supply operation at low voltages and current (5V and 1mA) the AD537 has the capability for driving high-voltage, high-current loads (36V and 20mA). The chip includes an accurate band-gap reference generator, a low-drift input amplifier capable of operating directly from millivolt signals, a precision current-controlled oscillator and a high-current output stage. It is a complete circuit, using low temperature coefficient silicon-chromium thin-film resistors throughout, except for one external resistor and one capacitor. These provide the user with a means for programming the full-scale input voltage from 100mV to 10V (or greater, depending on the positive supply voltage in some cases), and the full-scale (FS) frequency to any value less than 150kHz. Either positive or negative input voltages can be accepted. The scaling relationship is simply f = V/10RC, simplifying the choice of the external components. Linearity error is as low as ±0.07% for 10kHz FS guaranteed over an 80dB dynamic range. The output frequency is stable with temperature (typically ±50ppm/°C excluding the effects of external components) and supply (typically ±0.01%/V from 5 to 36V).

The specially-designed input amplifier, which actually functions as a voltage to current converter, has a typical drift of only ±1μV/°C when nulled, which permits operation directly from such low-level transducers as strain-gauges, thermocouples, current-shunts, etc., while offering a high (250MΩ) input resistance to positive signals. The output stage, an open-collector NPN circuit, can sink up to 20mA with a saturation voltage less than 0.4V, and withstand a supply of 36V. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4V below $+V_S$, permitting easy interfacing with any digital logic family. The high current capability means that LED's, long cables, or up to 12 TTL loads can be driven directly. Unlike most V-F converters, the AD537 is designed to deliver a square-wave output; this has advantages both internally (the power dissipation is essentially independent of frequency, so that self-heating effects do not cause linearity errors) and externally (the average level of the output is constant, useful in ac-coupled links; it also allows operation as a phased-locked-loop in F-V and other applications).

Two auxiliary outputs are provided to enhance the versatility. The first is a fixed voltage of 1.00V, generated by the primary band-gap reference circuit. This is useful in many applications described here; for example, it can be used to power a resistive transducer, or provide the reference voltage for an associated DAC. The second is an output scaled +1.00mV/°K which enables the circuit to be used as a reliable temperature-to-frequency converter; the error due to self-heating can be kept to less than 1°K using a 5V supply and light output loading. Used in conjunction with the fixed reference output, offset scales such as Celsius or Fahrenheit can be accommodated.

Whereas most V-F converters are limited in their range of applications to basic telemetry and slow A-D conversion, the low cost, low power drain and high flexibility of the AD537 open up a wide spectrum of uses. The long-term stability is excellent, and assured by subjecting every device to a stabilization bake and ten temperature cycles of -65°C to +150°C prior to final test. The circuit is available in three performance grades in a 14-pin ceramic package or 10 pin hermetic metal can. For complete specifications see the data sheet.

Theory of Operation

A block diagram of the AD537 is shown in Figure 1. The key to accurate operation is the current-to-frequency converter, which is a very carefully designed multivibrator. The main advantages of the circuit are its simplicity, requiring only a single timing capacitor; the use of push-pull charging, resulting in a large voltage across this capacitor even at low supply voltages, for improved timing accuracy and low cycle-to-cycle jitter; its square-wave output, generally more useful than the narrow pulse generated by charge-dispensing converters; and its good linearity. By using special adaptive biasing techniques operation of this multivibrator is possible over a very large dynamic range, from a maximum control

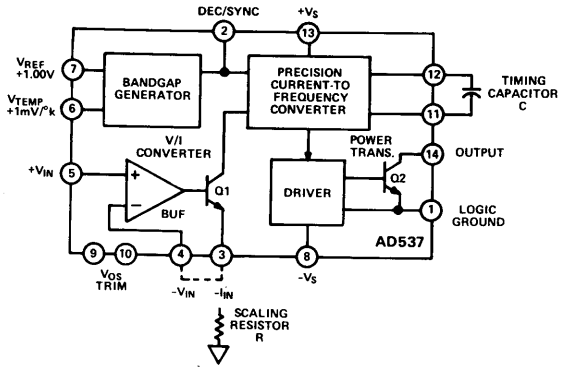


Figure 1. Block Diagram of AD537

current of 2mA to less than 100nA. It can be shown that the basic circuit has a well-defined temperature-coefficient of 300ppm/°K (at all values of control current), and use is made of the tight thermal coupling to the associated band-gap reference generator, which supplies an exactly-proportioned temperature-compensation voltage to the multivibrator. The band-gap cell also provides all the required bias for internal operation of the chip, the fixed reference output and the temperature-proportional output.

The square-wave output of the multivibrator operates the output driver which provides a floating drive current to the large-geometry output transistor, Q2 (Figure 1). Internally, there are actually two transistors (in a thermally symmetric layout for minimal interaction with the remaining circuits) designed for very low saturation voltage and driven to combine low ON voltages with a well-defined current limit.

The SYNC input (pin 2) allows the oscillator to be slaved to a master clock if desired. It also permits control of the state of the output. These uses of the SYNC pin are dealt with in later sections.

A versatile operational amplifier (BUF) serves as the input stage. Its purpose is to convert the applied input voltage to a control current in Q1 (Figure 1); this current is optimally 1mA at the input corresponding to the maximum output frequency. By strapping pins 3 and 4 the input voltage can be impressed across the external scaling resistor, R, which is chosen to provide the needed transconductance for the application. For example, for a FS input voltage of 2.5V the optimum resistor value in most cases will be 2.5kΩ. The $+V_{IN}$ terminal of the op-amp (pin 5) offers a high input resistance (250MΩ) with a bias current of about 100nA. The design of the op-amp ensures that the effect of finite bias current on drift is small, that is, drifts of the order of 1μV/°C can be achieved even with source-resistance/scaling-resistance imbalances of 1kΩ. Consequently, the AD537 can accommodate millivolt signals without the need for a pre-amplifier. The input configuration is also quasi-differential, so that errors due to ground-loops can be avoided by proper choice of signal connections. The common-mode range of the input extends from 4V below $+V_S$ (that is, from +11V for a $+V_S$ of 15V) right down to $-V_S$, so that inputs down to ground potential can be accepted even when operating from a single supply voltage. Negative inputs (voltages or currents) can be accepted, by fixing the voltage on pin 5 (usually to ground potential) and driving pins 3 and 4.

The precision voltage reference is based on Brokaw's cell and incorporates some novel features to ensure a small spread in output voltage without the need for laser-trimming. The internal voltage of approximately 1.22V is resistively-divided to provide the output of 1V at pin 7, which therefore has a finite output resistance (380Ω nominal). Loading errors will occur in applications where this voltage is used to drive external components. This is clarified in a later section. Likewise, the temperature-proportional output at pin 6 has a nominal source resistance of 900Ω, and loading must be considered. When the AD537 is used in the thermometer mode, the loading of the input op-amp (pin 5) is negligible.

Pins 9 and 10 are provided for trimming the offset voltage of the input op-amp to exactly zero, using an external pot whose slider is connected to $+V_S$. However, in many cases the low initial offset of the AD537 (2mV guaranteed for the AD537K) eliminates the need for trimming (it amounts to a zero-error of only 0.02% for a 10V input) and the device operates correctly without this pot. Note that no damage will result to the circuit if pin 9 or 10 is inadvertently connected to $-V_S$. Offset trimming is not available on the 10-pin metal can version of the AD537 due to pin limitations.

For further details of the internal design of the AD537, refer to B. Gilbert, "A Versatile Monolithic Voltage-to-Frequency Converter", *IEEE J. Solid State Circuits*, Vol SC-11, P852-864, Dec. 1976.

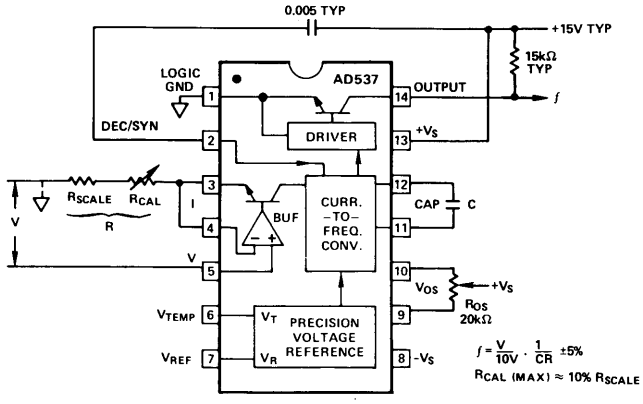
II BASIC OPERATING MODES

Positive Input Voltage

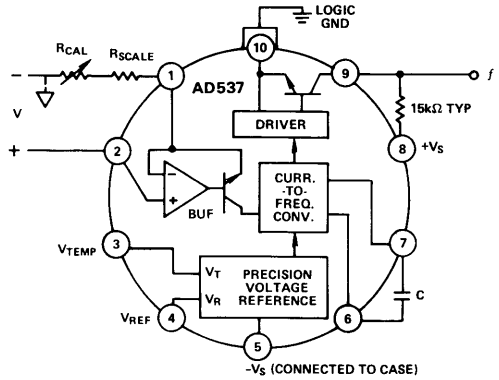
Figure 2 shows the connections for basic operation of the AD537 as a V-F converter with positive voltage inputs. Usually a single supply will be sufficient, with $-V_S$ and LOGIC GND strapped to the supply ground. The lower end of the scaling resistor should be connected to the appropriate signal ground to avoid errors due to the inevitable on-board voltage drops. The nominal value of R is chosen such that the FS input voltage sets up a current of 1mA in it. Thus, for a 0 to +10V input, R would be nominally 10kΩ. It is a simple matter to recalculate R for other FS voltages; note that with $+V_S$ = 5V the maximum input is +1V. However, the specifications allow for the fact that the supply may be 5% low, and in practice reliable operation can be achieved for inputs slightly in excess of +1V. Full-scale currents other than 1mA can be chosen, with some degradation of linearity.

In precision applications sufficient trim range must be provided to accommodate the scaling error of the AD537 (±7% max for the J, ±5% max for the K and S grades) and the tolerance on the timing capacitors, which might be ±3%. In the example just given, the fixed part of R could be 9.09kΩ and the scaling adjustment a 2kΩ pot of good resolution and stability. To accommodate an input of +10V the $+V_S$ supply must be at least +14V ($+V_{IN}$ + 4V); using a standard 15V supply a 10% over-range is possible.

Having chosen the scaling resistor to fit the FS input voltage requirement, the timing capacitor, C, is simply



a. 14 Pin Dip



b. 10 Pin Metal Can

Figure 2. Basic (Positive Input) Connections

calculated from the basic relationship

$$f = \frac{V}{10} \cdot \frac{1}{CR}$$

Thus, for a 10V FS input, the FS frequency is just 1/CR.

The timing capacitor will usually be either 0.01μF for 10kHz FS (1Hz/mV) or 1000pF for 100kHz FS (10Hz/mV), assuming R is 10kΩ. However, any convenient value can be used to set up a special scaling relationship. Linearity will be degraded with values below 1000pF, and 100pF is the minimum recommended capacitor size. There is no upper limit, but since the voltage on the capacitor reverses polarity every half-cycle, non-polarized types must be employed.

Good linearity requires the use of a capacitor with low dielectric absorption, and stable operation over temperature calls for a component having a small temperature coefficient. NPO ceramic, Teflon, and polystyrene capacitors best serve these needs. Mica and polycarbonate dielectrics are also acceptable, but linearity and stability will be degraded with most other types.

It is desirable to mount the capacitor as close as possible to pins 11 and 12, to avoid the effects of stray capacitance and pick-up.

Many of the applications found in these notes make use of the high sensitivity and low drift of the input amplifier. Special care should be exercised in returning the SIGNAL LOW input to the appropriate signal ground associated with the source, which can be at any potential from $-V_S$ to 4V below $+V_S$. The input resistance at pin 5 is very high (250MΩ typ.) so errors due to non-zero source resistance will not normally be encountered. The input bias current (100nA typ.) will generate an offset voltage of 100μV/kΩ. Where signals of high source resistance are used this offset may be significant and require the use of the offset trim adjustment, which has a range of approximately ±6mV. The input amplifier is designed so that imbalance between the source resistance and the scaling resistance does not cause appreciable drift after nulling has been effected with this adjustment; however, it is good practice to equalize these resistances whenever possible. The compensating resistor may either be included in series with pin 5 (when $R_S < R$ in which case it should be $R - R_S$) or in series with pin 4 (when $R_S > R$ in which case it should be $R_S - R$).

Calibration

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and pins 9 and 10. Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Every AD537 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature, and to ensure that the supply, source and load conditions are those applicable. Begin by setting the input voltage to zero. Adjust the offset pot until the AD537 just ceases to oscillate; this is most easily seen using a scope connected to the output (pin 14). For a 0.01% error it is permissible to adjust slightly above this point, until the output frequency is 1/10,000 of FS (for example, 1Hz for a FS of 10kHz). Then apply the FS input voltage and adjust R until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the small input current at pin 4. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input-voltage drift after offset nulling is typically below 1μV/°C.

Negative Input Voltage

By interchanging the SIGNAL HIGH and SIGNAL LOW inputs the AD537 can operate from negative input voltages, as shown in Figure 3. This connection does not offer a high input resistance, since the control current must now be provided by the source. Consequently the input resistance is simply equal to the scaling resistance, R, which is chosen to set up a nominal 1mA at the FS input voltage. Note that

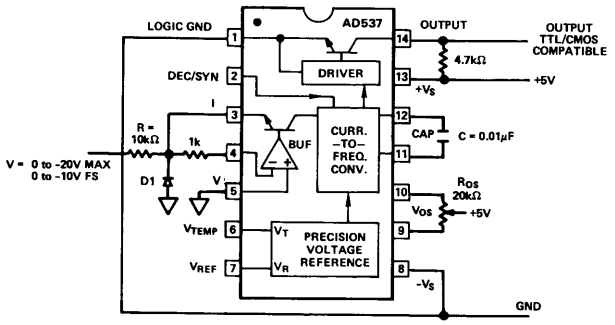


Figure 3. Negative Input Operation

the FS voltage can now be as large as desired, since it is not limited by the input amplifier common-mode range or supply voltage; for example, a -100V FS input would use a scaling resistor of 100kΩ, and the AD537 could operate from a +5V supply. If it is desirable to reduce the loading on the signal a lower FS control current can be used, with some sacrifice in dynamic range. For example, 1MΩ resistor could be used to convert the -100V input to a 100μA control current; the capacitor would then be reduced by a factor of ten to maintain the same FS frequency. This also provides a very large over-range capacity, useful in handling signals which may occasionally have large peak values.

Usually pin 5 will be at ground potential (strictly, at the SIGNAL LOW point), resulting in a current-sum node at pin 3. Thus, any number of signals may be added before conversion, and each source may have any desired scaling by appropriate choice of resistor. It is not necessary for pin 5 to be grounded; offset scales can be generated by setting the voltage on this pin at any value between $-V_S$ and $(+V_S - 4V)$. Diode D1 and the 1kΩ resistor (Figure 3) are added to provide overload and latchup protection.

The linearity in the negative-input mode is better than for positive inputs, since the degrading effect of finite common-mode rejection in the input amplifier is removed. This also allows the use of the minimum supply voltage, resulting in a further improvement in linearity.

The design considerations and trimming procedures are otherwise the same as for the positive-input mode.

Negative Input Current

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 4. A resistor-potentiometer connected from the V_R output, pin 7, to $-V_S$ will alter the internal operating conditions in a predictable way, and provide the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not alter the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C

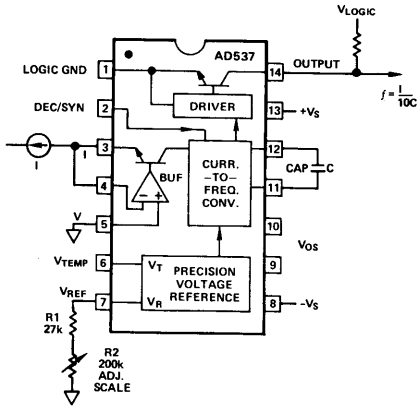


Figure 4. Scale Adjustment for Current Inputs

is selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

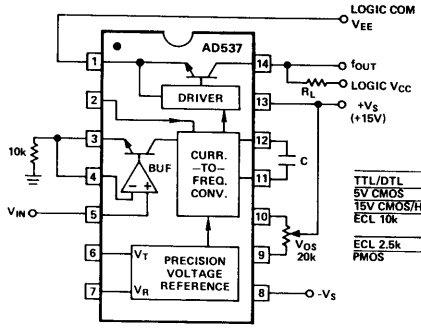
$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

Output Interfacing

The AD537 logic output is designed to interface with all digital logic families, LED's (for optical coupling), pulse transformers, and long lines. The open collector (pin 14) and the emitter (pin 1) of the output stage NPN transistor are both available for use; the emitter can be tied to any potential from $(+V_S - 4V)$ down to $-V_S$ and the collector can be pulled up to any voltage up to 36V above the emitter regardless of the $+V_S$ to pin 13.

Figure 5 shows the AD537 connected for a 0 to +10V input with general output interfacing. The required logic common voltage, logic supply voltage, pull-up resistor and $-V_S$ supply are shown in the accompanying table. In the TTL mode, up



	V_{CC}	V_{EE}	R_L	$-V_S$
TTL/DTL	+5	GND	4.7k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	4.7k	-8 to -15
ECL 2.5k	+1.3	-2	4.7k	-5
PMOS	0	-15	10k	-15

Figure 5. Interfacing Standard Logic Families

to 12 standard gates (20mA) can be driven at a maximum LOW voltage of 0.4V.

The output stage is current-limited and can be shorted indefinitely to pin 1 (normally ground). When shorted to $+V_S$ the current in the ON state is approximately 35mA, and under most conditions this will not result in damage. For example, with pin 1 at ground and pin 14 shorted to +15V, and the oscillator running, the average power in the output stage is 262.5mW (15 x 35/2). However, if high supply voltages are used and the output stage is in the ON state for long periods (low input levels), the peak dissipation of 1260mW (36 x 35) will cause considerable heating, and it is recommended to avoid this situation for prolonged periods.

Signal Isolation

It will often be necessary to couple the frequency output of the AD537 to a system at a different dc level. Where the voltage difference is fixed, or varying relatively slowly, capacitive coupling can be used. Usually, the purpose of the isolation scheme is to reject large amounts of common-mode voltage up to high frequencies, in which case optical or transformer coupling should be used. These also provide a higher degree of isolation safety. Examples are found elsewhere in these notes.

True Two-Wire Data Transmission

Figure 6 shows a useful technique for operating an AD537 at the remote end of a single wire pair, which serves to supply power to the circuit and to transmit the frequency-encoded signal back to a central point. The PNP circuit at the receiving end of the line converts the current modulation imposed by the output of the AD537 back into a voltage signal suitable for driving digital logic; in the example shown the supply current down the line is as follows:

	OUTPUT "OFF"	OUTPUT "ON"
ZERO SIGNAL	1.2mA	5.2mA
FULL-SCALE (1mA)	3.5mA	7.5mA

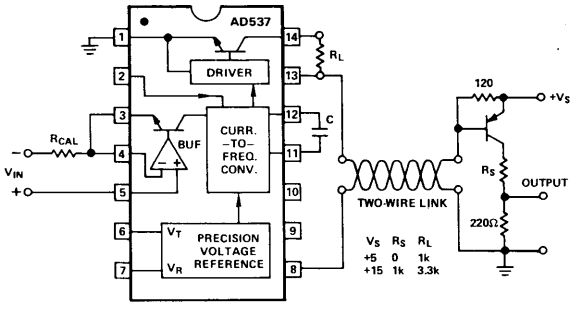


Figure 6. True Two-Wire Operation

The PNP circuit is designed so that the transistor is not appreciably turned on by the supply current to the AD537 in the "OFF" state; a large ratio of currents between FS/OFF and ZERO/ON ensures reliable operation. Where power considerations are of paramount importance a smaller value of FS control current can be employed and a more efficient means of detecting the modulation current would allow the use of a larger R_L. Approximately 500mV of variation appears on the remote end of the supply line; this does not affect operation of the AD537, due to its good supply-rejection ratio.

A useful feature of the AD537 in this application is the provision of a stable 1.00V reference output at the remote location, making it possible to drive various transducers requiring a stable supply. An example might be the conversion of linear position using a resistive-element transducer; other examples will be found later in these notes, including temperature measurement using the output at pin 6.

Signal Multiplexing

Where a variety of transducers, each of different type and sensitivity, and possibly other signal sources, are required to interface with a common data-acquisition system, one solution is the use of separate instrumentation amplifiers for each channel, driving an analog multiplexer which finally drives a V-F converter. The versatility of the AD537 allows it to operate directly from almost any signal source commonly encountered, and a more economic solution in some cases can result by using one V-F per channel and multiplexing their output digitally.

The open-collector feature of the AD537 makes this easy to implement. One method is shown in Figure 7; all V-F circuits are operating continuously, but only the device having its LOGIC COMMON pin grounded, through the open-collector decoder or other digital switching element, transmits its output. An alternative method uses the SYNC input (pin 2). In this method, all V-F's have pin 1 grounded, and all but one have pin 2 shorted to $+V_S$ (using a PNP transistor) which stops the oscillator circuit in these AD537's. This method has the advantage of reducing the risk of cross-talk between converters, but is less convenient to implement.

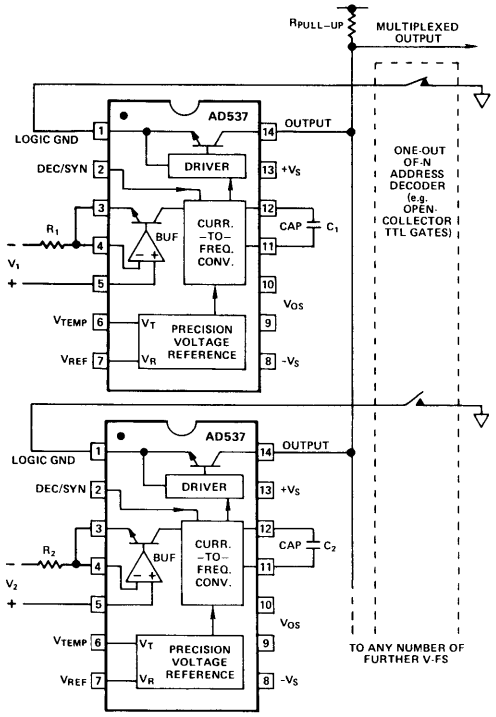


Figure 7. Signal Multiplexing

Two-Phase Output

Using two load resistors, one from the positive logic supply to pin 14 (output) and one from the negative logic supply

to pin 1 (supply ground), a two-phase output can be provided. Assuming equal resistors, and a typical situation where +5V and ground are used as logic supplies, the output at pin 14 is a square-wave from about +2.6V to +5V, and that at pin 1 goes from ground to about +2.4V and has the opposite phase. Unequal resistors can of course be used to alter the amplitude ratio of the two outputs.

Temperature Stability

The stability of the output frequency is determined by several factors. Broadly speaking, they can be grouped into offset drift and scale drift. The design of the AD537 is such that input offset drift is very small—in the 1μV/°C region—and unless the circuit is connected for operation from very low signal levels, this will rarely be a significant source of instability. Scaling drifts arise both in the AD537 itself—less than ±50ppm/°C for the AD537K—and in the external timing resistor and capacitor which must be of adequate quality for the application. In practice, it will be these external components which most seriously degrade stability over temperature; for most applications metal-film resistors are recommended.

Operation with Non-Zero TC

The drift induced by the external components can be corrected by introducing a deliberate drift of the opposite sign into the AD537. For example, if a particular resistor and capacitor cause the AD537 to exhibit an output frequency drift of 150ppm/°C, this drift can be corrected by connecting an 8.3kΩ resistor between the 1mV/°K output (pin 6) and $-V_S$ (pin 8). Other values, giving TC's of +20 to +350ppm/°C, can be found using the graph (Figure 8). Over this range the scaling factor is only slightly affected; the error is about +0.03% per ppm/°C. In the example the output frequency would be nominally 4.5% high, and this error can be allowed for when choosing the scaling resistor. It should be noted that this option also impairs the temperature-stability of the +1V output (pin 7).

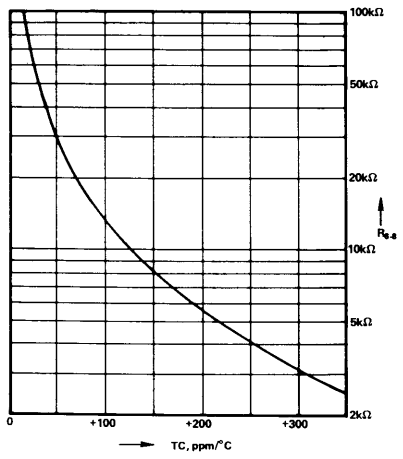


Figure 8. TC Versus R_{6-8}

Some Precautions

The AD537 is intended to be used with a minimum of additional hardware, and the circuits shown in these notes are for the most part complete. However, the successful application of an IC involves a good understanding of possible pitfalls and the use of suitable precautions.

Input Protection

Pins 3, 4 and 5 should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a resistor, R1 and a diode, D1 as shown in Figure 3. It is also desirable not to drive pins 3, 4 and 5 above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV for 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

The problem can be minimized by using a simple low-pass filter ahead of the converter. For a FS of 10kHz a single-pole filter with a time-constant of 100ms will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the probability that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package, as the SYNC function is not available.

Decoupling

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF are recommended for the AD537.

A decoupling capacitor may also be useful from pin 2 to pin 13 in those applications where very low cycle-to-cycle period variation (jitter) is demanded. The explanation is as follows: the voltage generated by the bandgap circuit is somewhat noisy, and this causes a jitter ratio of about one in 5000 (for example, a period uncertainty of 200ns at 1kHz). By placing a capacitor across pins 2 and 13 this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

III INSTRUMENTATION APPLICATIONS

Analog-to-Digital Conversion

A voltage-to-frequency converter is very useful as part of an analog-to-digital conversion scheme in many applications, for the following reasons. First, unlike converters based on binary-weighted networks, monotonicity is inherent under all supply and temperature conditions. A V-F with a nonlinearity of ±0.01% is thus roughly comparable to a 12-bit A-D with a worst-case differential linearity of ±1/2 Bit. Second, the fact that the signal is converted to a serial bit stream allows the simple analog part (the V-F) to be located close to the signal source, and the digital part (counter, timing gate, display) to be located centrally. As previously mentioned, many AD537's can be multiplexed on to a single transmission path, and share a single digital system. Finally, since the digital number is accumulated over a large number of cycles, integration of unwanted signals is inherent. In fact, the integration period is fixed by the gating interval, so that even for small inputs, when there may be only a few cycles to count, the same amount of signal integration is applied. Such a converter behaves as a filter with attenuation vs. frequency of

$$G(\omega) = \frac{1/\omega T}{\sin(1/\omega T)}$$

where ω is the angular frequency of the interfering signal and T is the digital gating time. Of course, the need to use a long gating interval is a basic limitation of all integrating A-D converters.

Figure 9 shows a typical scheme which delivers a 12-bit buffered output word and depends for its timing on an externally supplied clock. The small amount of logic required performs the reset-counter and load-latches functions automatically. No further control signals are necessary. Obviously, the clock can be generated by another AD537 if ratiometric measurements are to be made.

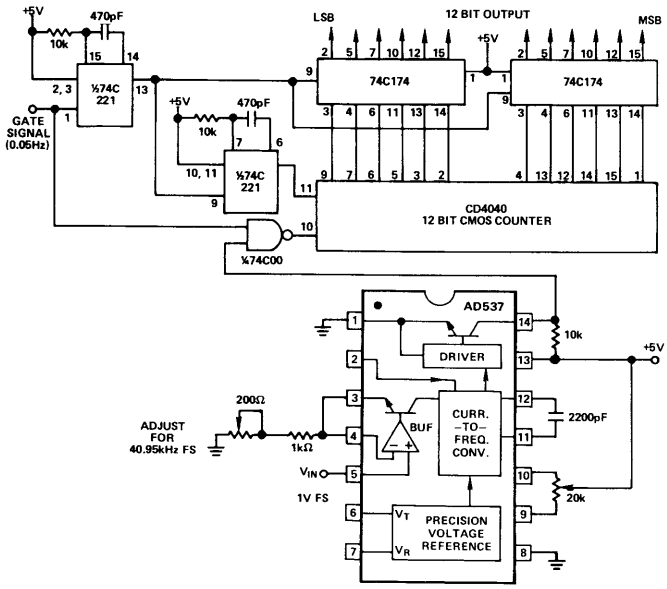


Figure 9. 12-Bit Analog-To-Digital Conversion

Accuracy

The absolute accuracy of an A-D converter using the AD537 will be much poorer than the linearity, since it is not fundamentally free from scaling drift. The scaling is a function of the internal reference voltage, the timing capacitor, the adjusted scaling resistor and the clock frequency, all of which are uncorrelated quantities subject to temperature- and supply-induced errors. An overall temperature stability of about ±100ppm/°C can be achieved in practice, comparable to that found in low-cost panel-meter DVM's.

Resolution

The resolution is determined primarily by the quantization imposed by the counting process, but there will also be a ±1 count uncertainty which can be troublesome for small inputs. This can be alleviated by adding several stages to the counter ahead of the first used stage, so that gating uncertainties are less apparent. Of course, to maintain the same scale, the V-F converter must operate at a higher frequency, and the trade-off in linearity may detract from the improvement in resolution.

Dynamic Range

The AD537 has a guaranteed dynamic range of 10,000:1, which is commensurate with a 13-bit quantization. In the example shown in Figure 9 the full-scale input of +1V generates a binary output of 111111111111 (decimal 4095) and the first bit occurs for an input of 244μV. To fully utilize this dynamic range it is necessary to null the input amplifier as described earlier under Basic Operating Modes.

Signal Isolation

V-F converters are useful for conveying signals between systems at greatly different potentials (for example, from the cathode of an electron microscope operating at several hundred kilovolts below ground) or for providing high-integrity isolation in equipment where ground currents would be hazardous (such as in medical instrumentation). Excellent special-purpose products are available for these requirements, usually in modular form, but in some cases the AD537 may offer an attractive alternative due to its low cost, low power consumption, high sensitivity and small size. Two basic points arise in these applications: first, the choice of the transmission medium; second, the provision of an isolated power supply.

Coupling Devices

The two most popular transmission mediums are magnetic and optical; a third choice, that of acoustical coupling, is applicable in some cases. Capacitive coupling is another possibility, although in many cases the large voltage between sending and receiving points, often accompanied by ripple and noise, excludes this approach. For illustrative purposes, a typical optically-isolated scheme is shown in Figure 10. To conserve power, the LED is driven at the relatively low level of 8mA, and one stage of gain is added on the receiving side. This circuit can operate at any frequency within the AD537 bandwidth and drive at least six standard TTL loads.

Isolated Power Supply

An ordinary 50/60Hz transformer-rectifier circuit can be

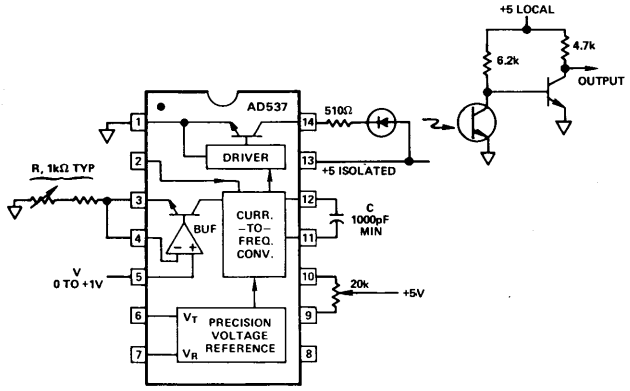


Figure 10. Typical Optical-Coupling Scheme

used to provide the floating voltage for the V-F converter. For high-voltage isolation, a toroidal transformer with an insulating bobbin should be used for the secondary. Alternatively, a dc-dc converter can be employed. However, in this case special care should be taken to ensure that all switching spikes from the dc-dc converter are completely filtered from the V-F circuit to prevent unwanted synchronization. Very little supply regulation is required; note that the current drain is nearly independent of frequency, simplifying the power-supply design.

Fiber-Optic Receiver

The output of a V-F converter is often transmitted over an optical-fiber cable for considerable distances, and detected by a photodiode at the receiving end. The photocurrents are usually small, and a preamplifier is necessary. Figure 11 shows a suitable circuit, having sufficient bandwidth to accept optical inputs up to 20kHz.

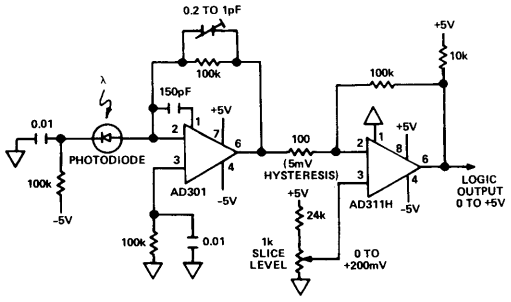


Figure 11. Photodiode Preamplifier

Handling Bipolar Inputs

The AD537 can handle signals of either polarity as has already been shown. Occasionally it is necessary to perform V-F conversion on a signal whose polarity is indeterminate. This can be achieved either by offset operation or by the use of an absolute-value circuit; both techniques will be described. Of course, the single-supply feature cannot be used in these circumstances. However, when the input is an alternating signal and it is only necessary to measure the average value, the AD537 can automatically perform precise half-wave rectification and operate from a single supply.

Offset Operation

By simply returning the timing resistor to a negative voltage (rather than ground), the V-F converter can accept negative and positive input signals, and generate a frequency

$$f = \frac{E_{IN} + E_O}{10V} \cdot \frac{1}{CR}$$

Clearly, the offset voltage E_O must have a magnitude greater than the most negative value of E_{IN}, and usually some overrange is desirable. Thus, a value of -12.5V might be used for E_O when the signal input has a full-scale range of ±10V. Figure 12a shows a simple implementation of this scheme, using the -15V supply as the offset source. To calibrate this circuit, first set the input to zero and adjust R1 for an output frequency of 10kHz. Then apply an input of +10V and adjust R2 for an output of 18kHz. This circuit has the advantage of retaining the high input resistance feature of the AD537. A disadvantage of this scheme is that the center-scale frequency is totally dependent on the -15V supply.

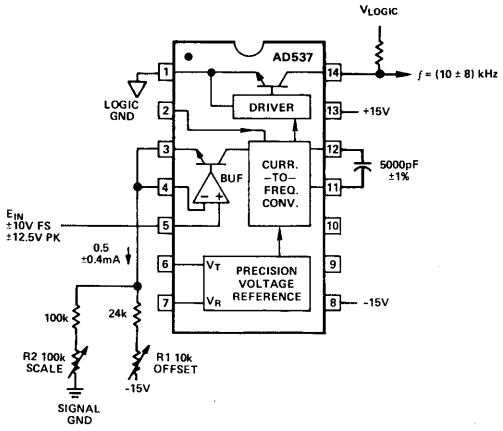


Figure 12a. Offset Operation, ±10V FS

A better arrangement is to make use of a stable reference element such as the AD589, as shown in Figure 12b. For the purpose of illustration a ±0.5V input range is shown. Calibration once again proceeds by first adjusting the zero-input frequency using R1 and then the +FS input using R2. Scaling for other operating conditions is straightforward.

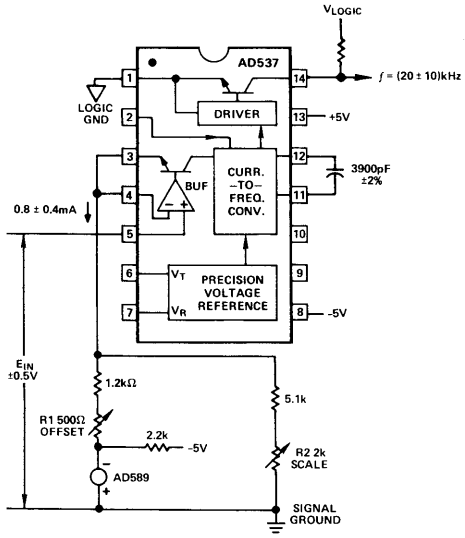


Figure 12b. Offset Operation, ±0.5V FS, Using AD589

Using Absolute-Value Circuit

In some cases the relatively large "zero-error" associated with offset operation may be troublesome. Also, the frequency data is inconveniently formatted if it is to be used for digital display. These problems are overcome by using an

absolute-value (precision full-wave rectifier) circuit ahead of the converter, with the bonus of effectively doubling the range of linear operation. By utilizing the high input resistance of the AD537 a very simple absolute-value circuit is possible (Figure 13). The circuit shown is scaled for an input of ±10V full-scale, but any voltage can be handled with appropriate change of scaling resistor. Similarly the full-scale frequency can be tailored to the application by changing the timing capacitor.

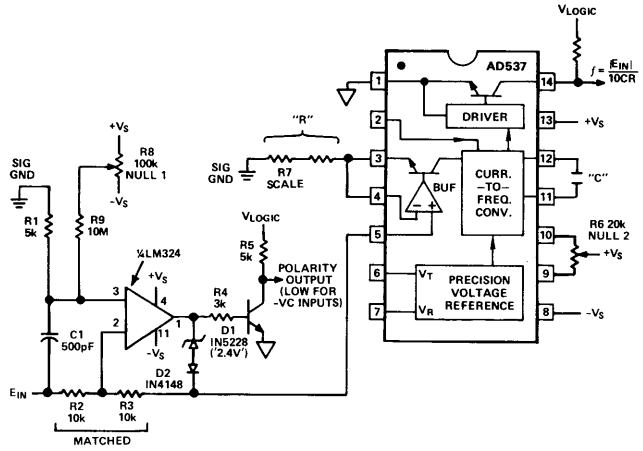


Figure 13. Bipolar Interface Using Absolute-Value Circuit

For positive inputs the op-amp is effectively disconnected since its output goes low and cuts off D2, and the signal is connected without attenuation or inversion to the input of the AD537 via 20kΩ. For negative inputs the op-amp output becomes positive and turns on D2 via the low-voltage zener D1, whose purpose is to ensure proper operation of the polarity detector. The input is thus inverted, so once again the AD537 receives a positive input. The output of Q1 is low for negative inputs, and it can be used to indicate signal polarity. (In a two-wire system such as described in Section II this information can be conveyed as a further modulation of the supply current, for example.)

For operation from a single supply an op-amp type such as the LM324 can be used. A dynamic latching condition can occur with this amplifier if the input switches abruptly. This is prevented by the addition of R1 and C1. These components can be omitted if the input is slowly-varying or if a standard op-amp type is used. The speed of this absolute value circuit is such that the input to the AD537 is "oscilloscope clean" for a 20V pk-pk sinewave or triwave input up to at least 2kHz. One caution to be noted is that the input resistance is unequal for positive and negative inputs, requiring either that the source resistance be very low (less than 10Ω for a 0.1% reversal error) or constant (in which case the error can be absorbed by subtracting this source resistance from R2. Full calibration requires the elimination of the op-amp offset by adjustment of R8. For most applications this can be achieved by simply grounding the input and observing the polarity output. Better accuracy can be achieved using a DVM to null the input to the AD537. After this step, calibration proceeds as for unipolar operation, except for the need to check the reversal error due to R2/R3 imbalance.

Measuring AC Signals

The AD537 only responds to inputs which cause pin 5 to be more positive than pin 4. For opposite-polarity inputs, no timing currents are generated. Thus, the device is inherently a half-wave rectifier with a very sharp "knee". This characteristic can be used to perform V-F conversion on an ac input signals without recourse to any further external parts. Filtering is automatically achieved by the integrating action of the timing capacitor for input frequencies above the instantaneous operating frequency. Of course, if the input has a period less than that of the oscillator frequency the output will be frequency-modulated, although in many cases further integration will be provided by the counters which often are used to measure the frequency. Examples of this mode of operation are given in Section V.

Transducer Interface

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly unlike many V-F converters which require signal pre-conditioning. The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer. Some examples of transducer interfacing are provided by way of suggestion; many others will be obvious.

Thermocouple Input

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678μV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices, *Nonlinear Circuits Handbook*, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 14 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400-700°C.

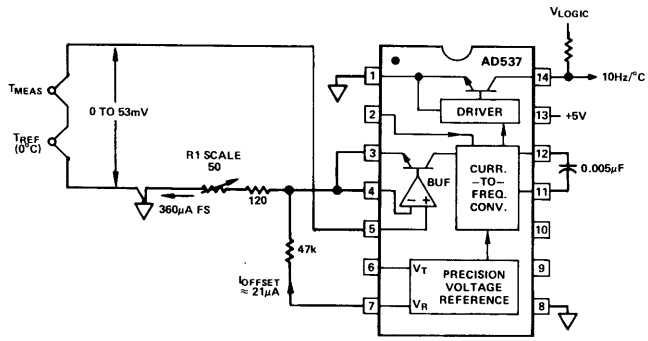


Figure 14. Thermocouple Interface with First-Order Linearization

Strain-Gauge Input

Depending on the application, the output of a strain-gauge consisting of a bridge of four resistors may be either unipolar or bipolar, linear or nonlinear. Thus, only an illustrative example can be given here. In all cases, the bridge requires excitation, and we here assume dc excitation using the 1.00V reference output buffered by an external op-amp (Figure 15). In this way, the calibration is not only independent of the supply voltage, but also very stable over temperature, since the same reference voltage (even though having a finite TC) is also used as the reference for the V-F section of the AD537.

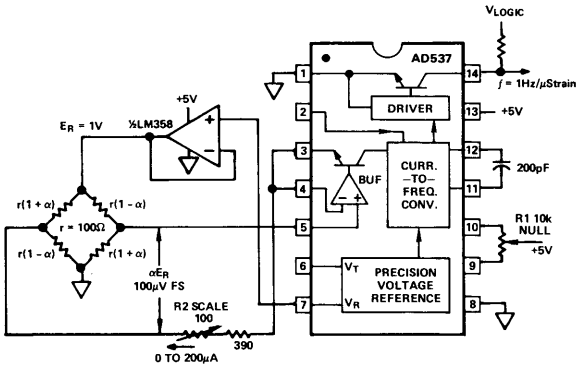


Figure 15. Typical Strain-Gauge Connections

This example assumes that the strain is always of the same polarity (unipolar operation) and that a balanced-force (linear) system is used. The timing resistor is returned to one side of the bridge, both to double the sensitivity and effect offset operation. This connection is capable of introducing a nonlinear error term, and we wish to determine its magnitude. Referring to Figure 16 it is evident that the current in the timing resistor (to which the frequency is proportional) is given by

$$I = \frac{\frac{1+\alpha}{2}E_R - \frac{1+\alpha}{2}E_R}{R + r\,\frac{(1-\alpha^2)}{2}}$$

This can be re-written

$$I = \frac{\alpha E_R}{R\left(1+\frac{r}{2R}\right)}\left\{1+\frac{r\alpha^2}{2R}\right\}$$

for typical small values of α, and this expression clearly reveals that a cubic error term results from this connection. In practice this error is tolerable. For example, for $R \geqslant 5r$ and $\alpha \leqslant 0.1$ the error is less than +0.1% absolute; if the system is calibrated at full-scale strain, this error is reduced to approximately **+0.025%** peak.

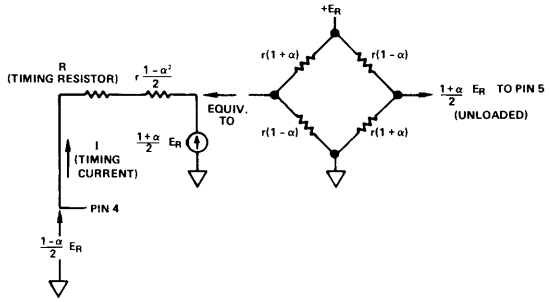


Figure 16. Circuit for Analysis of Nonlinearity

The circuit of Figure 15 is calibrated to generate a scale of 1Hz per microstrain (100kHz at the assumed FS value of $\alpha = 0.1$). Single supply operation allows this circuit to be located at the far end of a two-wire line, as previously discussed.

Position Transducers

Linear displacement transducers, rotary servopots, many kinds of level transmitters, light-comparators using photoresistors, etc. are readily interfaced with the AD537. In many cases it will be possible to use the reference output to power the transducer for greater accuracy and stability of scale. For track resistances down to 3kΩ this may be connected directly, as shown in Figure 17; however, the

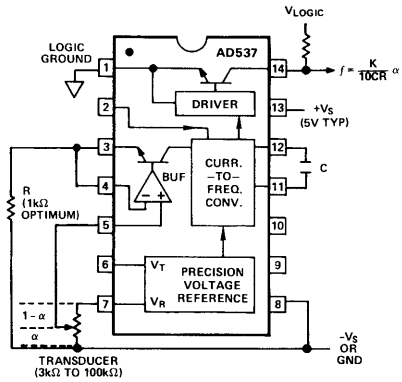


Figure 17. Resistive Transducer Interfacing

loading effects must be considered. First, the finite output resistance of the reference source (about 380Ω) causes the voltage across the track to be less than 1.00V, thus reducing the output frequency. Second, the track current flowing in pin 7 causes the voltage across the timing capacitor to be increased. This also decreases the frequency (by as much as 50% for a resistance of 3kΩ). The effect is quite predictable, and a scaling correction factor, K, can be applied; this is plotted in Figure 18. Alternately, a buffer amplifier can

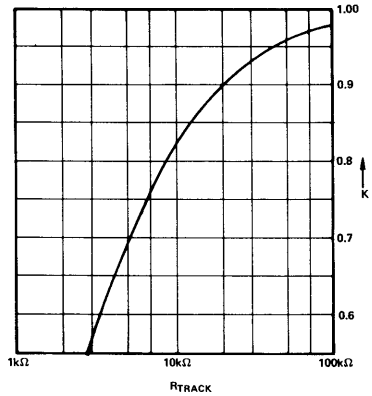


Figure 18. K-Factor Versus Track Resistance

be used, as for the strain-gauge driver shown in Figure 15, in which case no loading correction is necessary and much lower track resistances (down to about 100Ω) can be used.

Higher track resistances can also be used, up to at least 100kΩ. Above this value the parabolic error caused by the input bias current (about 100nA) at pin 5 may become troublesome. For example, at mid-position of a 100kΩ track, the error voltage is +2.5mV, or +0.25% of the 1V full-

scale signal. This problem is mitigated by using a larger excitation voltage or by including a low-bias op-amp buffer. This general configuration may also be used as a manually-adjustable clock generator needing a minimum number of components, having a wide frequency range with very linear control, and capable of operating from a TTL or CMOS supply rail.

Inverse-law operation may sometimes be desirable; that is, linear motion of the slider should result in linear control of the period rather than the frequency of the output. Figure 19 shows how this may be accomplished with good accuracy even when there is contact resistance to the slider. With the values shown, a range of 100:1 is provided, but the circuit is easily re-configured for other conditions.

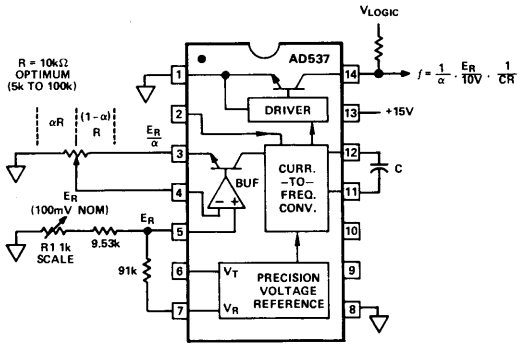


Figure 19. Linear Period Control

Photodiode Input

Some transducers, such as photodiodes and phototransistors, generate a current output and require an operating bias of a few hundred millivolts. Once again, the AD537 can provide the necessary interface conditions, as shown in Figure 20. The scaling accuracy will depend primarily on the stability of the phototransducer. It may be unnecessary to include provisions for scale adjustment; where justified, the scheme previously outlined for current-input operation is used as shown. Using a photodiode, the current will generally be small and direct interfacing may be impractical. A photoresistive (e.g. cadmium sulphide) cell may also be used.

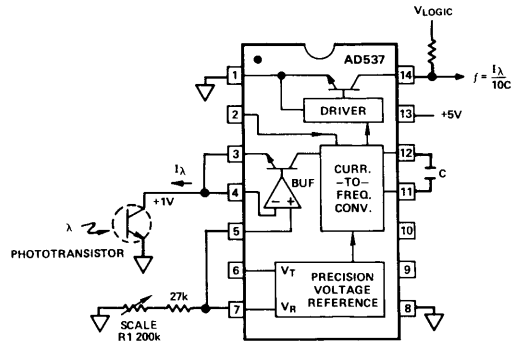


Figure 20. Phototransistor Interfacing

4–20mA Loop Operation

Various ways are available for converting instrumentation signals in the 4–20mA format to a frequency format. The choice will depend on whether the circuit is to be self-powered or powered directly from the current loop, and whether scale offset is to be introduced or not.

Externally-Powered

The method for converting the current-mode signal to a suitable voltage signal is trivial when no offset is needed and an external supply can be used. A somewhat more interesting problem is to provide offset in such a way that the output frequency is zero for a current input of 4mA. Figure 21 shows a suitable scheme, which makes use of the input amplifier sense terminal (pin 4) to introduce the offset.

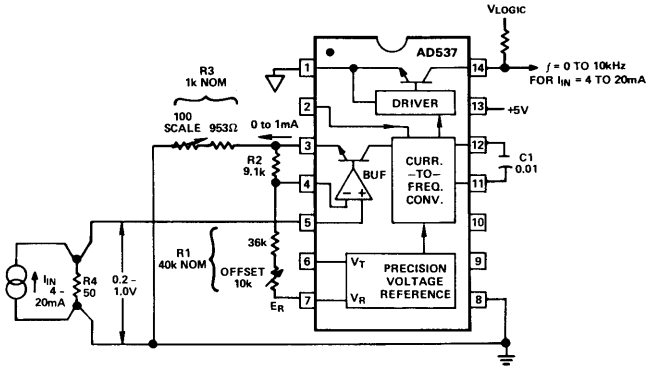


Figure 21. Offset Conversion of 4-20mA Signal

To understand the operation of this scheme, it should be noted that the offset voltage referred to the input is

$$E_O = E_R \frac{R2+R3}{R1+R2+R3}$$

The current in the timing resistor for values of E_{IN} above the offset is given by

$$I = \frac{1}{R3}\left\{E_{IN}\frac{R1+R2+R3}{R1} - E_R\frac{R2+R3}{R1}\right\}$$

Since the input is first converted to a voltage of 0.2 to 1.0V by the 50Ω load, an offset of 0.2V is required. For a nominal value of 1.0V for E_R this determines the ratio (R2 + R3)/(R1 + R2 + R3) = 0.2. The timing current, I, can be written

$$I = \frac{1}{R3}\cdot\frac{R1+R2+R3}{R1}(E_{IN} - E_O)$$

and for $E_{IN} - E_O = 0.8V$ at full-scale, we need

$$1mA = \frac{R1+R2+R3}{R1R3}\cdot 0.8V$$

for a 1mA full-scale current. This is only two equations, but there are three unknowns. A third requirement is that the loading on the reference output be light, 20μA for example. This determines the value of (R1 + R2 + R3) to be 50kΩ.

With these constraints, the resistor values can be calculated as shown. Note, however, that adjustment of offset and scale are unavoidably interactive, and the calibration procedure must be iterative.

Self-Powered Scheme

An interesting applications challenge is to find a way to use the signal current to also power the AD537. This is possible because the minimum value of 4mA is always greater than the quiescent current requirement of the IC. Even greater

utility results if the circuit can be optically coupled out, since the control loop then has complete isolation from the receiving system.

One approach is shown in Figure 22. Note first that there are two return paths for the signal current: through the main load resistor, R3, and through the timing resistor, R1 + R2. Since the current in the latter is exactly proportional to the load current in R3, linearity is preserved; even though the current gets used in a variety of ways by the rest of the circuit. The supply voltage is provided by the 5.6V zener diode, which together with the 1V full-scale voltage across R3 adds up to a worst-case compliance of 7V.

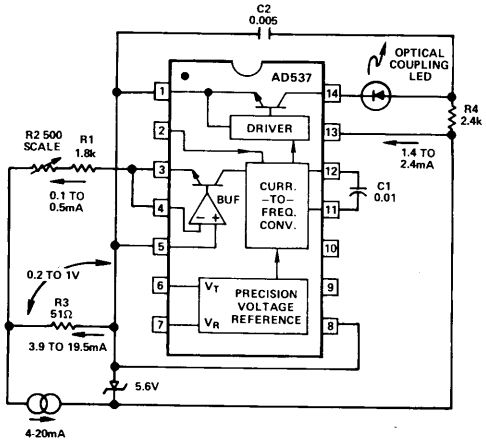


Figure 22. Isolated 4-20mA Converter

Each cycle the capacitor C2 is discharged through the LED at the peak current of approximately 25mA, internally limited in the AD537. The value of C2 is chosen to produce an optical pulse of about 1μs duration. The final diode current is limited to about 2mA by R4, calculated to ensure that even when the signal current is at its minimum value of 4mA there is at least 0.5mA in the zener; thus, the optical output persists at a lower level for a half-cycle. During the next half-cycle C2 recharges via R4, with a time-constant of 12μs, allowing full recharging in the minimum half-cycle time of 100μs.

In many cases the only calibration required will be to set the frequency to 5kHz at the full-scale input of 20mA. However, the V_{OS} of the AD537 may also be nulled for more exacting applications, using the standard technique described in Section I. Other scaling arrangements can readily be devised.

IV TELEMETRY AND COMMUNICATIONS

Frequency-Shift Modulators

A very common requirement is the transmission of binary data encoded as two discrete frequencies, for example, in data modems. The excellent temperature and supply stability of the AD537, its square-wave output and phase-continuous modulation property commend it as an alternative to semi-discrete implementations. Furthermore, its small power requirement allows it to be supplied from available telephone-line current at remote sites. Occastionally more than two levels can be encoded; these notes describe a binary modulator designed to Bell System 202 standards and an eight-level encoder.

Binary Encoder

Figure 23 is a schematic of an FSK encoder with a mark frequency of 1200Hz and a space frequency of 2200Hz. When the data input is low (mark condition) the timing current is supplied by R1. When the data input is high, Q1 saturates and the timing current is supplied by both R1 and R2. The inverted connection of Q1 ensures a very small offset error. Only one adjustment is needed; the voltage at pin 5 sets both mark and space frequencies. Note the very low current consumption of this circuit. The square-wave output must be filtered before transmission over a public telephone line.

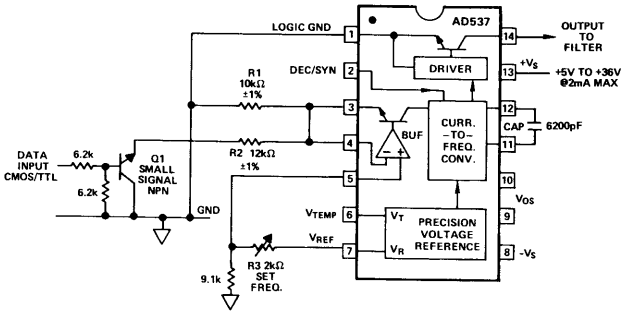


Figure 23. Bell System 202 Data Encoder

Eight-Level Encoder

A simple extension of the above circuit provides for the generation of eight linearly separated frequencies controlled by a 3-bit input word. Three inverted-mode transistors are used with collector loads of 1.8kΩ, 3.6kΩ and 7.2kΩ, which generate currents of 0.5mA, 0.25mA and 0.125mA respectively, when pin 5 is adjusted to 900mV. Using a 0.0125μF timing capacitor, this generates the frequencies zero through 7kHz. By adding a non-switched resistor (as in Figure 23) of 7.2kΩ, the frequencies 1 through 8kHz are generated. A more complex realization of digital frequency control is given under "Clock Generators" in Section V.

Phase-Locked Loops

The AD537 is useful as the VCO in phase-locked loops, due to its high linearity and the square-wave output. One application is as an accurate F-V converter; another is as an FSK demodulator. Both of these employ first-order loops. A linear phase-locked loop is also described, suitable for the recovery of signals buried in noise.

Basic F-V Converter

Figure 24 shows how the AD537 is connected for F-V conversion. The quad-nand open-collector TTL gate serves as a phase comparator, having as inputs the signal and the oscillator output. Its output is a rectangular pulse whose average value is forced to be equal to that voltage which causes the oscillator to run at the same frequency as the input. Since there is no low-pass filter, the circuit can lock on to any frequency from zero to full-scale (10kHz in this example), and this locked condition is acquired within four or five cycles. The dc output is extracted by a low-pass filter outside of the loop. As shown, the output has a FS value of +1V and is unbuffered.

The input duty cycle is not critical, but a square-wave is preferable. Pulses shorter than 50μs will cause errors.

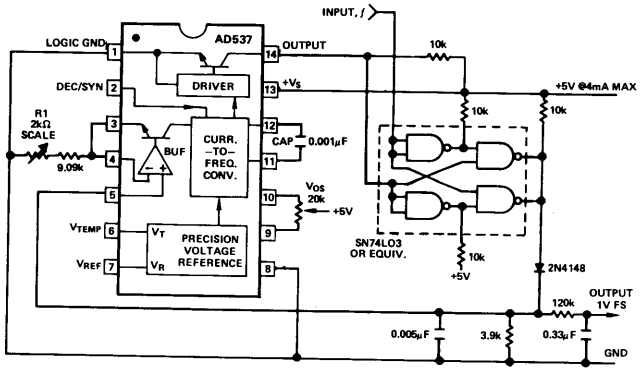


Figure 24. 10kHz F-V Converter

Similar trimming techniques as for V-F operation are employed. With the V_{OS} trimmer at mid-scale, trim the output to 1.00V for a frequency input of 10kHz using R1. Then apply a 10Hz input and trim V_{OS} for a 1mV output. Finally, re-trim R1 at 10kHz.

FSK Demodulator

For demodulation of a frequency-shift signal a narrower operating range is called for. Figure 25 shows a first-order loop similar to that just described, but operating only from 800Hz to 2600Hz. The center of this range is 1700Hz, which is also the center of the 1200/2200 Type 202 Data-set signal. The phase-comparator output is filtered by a simple low-pass circuit, suitable for data rates up to 120 baud. No trimming is required for this applications.

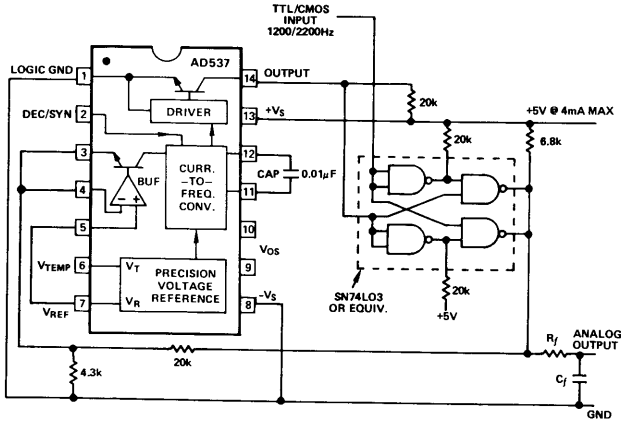


Figure 25. Bell System 202 Decoder

Linear PLL

The phase-locked-loop circuits described above operate from an essentially noise-free binary input. PLL's are also well-known for their value in extracting frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 26 the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It is easy to prove that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

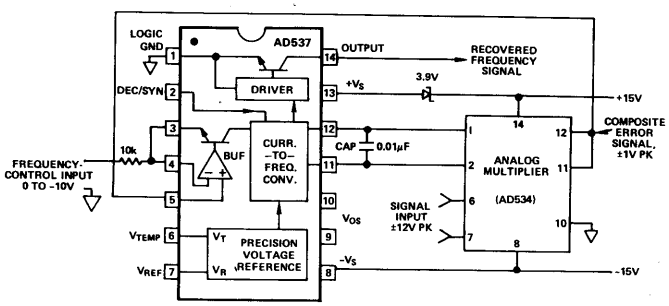


Figure 26. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 27 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

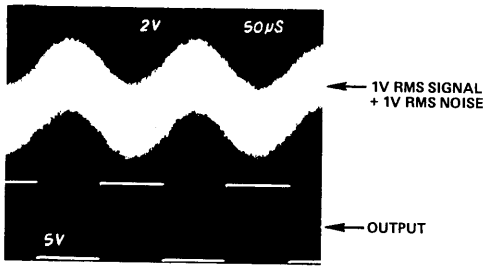


Figure 27. Performance of AD537 Linear Phase-Locked Loop

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

Waveform Generation

The AD537 combines many useful features as a waveform generator, including a very wide (10,000:1) control range with a single capacitor, cycle times up to 100 seconds (C=1μF), external voltage or current control, square-wave or triwave outputs. The capability for asymmetrical waveforms is also available.

Triangle Wave

The circuit shown in Figure 28 generates a loadable triwave output whose mark-space ratio can be set by adjustment of the factor α. For one half-cycle (when pin 14 is open-circuit), the only path for timing current is through R1; for the other (when pin 14 is short-circuit), both R1 and R2 are in

the circuit and the half-cycle is thus shortened. The mark-space ratio is maintained over the frequency-control range. Of course, if a symmetrical waveform is needed, R2 is omitted, releasing pin 14 for use as a square-wave output. The mark-space relationship can be inverted by reversing pins 1 and 3 on the AD521.

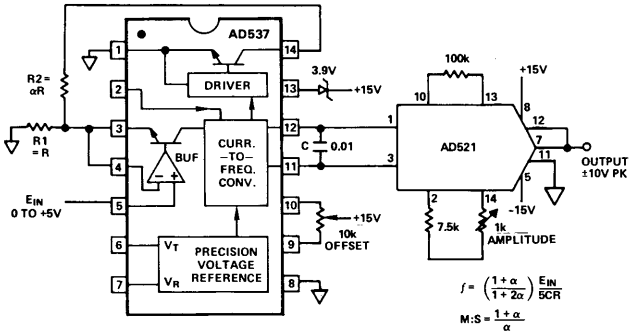
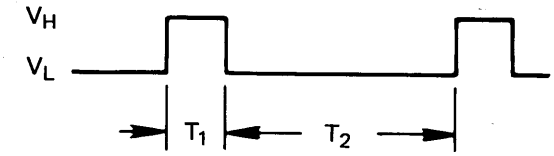


Figure 28. Asymmetric Triwave Generator

Note that the positive supply to the AD537 is reduced by the zener diode in order to remain within the common-mode range of the AD521 inputs. This also reduces the input signal range.

Voltage Programmable Pulse Generator

The circuit shown in Figure 29 produces a pulse train output with continuously variable output frequency, duty cycle, and output levels. The output waveform is shown below:



$$V_o = \begin{cases} V_H, \text{ for } T_1 = \dfrac{5RC}{V_1} \\ V_L, \text{ for } T_2 = \dfrac{5RC}{V_2} \end{cases} \qquad V_1, V_2 > 0$$

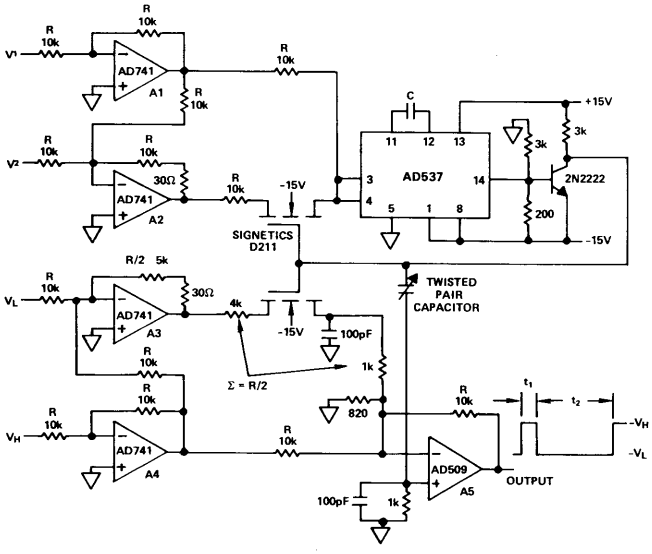


Figure 29. Voltage Programmable Pulse Generator

The circuit uses a 10kΩ timing resistor (R in the above formula), and the C value is chosen for the maximum square-wave running frequency. The minimum square-wave frequency is determined by circuit offsets. Frequency sweeps in excess of 1000 to 1 (corresponding to a 10mV to 10V range of V1 and V2) can easily be achieved. Additional range is possible by trimming offsets. The matching of the resistors around A1 and A2 will influence the accuracy of the duty cycle. If 0.01% resistors are used, a duty cycle sweep of 1000 to 1 with less than 10% error can be obtained. The 30Ω resistors shown in the feedback loops of A2 and A3 compensate for the R_{ON} of the FETs.

The output of the AD537 drives an external transistor which speeds up the transition and minimizes timing errors due to switching. The output amplifier, an AD509, is compensated slightly with the 100pF and 1k at the inputs. This results in a rise time of approximately 300ns with minimal overshoot and noise on the transitions.

Digitally Programmable Clock Generator

By combining a DAC with the AD537, digital control of frequency is achieved, using either an external binary word or manually-set thumbswitches. Figure 30 shows one realization using a 12-bit BCD-coded AD562 to provide 3-digit control of frequency from 100Hz to 99.9kHz.

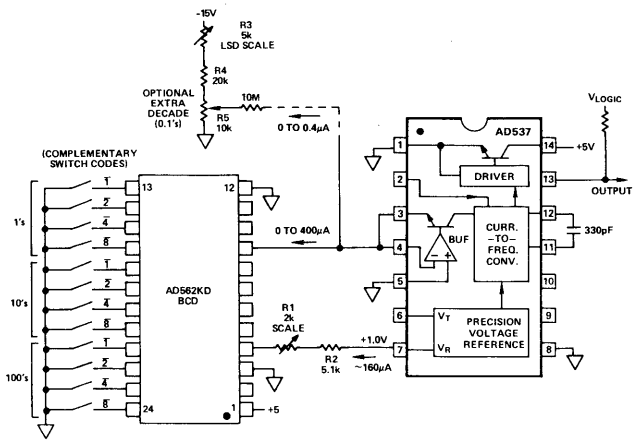


Figure 30. Digitally-Programmable Clock Source

The output current of the AD562 is used directly by the AD537, thus eliminating the need for a V_{OS} trim. Also, the reference output of the AD537 provides the AD562 reference input. This ratiometric operation contributes to overall stability. The DAC exhibits a current-gain of 2.5 at full-scale, so only 160μA of current is needed in the scale-setting resistors R1 and R2. If a straight-binary AD562 is substituted the FS output current is raised to 640μA, and the capacitor should be changed to 510pF for a nominal 100kHz FS.

Calibration is simple. With 999 on the thumbswitches adjust R1 for a frequency of 99.9kHz. The linearity of the AD537 ensures that all other frequencies are correct within the three-digit window. A fourth decade can be added in the LSD position as shown by the dotted lines.

Another digitally programmed clock generator is shown in Section VI of these notes.

V. SPECIAL APPLICATIONS

Long-Term Analog Integration

The integral of a unipolar input voltage is obtained simply by accumulating the output of an AD537 in a suitable counter:

$$N = \frac{1}{T}\int_{o}^{t} V(t)dt \quad , \quad T = 10CR$$

An analog output can be recovered using a DAC. Figure 31 shows a scheme using a 12-bit CMOS counter and a 10-bit CMOS DAC; the first two bits of the counter provide a prescaler, allowing the AD537 to run four times faster.

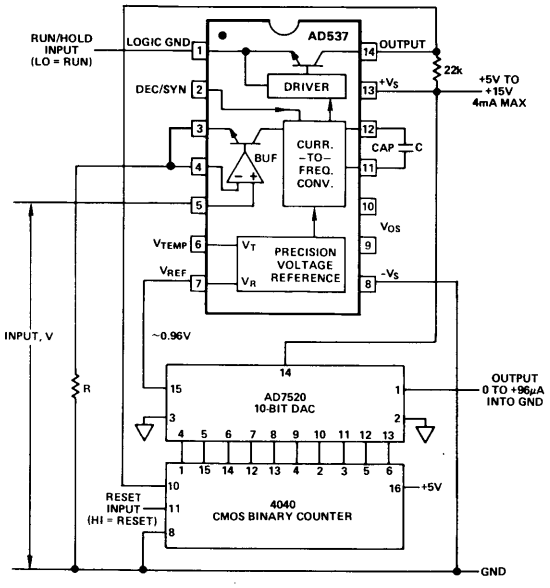


Figure 31. Long-Term Analog Integrator

Note that the 1.0V output of the AD537 is used as reference voltage, but the 10kΩ input resistance of the DAC loads this point, requiring a small correction in the output scaling, now nominally 96μA FS, and to the frequency adjustment which determines T. For a +1V analog input these values are recommended:

T	C	R	f(FS)
1 second	0.01μF	1.8K + 500Ω adj	4096Hz
1 minute	0.5μF	2.2K + 500Ω adj	68.27Hz
1 hour	10.0μF	6.8k + 1kΩ adj	1.138Hz

Longer integration constants should be obtained by interposing further prescaling counter stages ahead of the accumulator. Note that even when the AD537 is operating at low frequencies, wideband voltage fluctuations on the input are correctly integrated by the action of the timing capacitor.

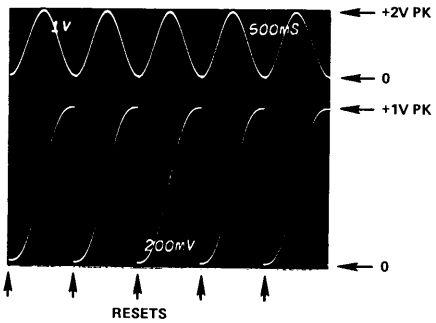


Figure 32. Output of Analog Integrator

Analog Division

In some cases it will be desirable to generate a frequency proportional to the ratio of two voltages. Of course, an analog divider may be used, but where the dynamic range of the denominator is fairly small (about 10:1) very good accuracy may be achieved using a few additional parts with the AD537. Figure 33 shows the scheme. First note that the numerator input voltage is applied to the usual input and scaling of full-scale input voltage and full-scale frequency is accomplished as in the standard modes. Positive inputs of up to (V_S - 4V) can still be accepted as well as negative voltages or currents. The division mode places no additional constraints on the numerator input.

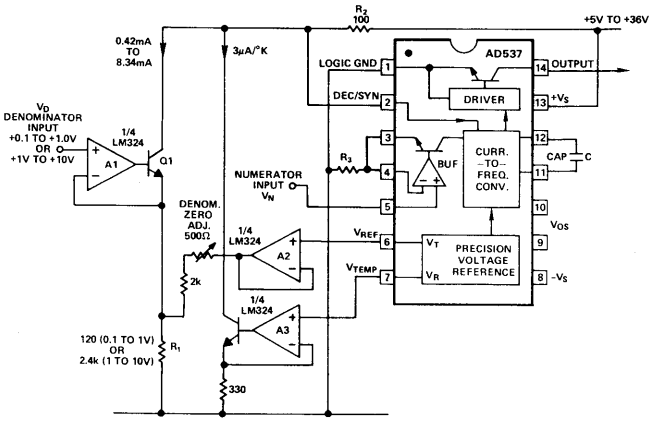


Figure 33. Analog Divider (Frequency Output)

Key to operation in this mode is the fact that the frequency is inversely proportional to the voltage between pin 2 and $+V_S$. Internally, this node has a resistance of 1.8kΩ to $+V_S$ and is supplied with a current of 460μA plus a further 50μA which is proportional to absolute temperature and is required to achieve temperature compensation of the basic current-to-frequency converter. By connecting an external 100Ω resistor, the control voltage at this node is reduced. This causes the nominal frequency to be raised by a factor of 19 times in the absence of any external current in this resistor. To restore temperature-independent operation, it is first necessary to supply 3μA/°K to this node. This is achieved using the thermometer output, the op-amp A3 (one-quarter of an LM324, chosen for its ability to operate from a single supply) and the transistor Q2 (any high-gain NPN). To provide conversion of the denominator signal to a voltage at pin 2 requires two steps: scaling and offset. Scaling for either +0.1V to +1.0V or +1.0V to +10V is demonstrated in the figure; the actual range extends considerably beyond the limits in both directions. Offset is necessary because there is a finite voltage at pin 2 even for zero denominator input, and this is provided by the stable +1.0V reference output. A2 buffers this voltage and A1 provides a high-impedance input point for V_D, the denominator signal. For R1 = 2.4K the output frequency is simply $V_N/V_D CR_3$. To adjust the denominator offset, connect the V_N and V_D inputs together (if they have same FS scaling voltage) and trim to maintain frequency independent of input voltage. Linearity of division is typically ±0.1%.

Temperature-to-Frequency Conversion

The 1mV/°K output of the AD537 is very exactly propor-

tional to absolute temperature, and the specified scaling error of ±0.1% can be absorbed in the overall scale adjustment. By operating at $+V_S$ = 5V and using small timing currents, the chip dissipation can be held to 6.5mW. This results in a temperature offset in free air of about +1°K, roughly equal to the typical input amplifier offset (since 1mV = 1°K). Accuracy in the absolute scale is therefore very high. Figure 34 shows the AD537S scaled for 10Hz/°K, corresponding to an output frequency range of 2180 to 4980Hz over the specified temperature range of -55°C to +125°C. For applications where ambient temperature is to be monitored, calibration to useful accuracy can be achieved by simply measuring the temperature at the package and adjusting the output accordingly. For more precise applications calibration at least two points (e.g., 0 and 100°C) will be necessary to eliminate offset effects.

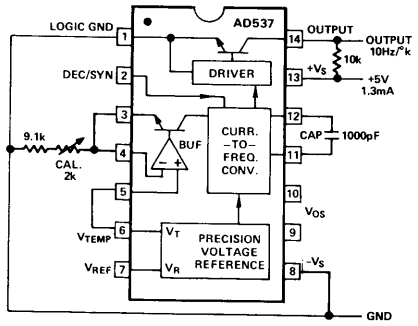
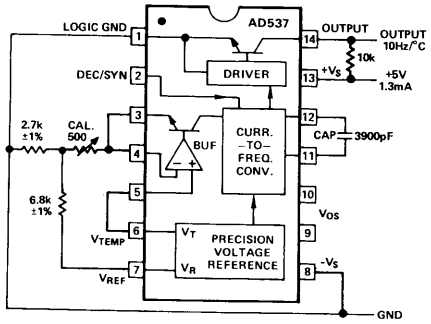
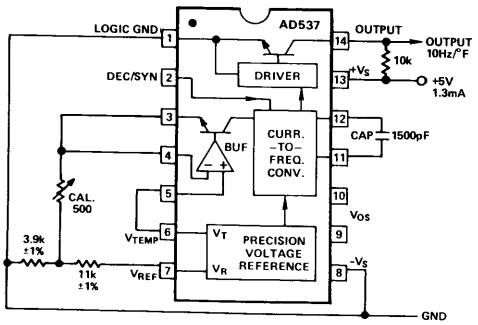


Figure 34. Absolute Temperature Transducer

The 1.00V output of the AD537 may be combined with the 1mV/°K output to realize other temperature scales. For the Celsius scale the lower end of the timing resistor must be offset by +273.15mV. Figure 35a shows how this can be achieved. The component values include corrections



a. Celsius



b. Fahrenheit

Figure 35. Connections For Offset Temperature Scales

for the loading of the 1.00V output. The frequency range is reduced to 0 to 1250Hz, corresponding to 0 to +125°C.

The Fahrenheit scale requires an offset of +255.37mV, and suitable component values are shown in Figure 35b. The output frequency range is now 0 to 2570Hz for a temperature range of 0 to 257°F (-17.78°C to +125°C). As for the absolute scales, satisfactory calibration is possible by adjusting the frequency to correspond to one locally-measured test temperature.

It should be noted that only the AD537S will perform to +125°C. For applications requiring a maximum temperature of +70°C (+158°F), the J or K grade can be used. The circuit values remain unchanged.

Sound Velocity Monitor

The thermometer and reference outputs of the AD537 can simplify the computation of many physical parameters. As an example, the velocity of sound in air can be computed from the formula:

$$V_S = (331.5 + 0.6T_C)$$

$$= (167.6 + 0.6T_K)$$

where V_S is velocity in m/sec
T_C is Celsius Temperature
T_K is Kelvin Temperature

The circuit of Figure 36 uses two resistors to provide the appropriate weighing of the thermometer and reference outputs as given by:

$$\left(\frac{R_2}{R_1+R_2}\right)1V + \left(\frac{R_1}{R_1+R_2}\right)\ 0.001V/°K = 167.61 + 0.6T_K$$

Thus, $\frac{R_2}{R_1} = \frac{167.61}{600}$. If we choose a value of 20k for R_2, then R_1 = 71.5k.

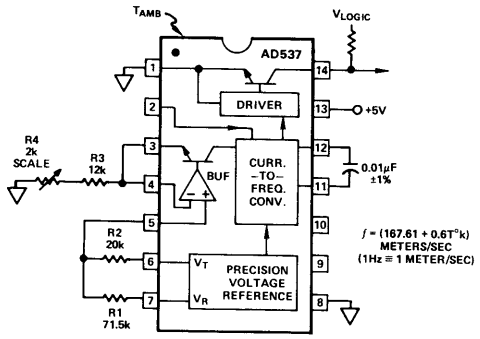


Figure 36. Sound Velocity Monitor

With these values, the voltage on pin 5 will be 452.8mV at 300°K. This must be scaled to an output frequency of 347.6Hz, corresponding to the velocity of sound at 300°K. If a 0.01µF timing capacitor is chosen, the value of R3 is found to be 13kΩ.

VI. MICROPROCESSOR INTERFACING

The AD537 is well suited to microprocessor interface applications due to its low cost, small physical size, and low power requirements. The device can be used as an output port, allowing software control of oscillator frequency, or it

can be used as the basis for a microprocessor-based data acquisition system.

Programmable Frequency Source

Figure 37 shows a circuit using an AD7522 10-bit CMOS digital-to-analog converter and an AD537 in a programmable oscillator circuit. The AD7522 is directly microprocessor-compatible and can be treated as either two output ports or two memory locations. Two locations are required to load 10 bits from 8-bit bus structures. The low order 8 bits are loaded into the DAC holding register on the rising edge of LBS, and the two most significant bits are loaded on the rising edge of HBS. The HBS signal is also connected to LDAC, which strobes the complete 10 bit word onto the actual DAC control lines coincident with loading of the two most significant bits.

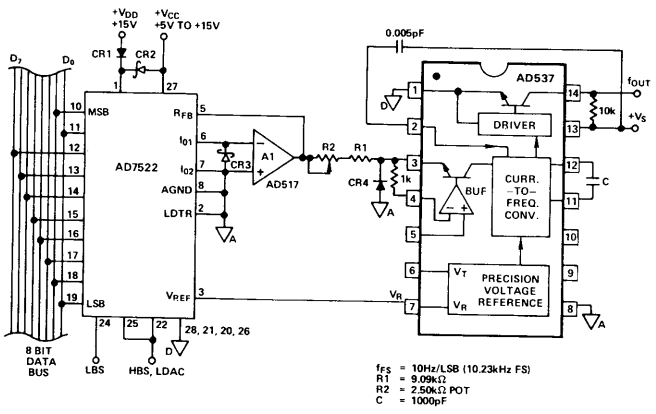


Figure 37. Digital Frequency Control from Microprocessor Bus

The reference for the AD7522 is provided by the 1.00V output of the AD537. The 10kΩ nominal impedance at the DAC reference input will lower the full-scale frequency of the AD537 due to loading on the 1.00 volt output (see Figure 18). Resistor R2 provides sufficient trim range to compensate for this effect. The DAC current output is converted to a voltage by the AD517, chosen for its low offset voltage and low drift. This voltage has a range of 0 to -1 volt F.S. and is applied to the AD537 configured for negative input voltage. As shown, the output frequency is scaled for 10Hz/LSB.

Data Acquisition

In microprocessor-based systems, a V-F converter is often used as a data-conversion element. The AD537 in particular can be used in systems requiring remote sensors reporting to a central processor. The serial outputs of many devices can be easily multiplexed, providing multiple-channel data acquisition at low cost.

The classic A-to-D conversion with a V-F converter involves using a series of counters to count pulses from the converter in a particular time interval. This gate signal must be, of necessity, quite stable, since any drift will cause a gain error in the conversion. Many microcomputers utilize a crystal oscillator for the system clock, and this can be used as the basis for a stable gate signal. Since most processor clocks run at a few megahertz, a divider stage will be necessary to provide a sufficiently long gate interval (usually a few hundred milliseconds). The gate frequency can, of course, also be derived from another AD537, in which case it can be adjusted to provide proper gate signals for several other AD537's operating at different full-scale frequencies.

If the parameter being measured is actually the denominator of the desired result, the role of the AD537 and the processor clock can be reversed. The AD537 output is used as the gate, and pulses of the system clock are counted. In this scheme, the total number of pulses counted bears an inverse relationship to the voltage at the AD537 input, relieving the microprocessor of the task of division. This type of conversion takes less time for a given level of resolution, since the processor clock runs much faster than the AD537 maximum frequency.

Figure 38 shows a generalized microprocessor data acquisition system using the AD537 as the basic analog-to-digital conversion element. The eight AD537's can be located some distance from the processor and linked by two-wire lines.

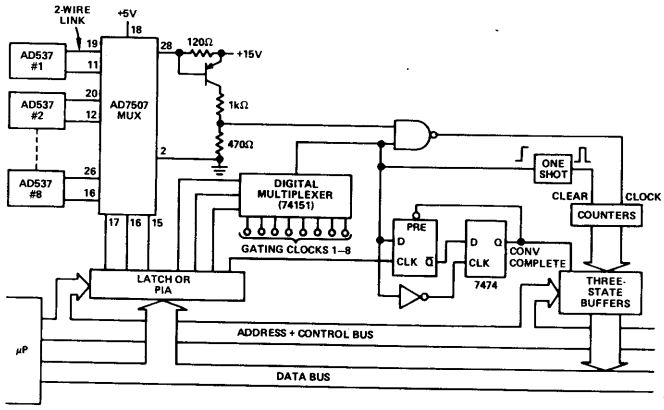
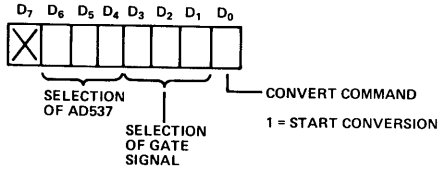


Figure 38. 8-Channel Microprocessor Data Acquisition System Using AD537

A single "write" instruction selects the AD537 to be monitored, the gating clock to be used, and issues the command to initiate a conversion. This byte might, for instance, use the following format:



The AD537 to be monitored is selected by the AD7507 analog multiplexer. The level shifter stage converts the current modulation to TTL-compatible pulses as described in an earlier section. A +15 volt supply is suggested, to compensate for the voltage drop due to the ON resistance of the multiplexer. The gating clock is selected by the 74151 digital multiplexer. As shown, any of the gate signals can be used on any of the input AD537's. This permits selectable gain ranging or shortened conversion times for measurements not requiring full resolution. If only one clock is to be used for each V-F channel, then both multiplexers can share the same selection bits.

The rising edge of the gate signal triggers a one-shot of minimal pulse width to clear the counters at the beginning of the conversion. The two flip-flops provide a definite "conversion complete" signal, based on the state of the gate signal at the beginning of the conversion. The gate signal itself is a poor indicator of status, since a conversion may be initiated while the counters are running. The first conversion would then be inaccurate. However, the logic shown provides a clear indication of status. This flag can be read as a memory location, or it can signal an interrupt to the processor.

The latches, buffers, and bus structures have deliberately not been specified. The choice of these components is dependent upon the particular microprocessor used, system configuration, and so forth. The actual implementation is left to the designer, and it is hoped that these notes have provided some insight into the practical considerations of data acquisition with the AD537.