ANALOG DEVICES

AN-280
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Mixed Signal Circuit Techniques

Introduction

There are considerably more problems involved in the successful design of Mixed Signal circuitry than mere circuit design. If we design an electronic circuit as a diagram, whether we use an old-fashioned pencil and paper or, as is the modern fashion, a computer and SPICE or some similar software, we are overlooking one of the most important factors in the design of successful hardware, namely that what we are designing is HARDware, and until it has been shown to work successfully in fact, rather than in simulation, our design is not complete.

This section of our seminar considers the problems which arise when reality reacts on a design which theory and modelling have shown to be satisfactory. What, in fact, has happened is that our model probably does not consider the effects of non-ideal components and of spurious or parasitic components resulting from the circuit layout which has been used. It is not, perhaps, too fanciful to describe this as the section of the Seminar dealing with Murphy's Law.

MURPHY'S LAW

IN ANY SET OF CIRCUMSTANCES THE WORST THING THAT CAN HAPPEN - WILL

- **Any effect which you think can be disregarded, can't.**
- **Nature always sides with the hidden flaw.**

Figure 11.1

Murphy's Law, though frequently expressed humorously, is not entirely a joke. It is a recognition of the complexity of physical systems and a warning against over-simplification and is comparable with Einstein's warning that "Everything should be made as simple as possible - but no simpler".[1]

IMPORTANT COROLLARIES TO MURPHY'S LAW

- **After it has worked successfully for two weeks it will fail during the first public demonstration.**
- **Equipment blows to protect fuses.**
- **Interchangeable parts aren't.**
- **Fail-safes don't.**

Figure 11.2

This section of the seminar discusses the various physical effects which must be considered in the design of the hardware of mixed signal systems. Often such consideration will amount to a quick calculation to demonstrate that further consideration is not necessary, but sometimes extensive analysis, or even actual experiments, will be necessary. However, the quick calculation must not be omitted, since problems are rarely obvious and often unexpected. The effects which must be considered will include many basic laws of physics.

BASIC LAWS INVOLVED IN THE DESIGN OF MIXED SIGNAL CIRCUITRY

- **Ohm's Law**
- **Kirchoff's Law**
- **Faraday's Laws**
- **Lenz's Law**

Figure 11.3

BIT SIZES FOR 10 V FULLSCALE CONVERTERS

RESOLUTION	1 LSB	0.5 LSB	% FS	ppm FS	dB FS
4-bit	625mV	313mV	6.25	62500	-24
6-bit	156mV	78mV	1.56	15625	-36
8-bit	39mV	19.5mV	0.39	3906	-48
10-bit	9.76mV	4.88mV	0.098	977	-60
12-bit	2.44mV	1.22mV	0.024	244	-72
14-bit	610μV	305μV	0.0061	61	-84
16-bit	153μV	76μV	0.0015	15	-96
18-bit	38μV	19μV	0.0004	4	-108
20-bit	9.5μV	4.8μV	0.0001	1	-120
22-bit	2.4μV	1.2μV	0.000024	0.24	-132
24-bit	0.6μV	0.3μV	0.000006	0.06	-144

Figure 11.4.

We therefore shall use as a section heading the major phenomenon considered in the section, but in the most general sense (for example, under "Resistance" we shall consider the non-ideal behavior of resistors, including noise, thermo- electric and inductive effects, which are not strictly issues of Ohm's Law).

When considering the effects of circuit conditions we are, of course, interested in their effects on the performance of the system as a whole. Failure to allow for this is at the root of many of the problems which this section considers. For example, a 16-bit system divides its full-scale (FS) range into 2^{16} or 65536, which means that 1 LSB in a 10 V FS system is only 153 μV. If we assume that we can tolerate errors of no more than 0.5 LSB, this calculation tells us that in a 16-bit system with 10 V FS we must keep the total error to less than 76 μV, which is approximately equal to the thermoelectric voltage in a nichrome wirewound resistor with copper/nickel leads having about 2°C temperature difference between its ends.

Binary logic circuitry, on the other hand, has only two states, logic 0 and logic 1, and noise immunity of hundreds or thousands of millivolts. This is why circuit designers who have only worked with digital circuitry tend to overlook the sources of error which we are considering in this section of the seminar.

Figure 11.4 lists the sizes of 0.5 LSB at various resolutions (the values are given for 10 V fullscale since this is a classical converter range and where LSBs are given a mV value in this section of the seminar a 10 V FS is assumed unless explicitly stated otherwise - scaling to other values of FS is a trivial operation). Every analog designer should be familiar with this table, since not only does it allow the comparison of converters which are specified in different ways but it also indicates whether a design is reasonable or not - if noise or system errors amount to 1 mV there is little point in designing a system with more than 12-bits resolution.

Resistance

Resistance of Conductors

Every engineer is familiar with resistors - little cylinders with wire ends - although perhaps fewer are aware of all their idiosyncrasies. Far too few engineers consider that all the wires and PC tracks with which their systems and circuits are assembled are also resistors.

At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard (1 ounce) PCB foil is 0.038 mm (0.0015"). The resistance of standard PCB copper is therefore 0.45 milliohms/square, which implies a resistance for the 0.25 mm track frequently used in computer designed digital circuitry of 18 milliohms/cm, which is quite large. Moreover the temperature coefficient of resistance for copper is about 0.4% /°C around room temperature, which can be a further inconvenience.

As an illustration of the effect of PCB track resistance consider a 16-bit ADC with a 5k ohm input resistance which has 5 cm of 0.25 mm PCB track between it and its signal source. This track has a resistance of approximately 0.09 ohms and introduces a gain error of 0.09 ohms / 5000 ohms (0.0018%) which is well over 1 LSB (0.0015% for 16 bits).

PRINTED CIRCUIT BOARD TRACK RESISTANCE

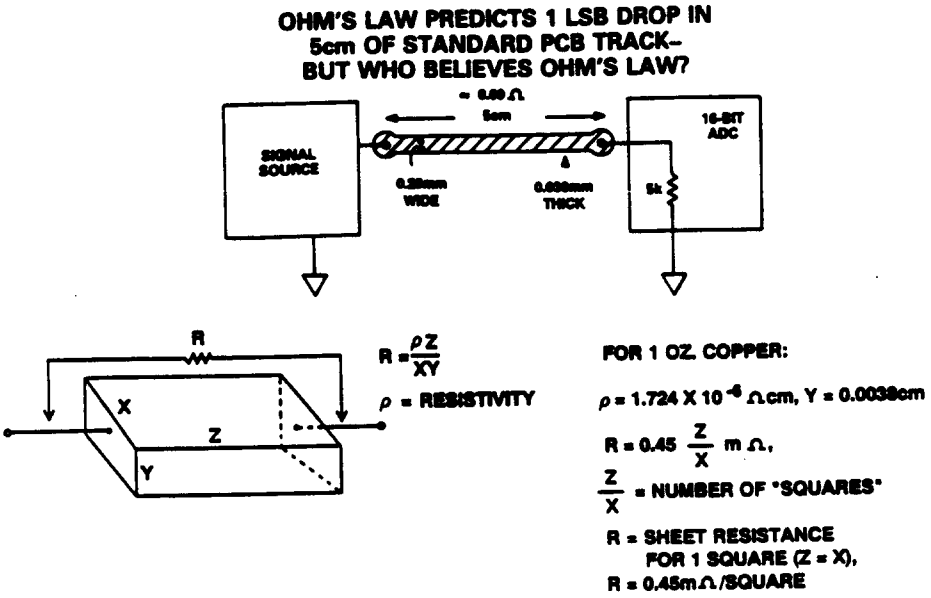


Figure 11.5

Skin Effect

This, of course, is a DC effect. At high frequencies we must also consider the "skin effect" where inductive effects cause currents to flow only in the surface of conductors. This has the effect of increasing the resistance of a conductor at high frequencies (note that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased - that will be dealt with later). Skin effect is quite a complex phenomenon and detailed calculations are beyond the scope of this seminar. However a good approximation for copper is that the skin depth in centimeters is

$$\frac{6.6}{\sqrt{f}}, \text{(f in Hz)}.$$

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the PC foil this tells us that for normal 0.038 mm PC foil we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important the resistance per square for copper is

$$2.6 \times 10^{-7} \sqrt{f} \text{ Ohms per square, (f in Hz)}$$

When calculating skin effects in PCBs it is important to remember that current flows in both sides of the PC foil (this is not necessarily the case in microstrip lines) so the resistance per square of PC foil is half the above value.

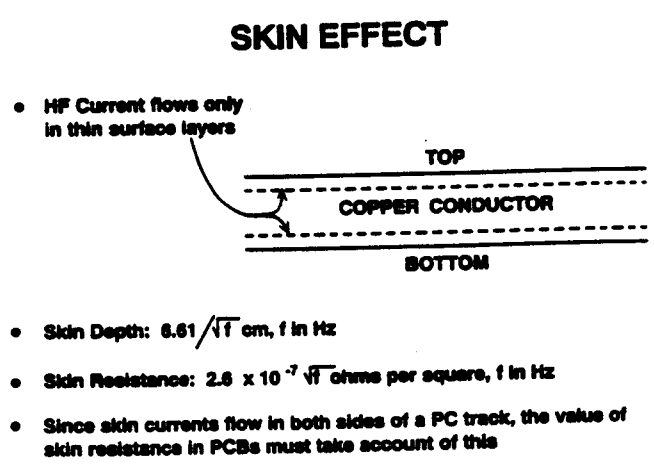


Figure 11.6

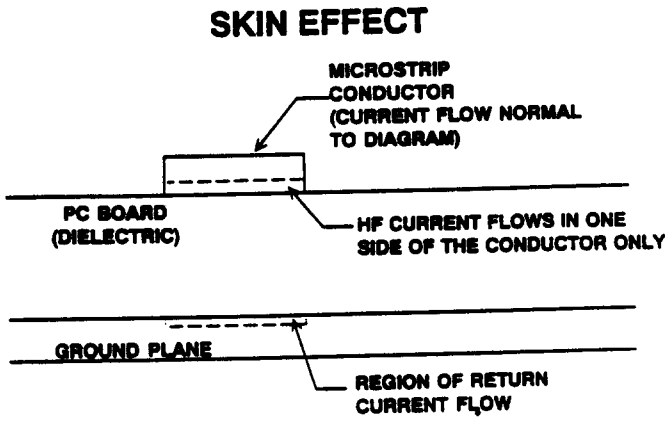


Figure 11.7

VOLTAGE DROP IN SIGNAL LEADS - "KELVIN" FEEDBACK

The gain error resulting from resistive voltage drop in signal leads is important only at high resolutions (as in the example) or where large signal currents flow. Where the load impedance is constant and resistive it can be compensated by adjusting the overall system gain. In other circumstances it may often be removed by the use of "Kelvin" or "voltage sensing" feedback.

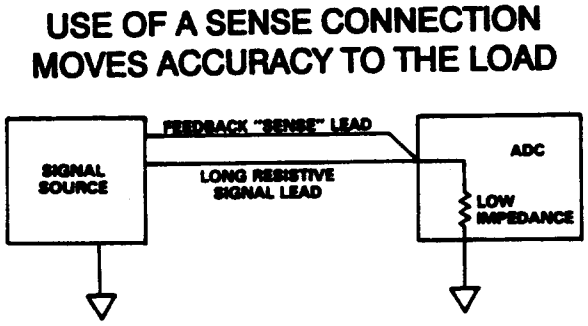


Figure 11.8

Separate force and sense connections at a load remove any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy since feedback may only be taken from one point.

LEAKAGE IN INSULATORS

Just as conductors are improperly viewed as superconductors, so are insulators often mistakenly treated as perfect insulators, rather than very high resistances, which is the more accurate model.

Most printed circuit board materials are very good insulators, but they are not perfect, and inadequately cleaned PCB material may be quite a poor insulator. Furthermore, PCBs are anisotropic - even on a clean PCB different parts of the surface may have different resistivities, and the bulk resistance (between two plated through holes, for instance) is generally lower than the surface resistance between two tracks.

Since the insulation resistance is so variable (and it will vary further with temperature and humidity) it is hard to predict in any particular circumstances but it is safe to assume that it is unlikely that the resistance between two conductors on a clean PCB will drop below 10^{10} - 10^{11} ohms, and with teflon PCB material (which is very expensive) will usually be over 10^{12} ohms.

GUARD RINGS

In applications where high impedances and very low currents are involved a guard ring may be used to minimize the effects of low insulation resistance. If critical high impedance nodes are surrounded by a ring of conductor which is at (or very close to) the potential of the node itself then the leakage current at the node will be minimized. If the node is at, or near to, ground then a grounded guard ring will be appropriate, if it is at some other potential it may be necessary to use a high input impedance buffer amplifier, with its input connected to the node, to force the guard ring to the node

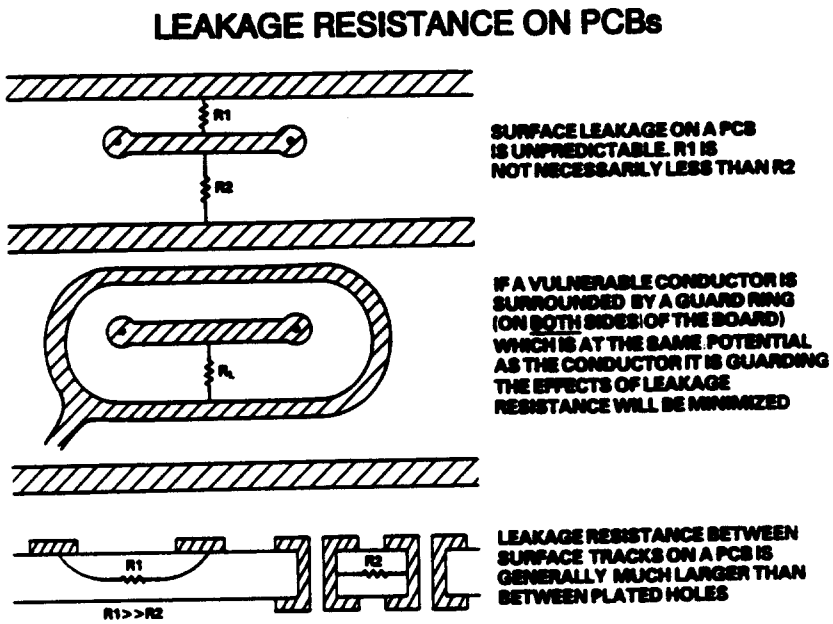


Figure 11.9

potential. It is obvious that, in general, guard rings should be on both sides of the PCB with plated-through holes.

Nodes which are sufficiently sensitive to require guard rings should not contain plated through holes (unless the PCB is made of teflon) because, as mentioned above, the bulk resistivity of PCB material is less than the surface resistivity.

An alternative to the use of a guard ring is to use teflon stand-off insulator(s) to support the high impedance point(s). If virgin teflon is used insulation resistance of around 10^{15} ohms is possible ("Virgin teflon" is a solid piece of new teflon material which has been machined to shape and has not been welded together from powder or grains). The material of the rest of the circuit board need not have particularly high insulation resistance.

A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK

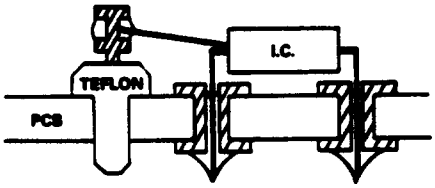


Figure 11.10

Electrostatic Damage (ESD)

Where resistances are very high, especially in conditions of low humidity, there is always the possibility of electrostatic charge and electrostatic damage. A full discussion of electrostatic damage (ESD) and its prevention will be found in Analog Devices' Application Note on the subject, which is available free of charge from Analog Devices.[2]

This application note describes procedures to minimize the risk of electrostatic damage to sensitive devices. The basic principle of all ESD protection is to prevent a vulnerable item from being in the path of a discharge. Many of the precautions used in factories are designed to minimize the possibility of any damaging discharge, even in the event of carelessness. When experienced engineers handle ICs they may dispense with most of the ESD protection apparatus and merely ensure that the IC is never in any potential discharge path: when taking a circuit from conductive foam, touch the foam to equalize charge before touching the circuit, similarly touch the foam with the hand before inserting the circuit in it, and hold your colleague's hand BEFORE passing the IC.

ELECTROSTATIC DISCHARGE (ESD)

ESD
PREVENTION MANUAL

ANALOG DEVICES

Figure 11.11

All integrated circuit structures are vulnerable to damage from the high voltages and high peak currents involved in even small electrostatic discharges but precision analog circuits suffer from a special disadvantage - the circuitry used to protect integrated circuit structures from ESD can often degrade the analog accuracy of the circuit where it is employed. Thus we have the choice between high performance and a high degree of protection. Which we choose will depend upon individual circumstances but it is essential to realize that the choice must be made - and if it is made in favour of accuracy then the circuit involved must not be exposed to electrostatic discharge.

A precision analog circuit exposed to ESD may not fail totally, but merely suffer degradation of its analog performance, and possible reduction of life expectancy. When an IC is returned to Analog Devices for failure analysis of inadequate performance the first check that is made when the package is opened is a visual inspection for evidence of electrostatic damage - and this is found in a large percentage of cases.

An interesting example of an unobvious effect of ESD occurred in Finland, where very cold winters produce very low humidity and particularly severe electrostatic problems. A customer complained that the AD549 low bias current BIFET op-amp had poor long-term reliability and that its noise performance deteriorated over a few years of use.

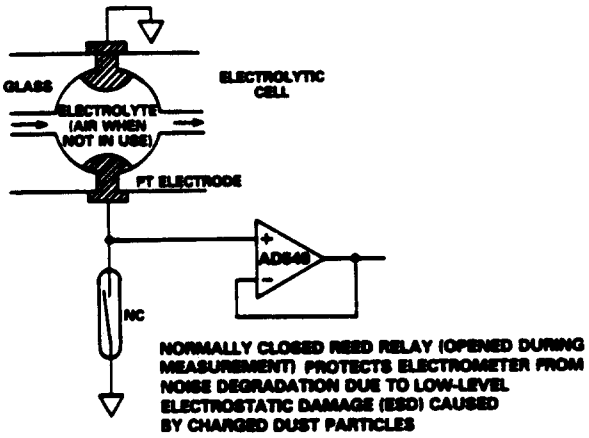


Figure 11.12

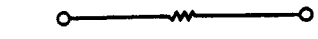
The amplifier was being used as a unity gain buffer with an electrochemical cell and the non-inverting input was connected to a platinum electrode and to nothing else. In use this electrode was immersed in electrolyte but after use it was washed (automatically) in deionized water and air dried. It was then left unconnected until the machine was next used.

Although there was no possibility of the electrode being touched at this time (it was in the very center of the machine) it could encounter random particles of electrostatically charged dust - and the pulse currents as these dust particles discharged were sufficient to cause gradual deterioration of the noise figure. As soon as arrangements were made to ground the electrode when it was not in use (with an NC reed relay for minimum leakage) the problem disappeared.

Parasitic effects in resistors

When we model a circuit, either informally or with a program such as SPICE, we generally assume that a resistor is a simple resistance. In fact any resistor is a much more complex device containing, at the very least, an inductance, a noise source, a capacitor and two thermocouples.

THE EQUIVALENT CIRCUIT OF A RESISTOR IS NOT



BUT

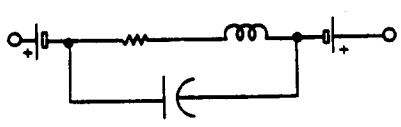


Figure 11.13

Inductive resistors

All resistors have some inductance (as we shall see, a straight piece of wire has some inductance) but wirewound resistors actually consist of a coil of wire, which must inevitably be inductive. Even if the coil is "non-inductive" and consists of N clockwise turns and N anticlockwise turns there will still be some mismatch and residual inductance. Residual inductance values of up to 20 μH can be expected in "non-inductive" wirewound resistors with values below 10 k ohms, although above 10 k ohms the reactance of such a resistor is more likely to be a capacitance of around 5 pF.

Some film resistors are also inductive, consisting of a spiral of resistive material on a cylindrical ceramic body. Again values of a few μH are typical. High frequency circuits must not use inductive resistors since their impedance is not equal to their resistance and, indeed, varies with frequency. Even low frequency circuitry, where the inductance of the resistors would not seem to be a problem, may suffer from instability arising from unforeseen HF effects of resistor inductance (the transistors used in low frequency op-amps frequently have Ft of up to 1 GHz).

Thermo-electric effects

Wirewound resistors have another problem. The junction of the resistance wire and the lead forms a thermocouple which has a thermoelectric EMF of 42 μV/°C for the standard "Alloy 180"/Nichrome junction of an ordinary wirewound resistor. If a resistor is chosen with the [more expensive] copper/nichrome junction the value is 2.5 μV/°C. ("Alloy 180" is the standard component lead alloy of 77% copper and 23% nickel.)

Such thermocouple effects are unimportant at AC or where a resistor is at a uniform temperature but if the dissipation in a resistor, or its location with respect to heat sources, can cause one of its ends to be warmer than the other then there will be a net thermoelectric EMF which will introduce a dc error into the circuit. With a normal wirewound resistor a temperature differential of only 4°C will introduce a dc error of 168 μV - which is greater than 1 LSB in a 10 V/16-bit system.

The problem may be minimized by mounting wirewound resistors to ensure that temperature differentials are minimized. This may be done by ensuring that both leads are of equal length to equalize thermal conduction through them, by making any airflow (whether forced or natural convection) nor-

MINIMIZING THERMOCOUPLE EFFECTS IN WIREWOUND RESISTORS

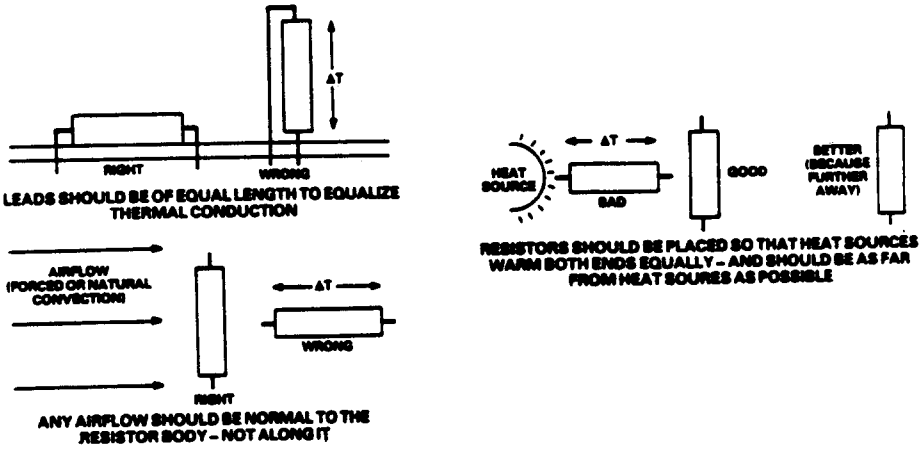


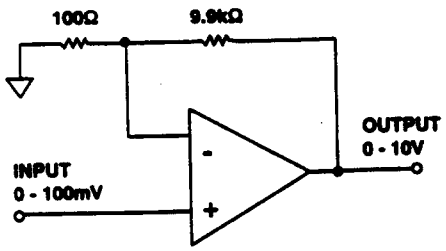
Figure 11.14

mal to the resistor body, and by taking care that both ends of the resistor are the same distance from any heat source on the PCB. Notwithstanding these precautions it is wiser to use resistors with copper, rather than "Alloy 180" leads, and to site them as far as possible from any heat source.

Stability & Matching

Thermal effects other than thermocouple effects will also affect the accuracy of circuits using resistors. Resistors are never completely stable with temperature and if either the temperature coefficients, or the actual temperatures of two resistors in a precision circuit are mismatched then the performance of the circuit will suffer. Temperature mismatch of two identical resistors in similar environments may arise from differences in self-heating or other causes.[3]

GAIN OF 100 STAGE



- Resistor mismatch due to mismatch of temperature coefficients, mismatch of temperature (possibly due to self-heating), or both, can cause gain errors.
- Ideally, all resistors whose matching can affect accuracy should be fabricated on a single substrate.

Figure 11.15

Typical temperature coefficients of discrete resistors are apt to be around 100 ppm/°C or more. The best way to minimize the effects of resistor temperature coefficients and to eliminate the effects of different resistor temperatures is to ensure that all resistors whose resistor matching affects the accuracy of a system are built on a single substrate. This substrate may be the glass or ceramic substrate of a thin film resistor network.

A better alternative, when possible, is to use an integrated circuit having laser trimmed thin film resistors on the silicon substrate of the IC. The temperature coefficient of such resistors can be well below 20 ppm/°C, and the differential temperature coefficient between two resistors on the same substrate is of the order of 0.5 ppm/°C or less.

Voltage Variation of Resistance

It is not possible to fabricate very high resistances on thin film or IC substrates, and high value discrete resistors are considerably less stable than lower value ones. It is inadvisable, therefore, to rely on the stability of high value resistors for the performance of a system. Some types of high value resistor have another imperfection: they have a slightly non-linear voltage/current curve and do not obey Ohm's Law accurately.

HIGH VALUE RESISTORS

- Likely to be Less Stable

and

- Non-Linear With Voltage

Figure 11.16

A final "imperfection" of resistors is an inconvenience but cannot properly be regarded as an imperfection as it is a fundamental property of all resistors: thermal or Johnson noise.

RESISTOR JOHNSON NOISE

- **All Resistors Have Noise: $V_N = \sqrt{4kTBR}$**
  - **T is Absolute Temperature**
  - **B is Bandwidth in Hertz**
  - **R is the Resistance in Ohms**
  - **k is Boltzmann's Constant (1.38E-23 J/K)**
- **It is possible to reduce the noise of a resistor by reducing T, B, or R but it is *NOT* possible to reduce k because Boltzmann is dead.**

Figure 11.17

At any temperature above absolute zero all resistors have noise due to thermal motion of their structure. This noise, which is described by

$$V_n = \sqrt{4kTBR}$$

(Where k is Boltzmann's constant: 1.38E-23 J/°K)

Johnson noise is present in ALL resistors and can only be reduced by reducing R, the resistance itself, B, the bandwidth of interest, or T, the temperature. Since the function involves a square root, the noise improvement for a drop in temperature from room temperature (298 °K) to liquid nitrogen (77 °K) is only of the order of 50%, so cooling a resistor, unless liquid helium is involved, is unlikely to be very profitable.

Johnson noise is purely an effect of resistance. The Johnson noise of complex impedances consists only of the Johnson noise of the resistive part of the impedance, so pure capacitance or inductance does not have Johnson noise, even though it has an impedance.

CAPACITANCE

STRAY CAPACITANCE

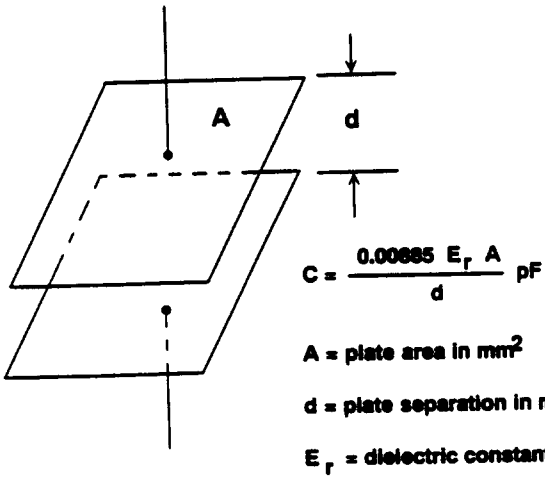
Where two conductors are not short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. There will therefore be a large number of capacitors associated with any circuit, which may or may not be considered in models of the circuit. Where high frequency performance matters (and even DC and VLF circuits may use devices with high Ft and therefore be vulnerable to HF instability) it is very important to consider the effects of stray capacity.

Any basic textbook will provide formulas for the capacitance of parallel wires, concentric spheres and cylinders, and many other configurations.[4] The only example we need consider in this seminar is the parallel plate capacitor, which is formed by conductors on opposite sides of a PCB.

Neglecting edge effects, the capacitance of two parallel plates of area A mm² and separation d mm in a medium of dielectric constant E_r relative to air is

$$0.00885\ E_r\ A/d\ \text{pF}.$$

CAPACITANCE



$$C = \frac{0.00885\ E_r\ A}{d}\ \text{pF}$$

- **A = plate area in mm²**
- **d = plate separation in mm**
- **E_r = dielectric constant relative to air**

- **Commonest type of PCB uses 1.5mm glass-fiber epoxy material with $E_r = 4.7$**
- **Capacity of PC track over ground plane is roughly 2.8pF/cm²**

Figure 11.18

From this formula we can calculate that for general purpose PCB material ($E_r = 4.7$, d = 1.5 mm) the capacitance between conductors on opposite sides of the board is just under 3pF/cm². In general such capacitance will be parasitic, and circuits must be de-

signed so that it does not affect their performance, but it is possible to use PCB capacitance in place of small discrete capacitors. However the dielectric properties of common PCB materials (teflon is an expensive exception) cause such capacitors to have a rather high temperature coefficient and to have poor Q at high frequencies, which makes them unsuitable for many applications.

Capacitive Noise & Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum is a dielectric). If there is a change of voltage on one there will be a movement of charge on the other. The basic model is shown in Figure 11.19.

CAPACITIVE COUPLING EQUIVALENT CIRCUIT

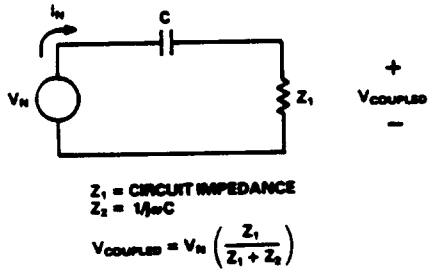


Figure 11.19

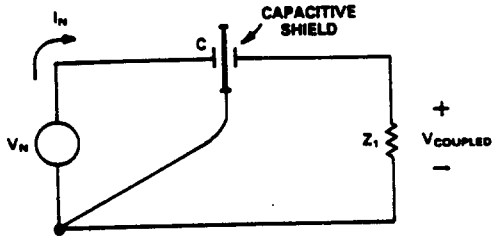
It is evident that the voltage coupled into Z1 may be reduced by reducing the signal voltage, Vn, the frequency involved, the capacitance, or Z1, but frequently none of these can be changed. The best solution is to insert a grounded conductor (known as a Faraday shield) between the noise source and the circuit which it affects.

The Faraday shield is easily implemented and almost invariably successful. For this reason capacitively coupled noise is rarely an intractable problem. However, to be effective the shield must completely block the electric field between the noise source and the shielded circuit and must be connected so that the noise current returns to its source without flowing in any part of the circuit where it might introduce conducted noise. A conductor intended as a Faraday shield must never be left unconnected as this almost always increases capacity and exacerbates the problem.

An example of this problem is seen in sidebrazed ceramic IC packages. These DIP packages have a small square conducting

CAPACITIVE SHIELDING

CAPACITIVE SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD



EQUIVALENT CIRCUIT ILLUSTRATES HOW A CAPACITIVE SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH Z_1

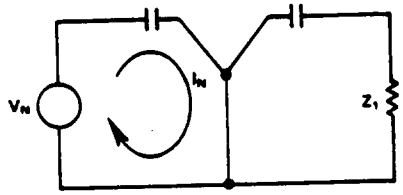
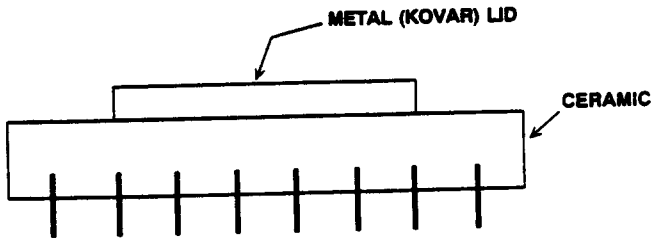


Figure 11.20

kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package or it may be left unconnected. Most logic circuits have a ground pin at one of the package corners and therefore the lid is grounded. Many analog circuits do not have a ground pin at a package corner and the lid is left floating - such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package where the chip is completely unshielded.

CAPACITIVE EFFECTS DUE TO METAL LIDS



- SIDEBRAZE CERAMIC D.I.L. PACKAGES SOMETIMES HAVE ISOLATED METAL LIDS
- THESE ARE VULNERABLE TO CAPACITIVE INTERFERENCE AND SHOULD BE GROUNDED (IF POSSIBLE)

Figure 11.21

Whatever the environmental noise level, it is good practice for the user to ground the lid of any sidebrazed ceramic IC where the lid is not grounded by the manufacturer - this can be done with a wire soldered to the lid (this will not damage the device as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable a grounded phosphor-bronze clip may be used to make the ground connection, or conductive paint from the lid to the ground pin. Never attempt to ground such a lid without verifying that it is, in fact, unconnected, as occasionally device types will be found with the lid connected to a power supply rather than to ground!

One case where a Faraday shield is impracticable is between the bondwires of an integrated circuit chip. This has important consequences.

STRAY CAPACITY BETWEEN CHIP BONDWIRES

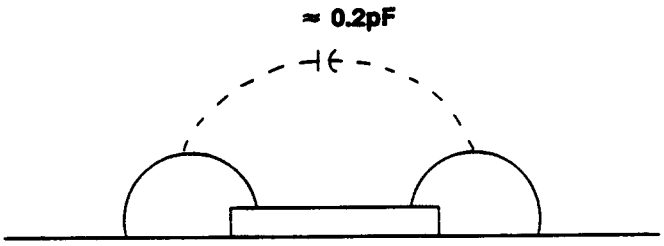


Figure 11.22

The stray capacitance between two chip bondwires and their associated leadframes is of the order of 0.2 pF. (Note this is "of the order" NOT "of the close order" - observed values generally lie between 0.05 and 0.6 pF.) If we have a high resolution converter (ADC or DAC) which is connected to a high speed data bus then each line of the data bus, which will be carrying noise with 2-5 V/ns dV/dT, is connected to the converter analog port via this stray capacitance. Whenever the bus is active intolerable amounts of noise will be capacitively coupled to the analog port and will seriously degrade the performance of which the converter is capable.

WITH A HIGH PERFORMANCE CONVERTER ON A HIGH SPEED DATA BUS, IT IS NOT POSSIBLE TO SHIELD THE ANALOG PORT FROM THE DIGITAL NOISE

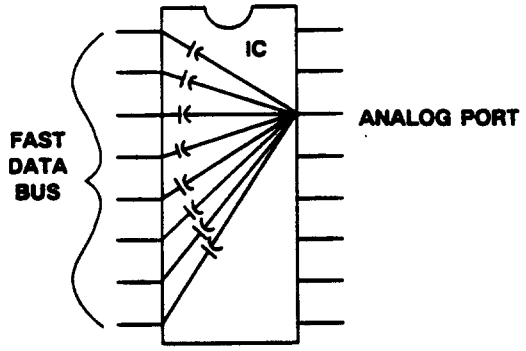
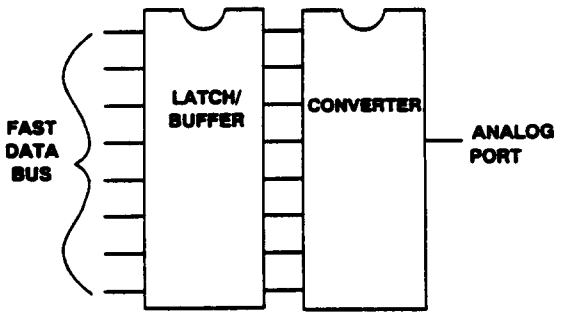


Figure 11.23

Present technology offers no cure for this problem, which also limits the performance possible from broadband monolithic mixed signal ICs having analog and digital circuitry on a single chip. However, it may be avoided quite simply by not connecting the databus directly to the converter but by using a latched buffer as an interface. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power and complicates design - but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile in individual cases.

BUFFER LATCH USED AS FARADAY SHIELD



- A BUFFER/LATCH CAN ACT AS A FARADAY SHIELD BETWEEN A FAST DATA BUS AND A HIGH PERFORMANCE CONVERTER
- IT ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY AND IMPROVED PERFORMANCE

Figure 11.24

EQUIVALENT CIRCUITS OF A REAL CAPACITOR

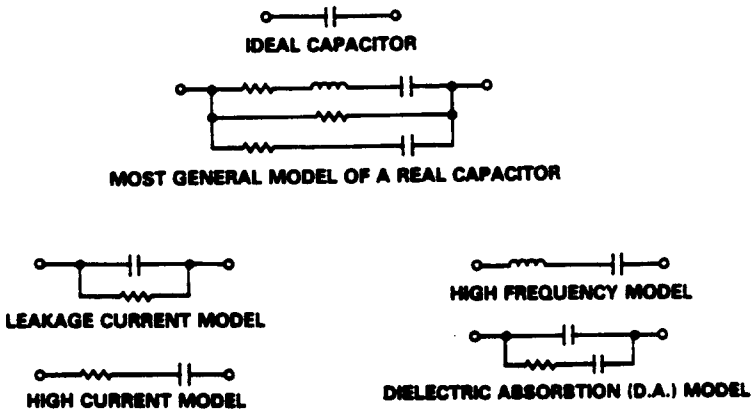


Figure 11.25

PARASITIC EFFECTS IN CAPACITORS

Just as we are too willing to assume that a resistor is a perfect resistor, so do we underestimate the parasitic components associated with a capacitor. Fig 25 shows the ideal, the general model of a real capacitor, and the simplified models which are adequate for the analysis of non-ideal behavior in most applications.

Capacitors are used for coupling (passing AC signals while blocking DC), for decoupling (removing AC superimposed on DC in both power and signal circuitry), for building filters or frequency-selective networks, and for storing charge in "sample and hold" circuits (also known as "track and hold" circuits or SHAs, SAHs or THAs).

CAPACITOR LEAKAGE

In coupling and SHA applications the leakage of the capacitor can be important. Electrolytic capacitors, where the dielectric is formed by an electrochemical reaction, have relatively high leakage currents of microamperes or even more and so are not used in applications where leakage matters. The leakage of electrolytic capacitors is greater during the first few minutes of operation after a period of storage (the leakage current while the capacitor is in use keeps the dielectric in good condition and it may deteriorate slightly in storage) - this feature can be important in equipment which must perform correctly after a long quiescent period.

The leakage of tantalum electrolytic capacitors is lower than that of aluminium ones and so in applications where capacitances of tens of microfarads or more (which can be easily achieved only with electrolytic capacitors) are required tantalum ones are used, despite their extra cost, if particularly low values of leakage current are necessary. At room temperature the leakage of aluminium electrolytic capacitors is of the order of 20 nA/μF and that of tantalum ones is 5 nA/μF.

Another feature of electrolytic capacitors, both aluminium and tantalum, is that most of them are polarized and require a DC bias for correct operation - a reverse bias may do damage and will certainly increase leakage (unpolarized electrolytic capacitors, which may be biased in either direction, do exist but they are uncommon, and considerably larger than the polarized variety).

Most other types of capacitor have leakage resistances in excess of hundreds of gigohms so that for most applications their leakage currents can be disregarded.

SERIES/LOSS RESISTANCE

The series resistance of capacitors causes them to dissipate power when high AC currents are flowing in them. This can have serious consequences at RF and in supply decoupling capacitors carrying high ripple currents but is unlikely to have much effect in precision analog circuitry. The series inductance, however, can have very inconvenient consequences.

INDUCTANCE OF CAPACITORS

The transistors used in precision analog circuits have transition frequencies (Ft) of hundreds of MHz or even several GHz, even though the precision circuitry itself may be operating at DC or low frequencies. This makes it essential that the power supply terminals of such circuits should be decoupled properly at high frequency.

A common structure for capacitors is two sheets of metal foil separated by sheets of plastic or paper dielectric and formed into a

HIGH FREQUENCY DECOUPLING (REQUIRED EVEN BY LF ANALOG CIRCUITS)

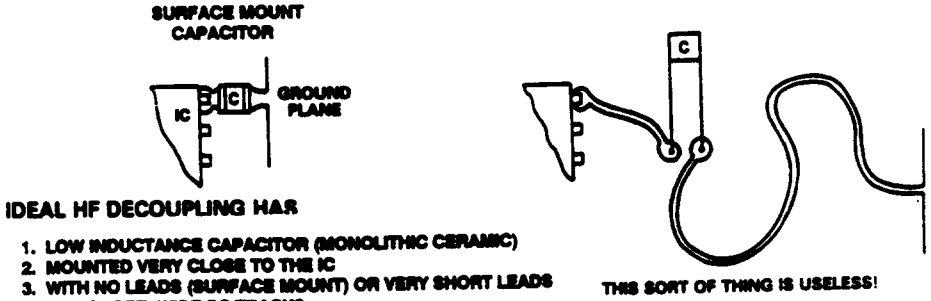


Figure 11.26

roll. Such a structure has considerable self inductance and behaves as an inductance rather than a capacitor at frequencies of more than a few MHz. It is therefore inadvisable to use electrolytic , paper or plastic film capacitors for decoupling at high frequencies.

Monolithic ceramic capacitors have very low series inductance (they are formed of a multilayer sandwich of metal films and ceramic dielectric and all the films are joined to a bus-bar rather than being connected in series). They are therefore ideal for high frequency decoupling. However, monolithic ceramic capacitors can be microphonic, and some types may be self-resonant with comparatively high Q. Disc ceramic capacitors, on the other hand, are sometime quite inductive, although less expensive.

The best way of ensuring that an analog circuit is adequately decoupled at both high and low frequencies is to use a tantalum bead capacitor in parallel with a monolithic ceramic one. The combination will have high capacitance but will remain capacitive at VHF frequencies. It is generally unnecessary to have a tantalum capacitor on each individual IC, if there is less than 10 cm of reasonably wide PC track between each IC and the tantalum capacitor it is possible to share one tantalum capacitor among several ICs.

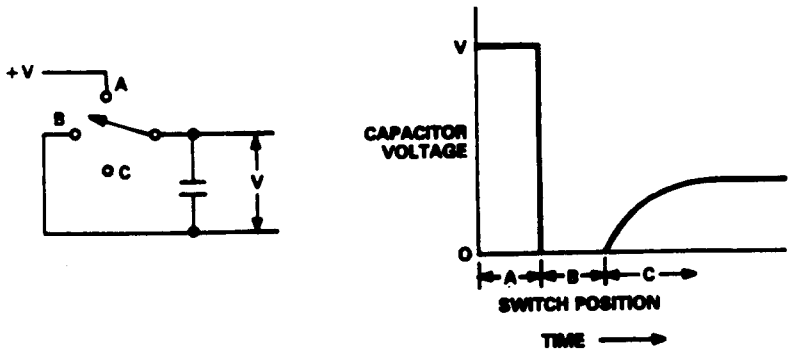
There is little point in taking great care in the choice of a non-inductive capacitor if it is then unsuitably mounted. Short lengths of wire have appreciable inductance so HF decoupling capacitors must be mounted as close as possible to the points that they are decoupling with short, wide PC tracks. Ideally HF decoupling capacitors should be surface-mount parts to eliminate lead inductance, but wire-ended capacitors are permissible provided the device leads are no longer than 1.5 mm. It is also important to understand where HF decoupling currents should flow and why HF decoupling is more important at some points than at others - the subject is covered at some length in an Analog Devices Application Note.[5]

HF instability in analog circuits is more common than is realized. Oscillation at hundreds of MHz will cause serious malfunction of precision circuitry but may not affect an oscilloscope (indeed the presence of an oscilloscope probe may damp the oscillation, so that the circuit works only when an oscilloscope is attached to it - this is an important diagnostic clue). It is quite good practice to use a broadband spectrum analyzer (say 1-1500 MHz) and a low capacity FET probe to check for parasitic oscillation any analog circuit which is malfunctioning for no obvious reason. This test will also show if the malfunction is due to the presence of a strong RF field from an external source.

Dielectric Absorption

Monolithic ceramic capacitors are excellent for HF decoupling but they have considerable dielectric absorption, which makes them unsuitable for use as the hold capacitor of an SHA. Dielectric absorption causes a capacitor which is quickly discharged and then open-circuited to recover some of its charge. Since the amount of charge recovered is a function of its previous charge this is, in effect, a charge memory and will cause errors in any SHA where dielectric absorption is present in the hold capacitor.

CAPACITORS HAVING SIGNIFICANT D.A. ARE USELESS FOR SAMPLE AND HOLD APPLICATIONS



DIELECTRIC ABSORBTION CAUSES A BRIEFLY DISCHARGED CAPACITOR TO RECOVER A PERCENTAGE OF ITS PREVIOUS CHARGE ON BEING OPEN CIRCUITED.

Figure 11.27

Capacitors for this application should therefore be selected to have minimal dielectric absorption. The best strategy is to use a SHA which is supplied with an internal capacitor or where the SHA manufacturer supplies the capacitor with the SHA. If this is not possible (sometimes one may require a longer hold time - and hence extra capacity) a capacitor should be chosen which has its low dielectric absorption (DA) specified on its data sheet.

Such capacitors are normally plastic dielectric types (polystyrene, polypropylene or teflon) but it is not safe to use just any plastic dielectric capacitor with a SHA as special processing and testing is necessary to ensure that it has low DA. For use with a SHA a capacitor should be chosen which is specified for low DA applications.

INDUCTANCE

STRAY INDUCTANCE

All conductors are inductive and at high frequencies the inductance of even quite short pieces of wire may be important. The inductance of a straight wire of length L mm and circular cross-section with radius R mm in free space is

$$0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H.$$

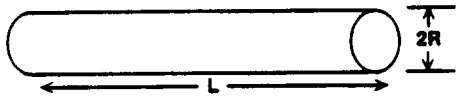
The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is

$$0.0002L\left[\ln\left(\frac{2 \cdot L}{W + H}\right) + 0.2235\left(\frac{W + H}{L}\right) + 0.5\right]\mu H.$$

In real systems these formulas both turn out to be approximate but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5 mm o.d. wire has an inductance of 7.26 nH and 1 cm of 0.25 mm PC track has an inductance of 9.59 nH - these figures are reasonably close to measured results.

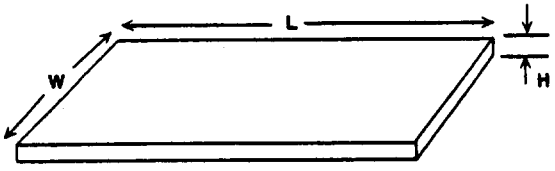
At 10 MHz an inductance of 7.26 nH has an impedance of 0.46 ohm and so can give rise to 1% error in a 50 ohm system.

INDUCTANCE



WIRE INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH (2R = 0.5mm, L = 1cm)



STRIP INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu H$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH (H = 0.038mm, W = 0.25mm, L = 1cm)

Figure 11.28

NONIDEAL AND IMPROVED SIGNAL ROUTING

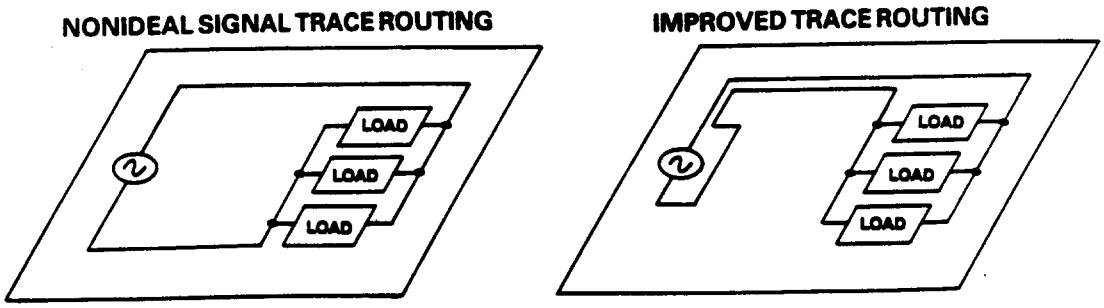


Figure 11.29

MUTUAL INDUCTANCE

Another consideration regarding inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in closed paths - there is always an outward and return path. The whole path forms a single-turn inductor. If the area enclosed by the turn is large the inductance, and hence the AC impedance, will also be large, whereas if the outward and return paths are close together the inductance will be much smaller. The principle is illustrated in Fig 11.29.

The nonideal routing in Figure 11.29 has another drawback - the large area enclosed by the conductor produces extensive external magnetic fields, which may interact with other circuits and cause unwanted coupling. Similarly the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop. The basic principle is illustrated in Figure 11.30 and is a common mechanism for the transfer of unwanted signals (noise) between circuits.

BASIC PRINCIPLES OF INDUCTIVE COUPLING

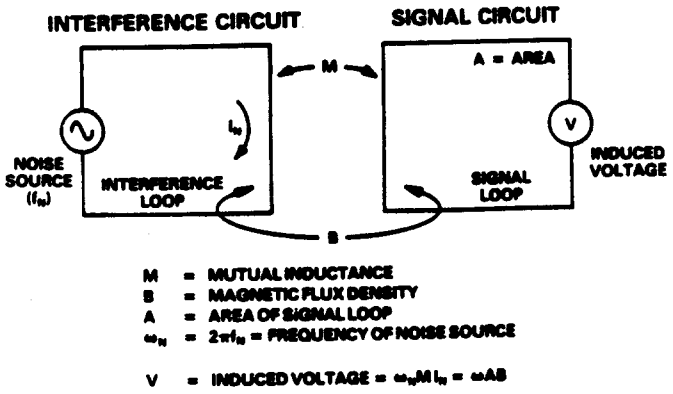


Figure 11.30

As with most other sources of noise, as soon as we define the principle at work we can see ways of reducing the effect. In this case reducing any or all of the terms in the equations in Figure 11.30 will reduce the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on both sides and, possibly, increasing the distance between them.

PROPER SIGNAL ROUTING REDUCES MUTUAL INDUCTANCE

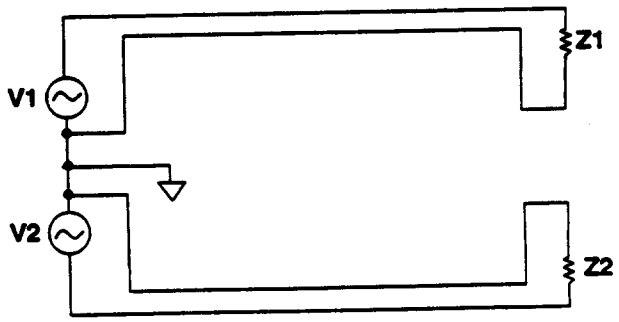


Figure 11.31

Mutual inductance is a common problem in ribbon cables, especially when a single return is common to several signal circuits. Separate signal and return lines for each signal circuit reduces the problem, and using a cable with twisted pairs for each signal circuit is even better (but more expensive and often unnecessary).

MUTUAL INDUCTANCE AND SIGNAL COUPLING IN RIBBON CABLE

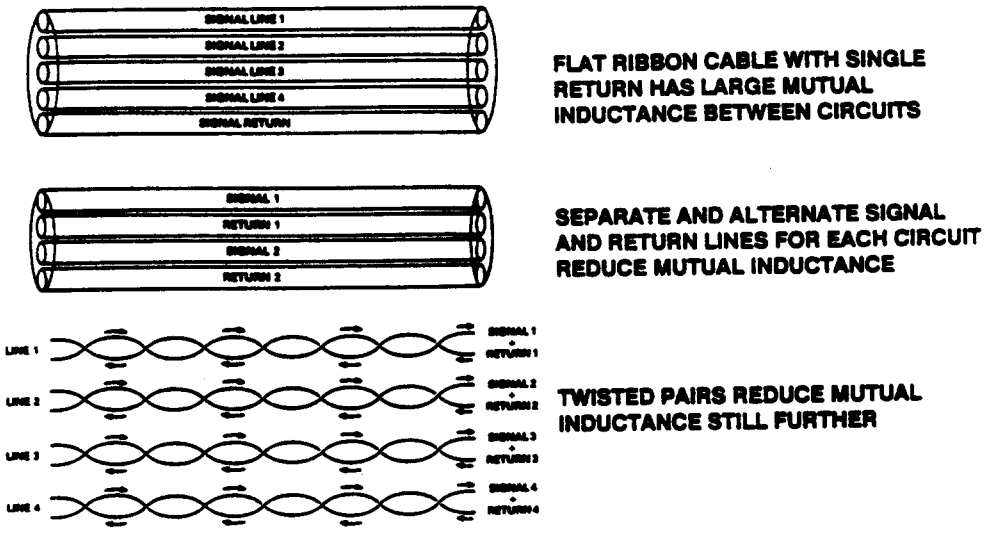
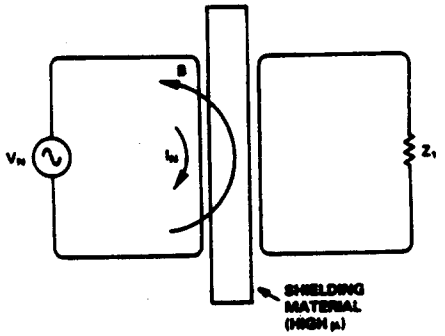


Figure 11.32

Shielding magnetic fields to reduce mutual inductance is sometimes possible but is by no means as easy as shielding electric fields with a Faraday shield. HF magnetic fields are blocked by conductive material, while LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

MAGNETIC SHIELDING



- Magnetic shielding is not as easily accomplished as electrostatic shielding, but may be done at HF with a simple conducting screen, and at LF and DC with a screen of high permeability material such as Mu-metal.

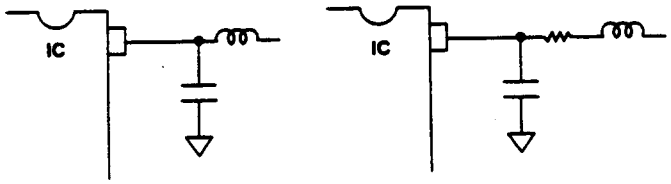
Figure 11.33

RINGING

An inductor in series or parallel with a capacitor forms a resonant, or "tuned", circuit, whose key feature is that it shows marked change in impedance over a small range of frequency (how sharp the effect is depends on the Q of the tuned circuit). The effect is widely used to define the frequency response of narrow-band circuitry but can also be a source of problems.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit then that tuned circuit may be excited by signals in the circuit and ring at its resonant frequency. A common example is shown in Figure 11.34 where the resonant circuit formed by an inductive power line and its decoupling capacitor may be excited by pulse currents drawn by the IC.

RESONANT CIRCUITS FORMED BY DECOUPLED POWER LINES



EQUIVALENT CIRCUIT OF DECOUPLED POWER LINE - RESONANT AT

$$f = \frac{1}{2\pi\sqrt{LC}}$$

SMALL SERIES RESISTANCE CLOSE TO THE IC REDUCES THE Q

Figure 11.34

The effect may be minimized by lowering the Q of the inductance, which is most easily done by inserting a small resistance in the power line, close to the IC.

Parasitic effects in inductors

Although inductance is one of the fundamental properties of an electronic circuit, inductors are less common as precision components than resistors and capacitors. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of μH, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are relatively rarely used in precision analog circuitry, except in tuned circuits for high frequency narrow band applications.

Of course they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant. The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core its inductance will be essentially unaffected by the current it is carrying, but if it is wound on a core of a magnetic material (magnetic alloy or ferrite) its inductance will be non-linear since at high currents the core will start to saturate.

SATURATION

- **Inductors with solid cores (magnetic alloy or ferrite)**
  will behave non-linearly
  if required to carry too much current.
- **This is unlikely to be a direct problem in precision circuitry but may affect power supply noise performance and thus affect precision circuitry indirectly.**

Figure 11.35

Such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits. Since all inductors will have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet) and should only be used as precision inductors at frequencies well below this.

STRAY CAPACITANCE MAKES ALL INDUCTORS INTO TUNED CIRCUITS

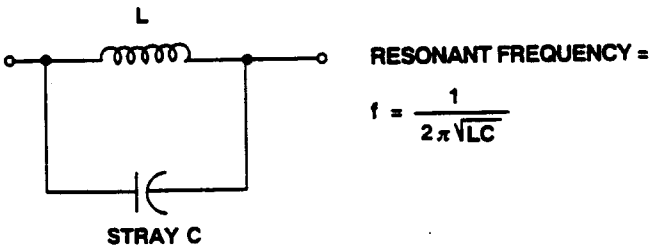


Figure 11.36

Q or "Quality Factor"

The other parasitic characteristic of inductors is their Q (or "Quality Factor"), which is the ratio of their reactive impedance to their resistance.

$$Q = 2\pi f L / R$$

It is rarely possible to calculate the Q of an inductor from its DC resistance since skin effect (and core losses if the inductor has a magnetic core) ensure that the Q of an inductor at high frequencies is always lower than that predicted from DC values.

Q is also a characteristic of tuned circuits (and of capacitors - but capacitors generally have sufficiently high values of Q that it may be disregarded for most practical purposes). The Q of a tuned circuit, which is generally very similar to the Q of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance.

Q or "QUALITY FACTOR"

- **The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.**
  $Q = 2\pi fL/R$
- **The resistance is the HF and *NOT* the DC Value.**
- **The 3dB bandwidth of a single tuned circuit is Fc/Q where Fc is the center frequency.**

Figure 11.37

LC tuned circuits rarely have Q of much more than 100 (3 dB bandwidth of 1%) but ceramic resonators may have Q of thousands and quartz crystals have Q of tens of thousands.

SIGNAL RETURN CURRENTS

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit.[6]

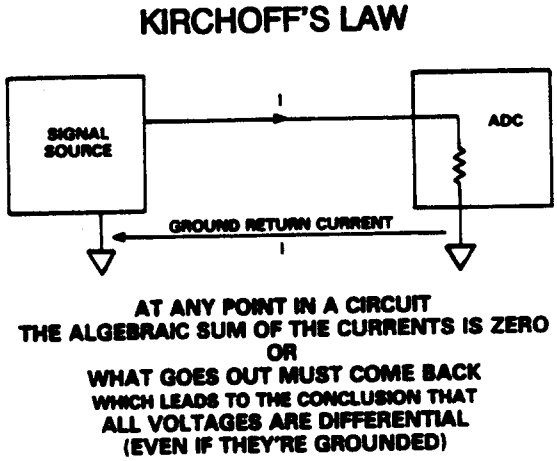


Figure 11.38

Most people consider the return current when considering a fully differential circuit, but when considering the more usual circuit where a signal is referred to "ground" it is common to assume that all the points on the circuit diagram where the ground symbol is to be found are at the same potential. This is unwise.

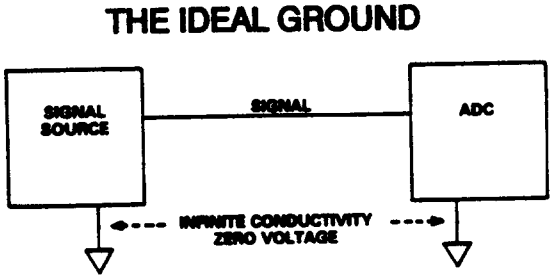


Figure 11.39

GROUND NOISE & GROUND LOOPS

A more realistic model of ground is shown in Figure 11.40. Not only does the return current flow in the complex impedance which exists between the two "ground" points shown in Figure 11.39, giving rise to a voltage drop in the total signal path, but external currents may also flow in the same path, generating uncorrelated noise voltages which are seen by the ADC.

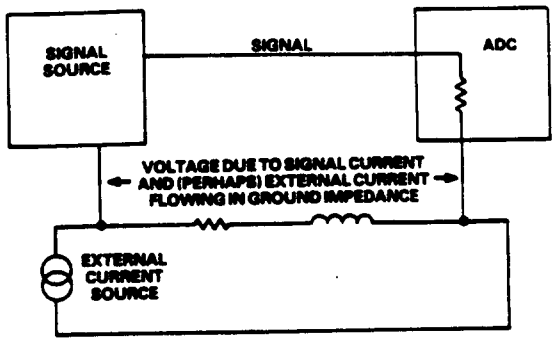


Figure 11.40

It is evident, of course, that other currents can only flow in the ground impedance if there is a current path for them. Figure 11.40 shows such a path at "ground" potential, which is the notorious "Ground Loop", but equally severe problems could be caused by a circuit sharing an unlooped ground return with the signal source but drawing a large and varying current from its supply and ground return.

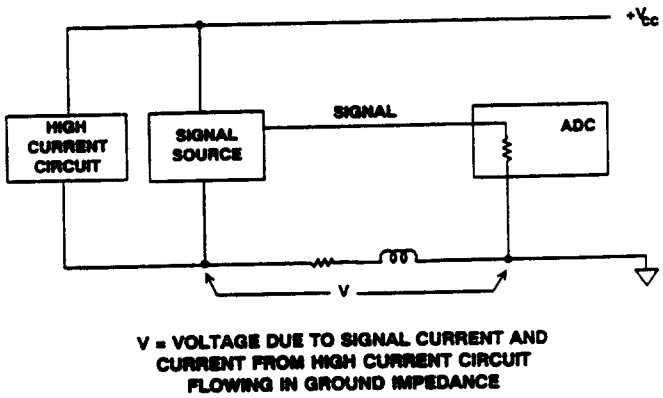
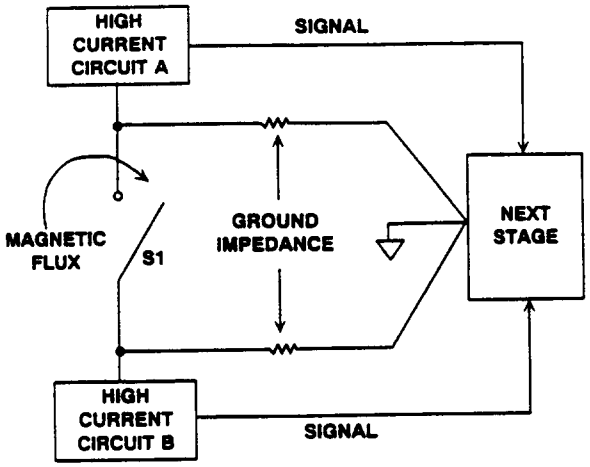


Figure 11.41

It is evident from Figure 42 that if a ground network contains loops there is a greater danger of it being vulnerable to EMFs induced by external magnetic fields, and of ground current "escaping" from high current areas to cause noise in sensitive regions. For these reasons ground loops are best avoided.

However, there are situations where looped grounds are unlikely to cause unacceptable noise and the configuration may actually offer benefits in the form of safety or reduced impedance. In such circumstances the optimum ground arrangement may

GROUND LOOP



CLOSING S1 FORMS A GROUND LOOP.

NOISE MAY COME FROM:

- MAGNETIC FLUX CUTTING THE GROUND LOOP
- A'S GROUND CURRENT FLOWING IN B'S GROUND IMPEDANCE
- B'S GROUND CURRENT FLOWING IN A'S IMPEDANCE

Figure 11.42

contain loops. Sensible engineers should not allow the almost superstitious dread inspired by the term "ground loop" to prevent the adoption of such designs, if careful analysis and experiment has shown that they actually are optimum.

There are a number of possible ways of attacking the problem of ground noise, apart from the (presently) impracticable one of using superconducting grounds. It is rare for a single method to be used to the exclusion of all others, and systems generally contain a mixture of approaches. For the purposes of description, however, it is better to describe each approach separately.

Star (Mecca) Grounds

The "star" or "Mecca" ground philosophy builds on the theory that there is a single point in a circuit to which all voltages are referred. This is known as the "star" or "Mecca" point.

STAR (MECCA) GROUNDS

If all signal voltages in a system are measured with respect to a single point, that point is said to be the *star* ground of the system.

Figure 11.43

This philosophy is reasonable but frequently encounters practical difficulties. For example if we design a system with a star ground, drawing all the signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we frequently find, when the power supplies are added to the circuit diagram, that the power supplies either add unwanted ground paths or that supply currents, flowing in existing ground paths, are sufficiently large, or noisy, or both, as to corrupt the signal transmission. This problem may often be avoided by having separate power supplies for different parts of the circuit - separate analog and digital supplies, and separate analog and digital grounds joined at the star point, are common in mixed signal applications.

Separate Analog and Digital Grounds

Digital circuitry is noisy. Saturating logic draws large fast current spikes from its supply during switching and, having noise immunity of hundreds of millivolts or more, has little need of high levels of supply decoupling.

Analog circuitry, on the other hand, is very vulnerable to noise in supplies or grounds. It is therefore sensible to separate analog and digital circuitry to prevent digital noise from corrupting analog performance. Such separation will involve separation of both grounds and power supplies, which may be inconvenient in a mixed signal system. Nevertheless, if a system is to give the full performance of which it is capable it is often essential to have separate analog and digital grounds and power supplies. The fact that some analog circuitry will operate from a single +5 V supply does NOT mean that it may safely be operated from the same noisy +5 V supply as the microprocessor and dynamic RAM, the electric fan, and the solenoid jackhammer!

SUPPLY & GROUND NOISE

- Digital circuitry is noisy
- Analog circuitry is quiet
- Circuit noise from digital circuitry carried by power and ground leads can corrupt precision analog circuitry
- It is advisable to separate the power and ground of the digital and analog parts of a system
- Analog and digital grounds must be joined at ONE point

Figure 11.44

However, analog and digital ground in a system must be joined at some point to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system - it is often convenient to make the connection at the power supplies.

Many ADCs and DACs have separate "analog ground" and "digital ground" pins, and users are advised, on the data sheets, to connect these pins together at the device package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

ANALOG GROUND & DIGITAL GROUND

- Monolithic & hybrid ADCs frequently have separate AGnd & DGnd pins which must be joined together at the device.
- This is not done from a desire to be difficult, but because the voltage drop in the bondwires is too large to allow the connection to be made internally.
- The best solution to the grounding problem arising from this requirement is to connect both pins to system "analog ground".
- It is likely that neither the digital noise so introduced in the system AGnd, nor the loss of digital noise immunity, will seriously affect the system performance.

Figure 11.45

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the parts of the converter to which the pins are connected, and not to the system grounds to which they must go.

In general these two pins should be joined together and to the analog ground of the system. It is not possible to join the two pins within the IC package because the analog part of the converter cannot tolerate the voltage resulting from the digital current flowing in the bond wire to the chip.

If these pins are connected in this way the digital noise immunity of the converter is diminished by the amount of common- mode noise between the digital and analog system grounds. Since digital noise immunity is of the order of hundreds or thousands of millivolts this is unlikely to be important.

ANALOG GROUND (AGND) AND DIGITAL GROUND (DGND) OF ADCs/DACs SHOULD BE RETURNED TO SYSTEM ANALOG GROUND

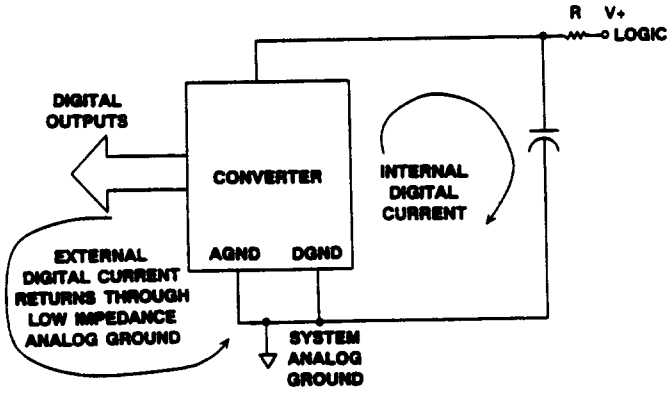


Figure 11.46

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be quite small, and can be minimized by ensuring that the converter outputs do not drive large fanouts. If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a 0.1µF capacitor sited as close to the converter as possible all the internal digital currents of the converter will return to ground through the capacitor and will not appear in the external ground circuit. If the analog ground impedance is as low as it should be for adequate analog performance the additional noise due to the external digital ground current should rarely present a problem.

GROUND PLANES

Related to the star ground system is the use of a ground plane. One side of a double-sided PCB, or one layer of a multi-layer one, is made of continuous metal, which is used as ground. The theory behind this is that the large amount of metal will have low resistance and as low inductance as is possible.

GROUND PLANES

- One entire side or layer of a PCB is continuous grounded conductor.
- This gives minimum ground resistance and inductance but is not always sufficient to solve all grounding problems.
- Breaks in ground planes can improve or degrade circuit performance - there is no general rule.
- Twenty years ago ground planes were difficult to fabricate. Today they are not.
- If your PCB facility objects to fabricating ground planes - GET A NEW PCB FACILITY!

Figure 11.47

It is sometimes argued that ground planes should not be used because they are liable to introduce problems in manufacture and assembly. Such an argument may have had a limited validity twenty years ago when PCB adhesives were less well developed, wave-soldering less reliable, and solder resist techniques less well understood, but today it should not be tolerated.

Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance and in some circumstances they can be enough to prevent proper circuit function. Figure 11.48 shows such a problem - and a possible solution.

Consider a ground-plane PCB 100 mm wide with a ground connection at one end and a power amplifier at the other drawing 15A. If the ground plane is 0.038 mm thick and 15 A flows in it there will be a voltage drop of 68 μV/mm. This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. However, if we slit the ground plane so that high current does not flow in the region of the precision circuitry we can possibly solve the problem - even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

A SLIT IN A GROUND PLANE CAN RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

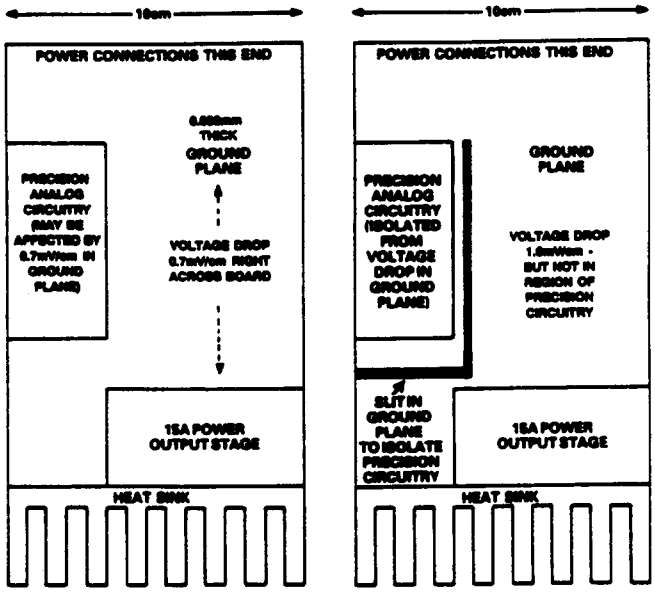


Figure 11.48

TRANSMISSION LINES

A break in a ground plane is not always a good thing. We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As we saw in Figure 11.7, when an HF signal flows in a PC track running over a ground plane the arrangement functions as a microstrip transmission line and the majority of the return current flows in the ground plane underneath the line.

The characteristic impedance of the line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. For most lower frequency applications the characteristic impedance will be unimportant, as the line will not be correctly terminated, but at UHF and higher

MICROSTRIP TRANSMISSION LINE

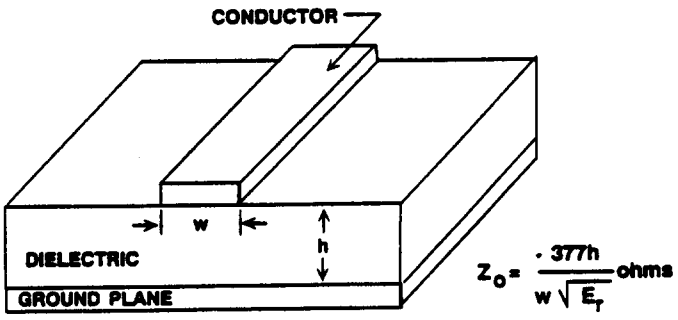


Figure 11.49

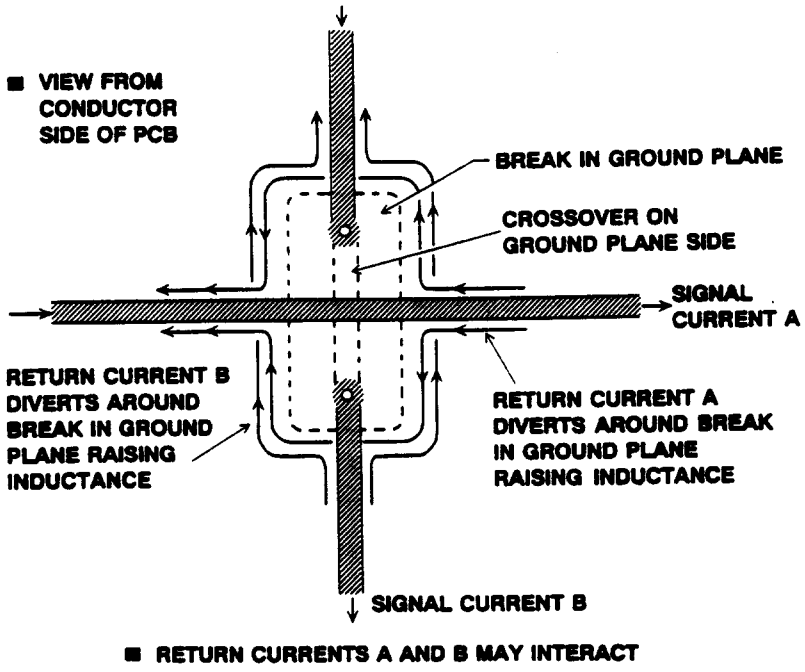


Figure 11.50

it is possible to use PCB tracks as microstrip transmission lines in properly terminated systems. If losses in such systems are to be minimized the PCB material must be chosen for low high frequency loss. This usually means the use of expensive teflon PCB material.

Where there is a break in the ground plane under a conductor the return current must flow around the break and both the inductance and the vulnerability of the circuit to external fields are increased.

Where such a break is made to allow a crossover of two perpendicular conductors it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than simple double-sided boards but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

Use of double-sided or multi-layer board with at least one continuous ground plane is undoubtedly one of the most successful approaches to the design of high performance mixed signal circuitry. Often the impedance of the ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system, but this does depend upon the resolution and bandwidth required and the amount of digital noise in the system.

System Grounds

In systems where there are several PCBs grounding may be more of a problem. At first sight it would appear that the problem is similar to that of a single PCB where particular subsystems must be positioned so that large ground currents do not flow where ground noise must be minimized - in a multi-card system the grounds of individual PCBs must be interconnected so that such harmful interactions are minimized.

There are three problems with this. First of all there is far less opportunity for rearranging the physical layout of a system consisting of a few cards connected to a common backplane. Secondly many multi-card systems are designed to be reconfigured in a "mix 'n' match" arrangement to allow large numbers of system options - it can be impossible to predict what systems are going to be required and to ensure that all of them are noise free. Finally, multicard systems are likely to have higher ground currents than occur on single, relatively simple, PCBs - but these currents must flow in the higher impedances which are associated with the intercard connectors even when multiple ground pins are used.

The basic principles still apply: ground impedance must be as low as possible, high level and low level signals must be separated so that they do not interfere with each other, and capacitance and mutual inductance coupling must be avoided. Nevertheless, it must be accepted that situations can arise where it is not possible to transfer a high speed, high accuracy signal from one PCB to another without unacceptable signal degradation.

MULTIPLE CARD SYSTEMS

- **Multiple card systems are likely to have higher ground currents and higher ground impedances than are found on a single PCB.**
- **It is therefore more difficult to transfer ground-referenced signals accurately between cards than across a PCB.**
- **In some cases it will be IMPOSSIBLE to transfer ground-referenced signals between PCBs without unacceptable loss of quality.**

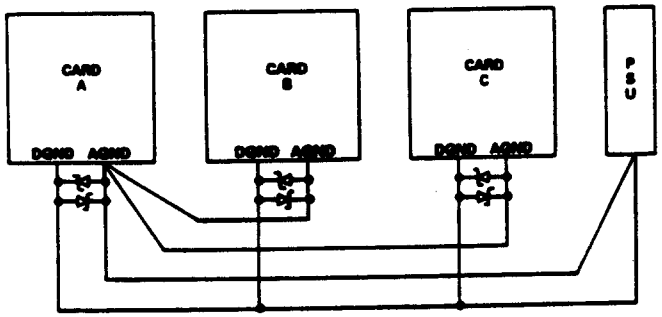
Figure 11.51

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane and have a ground plane (or even two - one analog, one digital) on that mother card. If the earlier advice about multiple ground pins has been observed this arrangement is capable of excellent performance. Where there are several card cages (racks for PCBs) the ground planes of the several mother boards must be tied together and, probably, to the metal chassis holding the card cages - the exact layout of the interconnections will depend on the overall system architecture.

If a mother board with a ground plane is not possible then the ground pins of the PCB sockets must be wired together, with due attention to probable current flows and common ground impedances, with heavy, multi-strand wire, having as low resistance as possible. In many cases the resulting ground screen will be tied to chassis ground at a number of points but it will sometimes be better to join them at a single star point.

It is not just the ground layout that is important in high performance mixed signal systems, the siting of different subsystems and the routing of signals is most important in determining overall system performance.

STAR ANALOG GROUND IN A MULTICARD SYSTEM



- Schottky diodes protect cards in the event of loss of analog ground
- This grounding system may be inadequate at high resolution or where large ground currents flow
- This MAY permit accurate intercard transmission of ground referenced signals

Figure 11.52

SIGNAL ROUTING

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- **Physically Separate Analog and Digital Signals**
- **Avoid Crossovers Between Analog and Digital Signals**
- **Be Careful with Sampling Clock and A/D Converter Analog Input Runs**
- **Be Careful with High Impedance Points**
- **Use Lots of Ground Plane**
- **Use Microstrip Techniques for Controlled Impedances**

Figure 11.53

If a ground plane is used, as it should in be most cases, it can act as a shield where-sensitive signals cross. Figure 11.54 shows a good layout for a data acquisition system

where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

PCB FLOWCHART

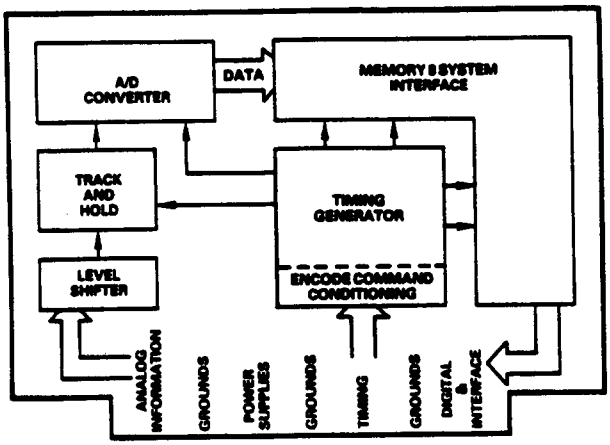


Figure 11.54

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins to reduce coupling between them.

EDGE CONNECTIONS

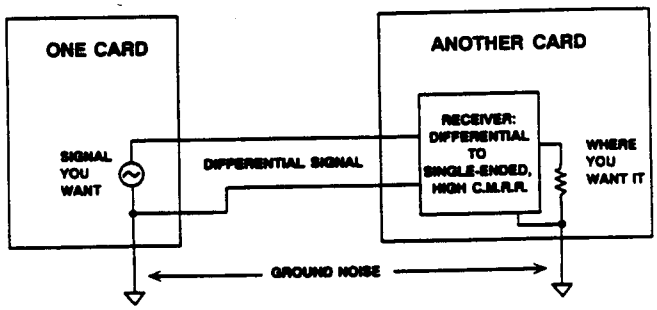
- **Separate sensitive signals by ground pins**
- **Keep down ground impedance with multiple (20-30% of total) ground pins**
- **Have several pins for each power line**
- **Critical signals may require a separate connector (possibly co-ax)**

Figure 11.55

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mohms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 20-30% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Modern high performance mixed signal systems handle signals with resolutions of 8 bits at sampling rates of over 500 MHz and resolutions of 14 bits sampled at more than 10 MHz. Preserving signal integrity between cards in a multi-card system is extremely difficult at such performance levels and may be impossible.

DIFFERENTIAL TRANSMISSION MINIMIZES GROUND ERRORS



- At DC and LF the receiver will be an instrumentation amplifier
- At HF the receiver will be a transformer
- There is no ideal receiver for video signals which have components from DC to HF

Figure 11.56

The use of balanced transmission lines can help but if the signal bandwidth extends to DC there will be a need for a very high performance instrumentation amplifier at the receiving end to restore a ground referenced signal.

VIDEO SIGNAL TRANSMISSION

- **It is often impossible to transmit very broadband high accuracy signals between the PCBs of a multicard system without unacceptable loss of quality.**
- **In such cases the system must be reconfigured to allow all the analog processing to take place on a single PCB.**
- **It may be inconvenient, but it's the only way you'll get it to work!**

Figure 11.57

The best, and in many cases the only, solution to problems of this sort, is to partition the system so that the highest quality signals are not transferred between boards.

Power Supplies

When we design an electronic circuit we generally assume that the power supplies provide noise-free power, at exactly the nominal voltage, with zero source impedance at all frequencies. This is rarely the case.

We also assume that the published power supply rejection figures (PSRR) for the devices which we use are valid at all frequencies from DC to light. This is rarely the case either.

POWER SUPPLY NOISE

- **Long-term voltage variation (Long-term variations in voltage or AC line voltage)**
- **AC Line noise (Both 100/120 Hz ripple on rectifier output and transient noise on the AC line which passes to the DC output)**
- **Switching noise (Digital noise from switching-mode power supplies)**
- **Power line noise transfer (Unwanted signals which pass from one part of a circuit to another via the common power supply)**

Figure 11.58

Power supply noise

Every power supply is noisy. This noise may contain long-term voltage drift, line ripple at 100 or 120 Hz, high frequency spikes from switching regulators, or all of these at once. Power supplies also have finite output impedance, so that if a circuit draws a varying current the supply voltage will vary with the current - if two circuits are supplied from a common supply this provides a mechanism whereby one circuit may affect the other. Once we appreciate all these effects we can attempt to quantify them, and take steps to minimize their adverse effects on our systems.

Long-term supply voltage changes, whether due to battery voltage drop during life or line voltage variations, are rarely a problem since where such variations might cause difficulties the system will incorporate a supply voltage regulator to keep variations within acceptable limits. Similarly ripple at twice the AC line frequency, and any spikes or HF noise which may enter the system via the AC supply, should not cause degradation of performance in a well-designed system: if the decoupling capacitors in the rectifier circuitry do not adequately minimize the effect, the series regulator almost certainly will. It is, however, always worthwhile to have a surge eliminator on the AC line input to any system - while such a circuit is unlikely to be needed in preventing normal line noise from currupting system performance, it is essential to prevent occasional large surges (from lightning or similar causes) from doing actual damage to the power supply or the system that it is powering.

Switching-mode power supplies

The commonest type of power supply noise is switching noise. Switching power supplies are small, cheap, efficient and, in too many cases, extremely noisy! Not only do they generate conducted noise, they are also efficient producers of capacitively coupled noise, magnetically coupled noise, and electromagnetically coupled noise. The best possible advice is not to use them.

SWITCHING-MODE POWER SUPPLIES

- **Generate every imaginable type of noise and some inconceivable ones as well!**
- **DO NOT USE THEM WHERE NOISE IS IMPORTANT.**
- **If their use is unavoidable do not relax and enjoy it, *but* take extreme precautions against all forms of noise.**
- **Remember that a manufacturer's design change in a bought-in switching-mode power supply may alter its effects on your system noise without altering its published specification.**

Figure 11.59

It is, unfortunately, not always possible to avoid the use of switching power supplies. Where they must be used they must be treated with the gravest suspicion and all possible precautions should be taken to prevent their noise from corrupting the analog circuits that they power. Their input and output lines should be decoupled at all frequencies, they should be shielded to prevent external electric and magnetic fields from causing interference, and they should be sited as far as possible from sensitive circuits so that residual electric and magnetic fields are prevented by distance from doing serious damage.

Where switching supplies are used it is always worthwhile to remove them temporarily and supply the system with batteries or a low noise bench supply in order to determine if the system performance is being compromised by the switching supply. It often is.

The noise transients on the output lines of switching supplies consist of voltage spikes of very short duration. As we have pointed out above, large capacitors, such as electrolytic or plastic film types, have quite considerable inductance and too high an impedance at HF to decouple such spikes satisfactorily. The best output filter for a switching supply will have high value capacitors to remove the low frequency noise which will also be present, and a pi filter using ceramic capacitors, with short leads having low impedance at HF, plus a series inductor (which may be a ferrite bead on the output line) to provide inductive blocking of the spikes. It is possible to buy such a pi filter as a single bulkhead mounted feedthrough component.

Electromagnetic Interference

Radio frequency interference

Noise can enter a circuit as electromagnetic radiation. Circuits can also generate electromagnetic radiation which can interfere with electronic devices at quite considerable distances away. Recent legislation in the United States, the European Community and many other countries sets limits on the amount of interference generated and the vulnerability of circuits to such interference.[7]

This legislation, and the techniques needed to comply with it, are the subjects of many seminars and training courses, and an Analog Devices Application Note.[8] It is not proposed to cover the topics in detail in this seminar.

ELECTROMAGNETIC NOISE GENERATION

- **Circuits must be designed so that external E/M fields are minimized.**
- **This is done by shielding, decoupling, minimizing the area of HF current loops and designing circuits which generate as little EMI as possible.**
- **IT'S NOT JUST A GOOD IDEA**
- **IT'S THE LAW!**

Figure 11.60

However, the principles of minimizing external radiation are closely related to the principles of low noise design which we have already discussed: high frequency and high dV/dT signals should be screened with Faraday shields, the area of current loops should be minimized, conductors should be decoupled at HF wherever unnecessary HF signals might otherwise occur, and external wires should be isolated with inductors or ferrite beads.

It is still too common at seminars like this to encounter skepticism about the need to protect circuitry from external electromagnetic fields. Even twenty years ago such skepticism was unjustified but today, when transmitters are ubiquitous, it is folly. Besides the more obvious broadcast, emergency and mobile radio services there are cellular and cordless telephones, radar, garage door openers and other remote controls, telemetry, and amateur and CB radio. For any designer to imagine that his circuit will never encounter a radio transmitter during its lifetime is folly on a grand scale.

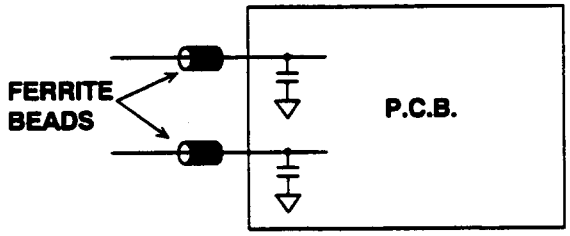
ELECTROMAGNETIC NOISE INTERFERENCE

- **The World is full of radio transmitters.**
- **Police, taxis, broadcast, amateur, CB, cellular and cordless telephones, telemetry and garage door openers.**
- **Do not imagine that your circuit will never encounter one.**

Figure 11.61

This is particularly so because the design of circuits which are immune to electromagnetic radiation of reasonable levels is not particularly difficult. If every conductor which leaves a PCB can be decoupled with a ceramic capacitor and a ferrite bead, it is probable that no further precaution is necessary.

EMI PREVENTION



IN MANY CASES, ALL THAT IS REQUIRED IS AN L FILTER, CONSISTING OF A FERRITE BEAD AND A CAPACITOR, ON EACH EXTERNAL CONNECTION TO THE BOARD

Figure 11.62

A few ports may be more vulnerable and require a pi filter rather than an L filter, and, of course, ports where an HF signal must actually enter or leave the board must be filtered to suppress other EMI but allow the signal to pass unaffected.

Boards which may be required to work in areas of high RF field should be screened with a conducting Faraday shield.

Photoelectric effects

Light is also a form of electromagnetic radiation and can effect semiconductor devices. Every silicon P-N junction is a photodiode, although their efficiencies vary widely. Wherever devices are not screened from ambient light, photoelectric effects may be observed.

Nearly all integrated circuits are encapsulated in light-tight packages (EPROMs are an exception, and it is possible to measure threshold changes in EPROMs as light intensity is varied, but since they are digital devices, and remain in specification despite light level changes, the effect is unimportant).

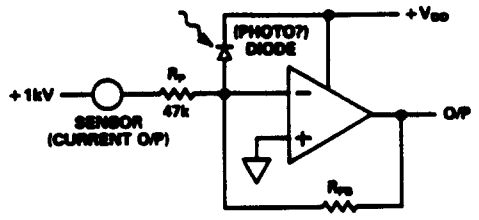
Diodes, on the other hand, are frequently encapsulated in translucent glass packages. When illuminated by light from fluorescent lamps, modulated at 120 or 100 Hz, they can act as a source of hum.

When the signal source of an op-amp contains an energizing voltage which is much higher than the op-amp supply it is common to use a diode and a current limiting resistor to protect the op-amp in the event of a sensor short-circuit. In normal operation the diode is reverse biassed and contributes only its (low) leakage current to the circuit but should the sensor be short-circuited the resulting current will flow through the diode to the op-amp supply rather than destroy the op-amp. It is, of course, important to choose the resistor so that it neither degrades the noise performance of the system nor allows too much current to pass under fault conditions.

The European Applications Department of Analog Devices encountered such a system where about 10% of all the amplifiers built suffered from severe hum at twice the power line frequency. The customer, of course, blamed the op-amp for poor supply rejection but analysis showed that even when the circuit was powered from batteries the problem persisted. The cause eventually turned out to be fluorescent lighting affecting the protective diode - a 1N914 in a glass case.

About 10% of diodes from the particular manufacturer were quite active as photodiodes and when illuminated by fluorescent lights their leakage current was modulated at 100 Hz (this was a European problem) - and the 100 Hz was, of course, amplified with the sensor signal. Use of a black epoxy packaged diode provided a complete cure.

UNEXPECTED PHOTOELECTRIC EFFECTS IN SILICON JUNCTIONS CAN DEGRADE CIRCUIT PERFORMANCE



THE DIODE PROTECTS THE OP AMP UNDER FAULT CONDITIONS BY DIVERTING FAULT CURRENT (LIMITED BY R_P) TO THE SUPPLY RAIL. THE DIODE SHOULD NOT BE PHOTO-RESPONSIVE, OTHERWISE FLUORESCENT LIGHTING MAY MODULATE ITS LEAKAGE CURRENT AT 100/120Hz AND CAUSE HUM. USE A PLASTIC DIODE - NOT A GLASS ONE.

Figure 11.63

Logic

The majority of this section of our seminar has considered problems within the analog parts of mixed signal systems. Despite their much greater noise immunity, the digital parts of these systems can also suffer from designers' lack of consideration of basic laws. Common problem areas include bus interface issues, including fan-out and timing, for both converters and DSP processors, the care and feeding of sampling clocks, and the design of systems which generate minimum noise (we have already discussed how to keep logic noise from affecting the analog parts of a system - this task becomes easier if the logic noise is minimized in the first place).

DIGITAL PROBLEM AREAS IN MIXED SIGNAL SYSTEMS

- Bus interface - fan-out
- Timing variations
- Sampling clock jitter
- Logic noise

Figure 11.64

FAN-OUT

All Analog Devices' DSP processors, and most of their DSP ADCs, have TTL-compatible CMOS logic ports. The inputs have $V_{il(max)}$ of 0.8 V and $V_{ih(min)}$ of 2.0 V, while the outputs have $V_{ol(max)}$ of 0.4 V and $V_{oh(min)}$ of 2.4 V at particular currents. The DSP processors are also rated for the capacitive load that they will drive without degradation of their timing.

In order to determine the fan-out of such devices it is necessary to consider the curren that they are called upon to source and sink and the capacitance that they will see. This is done from the data sheets of the devices that they will be called upon to drive.

FACTORS LIMITING LOGIC FAN-OUT

- **Maximum available source current (logic high): Dominant factor for *resistive* loads**
- **Maximum available sink current (logic low): Dominant factor for *TTL* loads**
- **Maximum permitted node capacitance: Dominant factor for *CMOS* loads**
- **Node capacitance has contributions both from the input capacitances of gates on the node and from wiring and PC tracks associated with the node.**

Figure 11.65

Consider a typical fast TTL gate, such as the 74F32 OR-gate. Its maximum input high current ($I_{ih(max)}$) is 20 µA, its maximum input low current ($I_{il(max)}$) is 0.6 mA and its maximum input capacitance is 5 pF. An ADSP-2100 will source 1 mA when its output is high, it will sink 4 mA when its output is low, and it will drive capacitance of up to 100 pF.

The ADSP-2100 will therefore drive the capacitance of 20 74F32 gates, it will drive the input current of fifty such gates in the logic 1 (high) state, but it will sink the input current of only 6.7 (in practical terms, 7) such gates. The lowest of these is evidently the fan-out which it will drive.

In typical systems it is likely that a device will be called upon to drive a mixture of devices, so the calculations will be more complex - but the basic principle will be the same. In most systems involving TTL the fan-out will be limited by the sink current, but in CMOS systems the node capacitance is likely to be the limiting factor. The above calculations do not consider the capacitance of the PC tracks and any cables which the

ADSP-2100 DRIVE CAPABILITY

- **Will drive 100 pF**
- **Will drive 1 mA at logic 1 (≥2.4 V)**
- **Will sink 4 mA at logic 0 (≤ 0.4 V)**

Therefore it will drive:

- **22 74ACT CMOS Gates (= 99 pF, ±22 µA)**
- **10 74LS Schottky TTL Gates (= –4 mA)**
- **7 74F Schottky TTL Gates (= –4.2 mA)**
- **1 Grounded 2.4 k resistor (= 1 mA)**
- **Or any combination of loads which does not exceed a total capacitance of 100 pF, a total drain of 1 mA at logic 1, and a total source of 4 mA at logic 0. (Remember to allow for the capacitance of PCB tracks and wiring.)**

Figure 11.66

device may be called upon to drive but such capacitance can sometimes be a limiting factor, and should always be considered, if only to be eliminated.

Most data converters have less powerful output stages than processors and their fan-out is lower. Additionally the return current of the output drive from a converter will flow in the system analog ground (for reasons discussed earlier in this section) and should therefore be kept as low as possible in order to minimize digital noise in the analog part of the system.

This is best achieved by using CMOS, rather than TTL logic. The DC input currents of CMOS are orders of magnitude lower that those of TTL. However, the input capacitances are comparable so the switching transients are not much lower. It is therefore advisable to buffer ADC outputs with an external buffer to minimize digital output currents from the ADC. Such a buffer will also help to isolate the ADC from digital noise in the rest of the system.

TIMING VARIATIONS

A common cause of malfunctions in digital systems, and particularly in the digital parts of mixed signal systems, is timing error, which often arises from failure to consider the effects of temperature variations on the system.

The specifications of converters, memories and processors all contain such parameters as "set-up" and "hold" times. These are the times, respectively, that data must be present before a clock edge may occur, or that it must remain valid after the edge. At room temperatures many digital circuits are quite

tolerant of operation with set-up and hold times which are shorter that the specified minimum - but at extremes of temperature they may be more demanding.

LOGIC TIMING VARIES WITH TEMPERATURE

- **Specifications such as "set-up" & "hold" (the time a signal must be present before a strobe and the time that it must remain after one, respectively) can vary widely with temperature.**
- **A system designed with room temperature "typical" values may only perform properly at room temperature, if then.**
- **Designers MUST use min/max specifications at temperature extremes to ensure correct operation at all times.**

Figure 11.67

Where a system consists only of digital circuitry it is likely (but not certain) that changes in input and output timing will behave similarly so that systems continue to function over temperature. Where ADCs or DACs are interfacing with digital systems the very different processes used for the converters may result in timing changes not tracking and performance, or even functionality, suffering.

Engineers designing mixed signal systems should always ascertain that the maximum and minimum timing specifications of all the circuits in their systems are compatible over the full temperature range of intended operation. Where there is any doubt buffers or monostables should be used as pulse extenders to ensure that all set-up and hold specifications are complied with.

SAMPLING CLOCK NOISE

As has been mentioned elsewhere in this seminar, phase noise on the clock of a sampled data system is indistinguishable from phase noise on the signal itself and it is therefore of critical importance to ensure that the sampling clock has sufficient spectral purity that its phase noise is less than the smallest component to be detected in the signal under analysis.

To achieve this the sampling clock should be isolated as much as possible from the noise present in the digital parts of the system. In particular, buffers used for the sampling clock should, ideally, be on separate chips, with separately decoupled supplies, from the remainder of the digital system, and the sampling clock signal lines should not be sited where they can pick up digital noise from the rest of the system.

SAMPLING CLOCK NOISE

- **Phase noise of the clock must be less than the minimum signal to be detected in the system.**
- **Therefore the sample clock signal must be protected from digital noise.**

BUT

- **Clocks are digital and can corrupt the analog part of the system.**
- **Therefore sampling clock lines must be kept separate fro m both the analog and the digital parts of the system.**
- **The sampling clock must use an oscillator with low phase noise.**

Figure 11.68

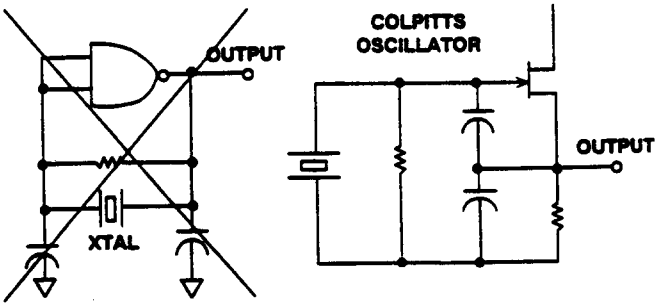
Of course the sampling clock is itself a digital signal. It has as much potential for causing noise in the analog part of the system as any other digital signal. In fact, due to its presence in the converter and SHA sections of a system, it is generally the leading suspect for noise. We therefore see that a sampling clock is very inconvenient as it must be isolated from both the analog and digital parts of the system.

The sampling clock generator must also have adequate spectral purity. RC and other relaxation oscillators just will not do since amplitude noise in whatever circuit functions as a comparator will appear as phase noise on the output signal. LC oscillators have better phase noise, but the lowest noise is obtained with the use of a quartz crystal oscillator. For very high speed clocks a SAW (surface acoustic wave) oscillator is preferable.

A popular design of quartz crystal oscillator uses a resistor, one or more logic gates, a quartz crystal and a couple of capacitors. The design is not popular with engineers who understand quartz crystals or oscillators - such designs have bad phase noise and are liable to overdrive the quartz crystal (not enough to shatter it, as sometimes happened with self-excited crystal-controlled transmitters using vacuum tubes, but enough to affect its long-term stability). The only justi-

fication for the use of such oscillators is in watch and clock circuits where the low voltages involved minimize the overdrive and the phase noise is integrated over long periods and so is unimportant.

OSCILLATORS



Crystal oscillators built with logic gates have large phase noise.

Low noise crystal oscillators are easily designed with discrete components.

Figure 11.69

Ideally quartz oscillators should use discrete bipolar and FET devices in the circuits recommended by the crystal manufacturers. These circuits are optimized for both crystal drive level and phase noise. The output signal can then be amplified (possibly with a logic gate at this point) to drive the converters.

Logic Noise

One of the most common causes of loss of performance in mixed signal systems is degradation of analog performance by noise from the digital parts of the system. We have already discussed at some length how this digital noise may be isolated from the sensitive analog parts of the system, but it is also worthwhile considering how this noise may be diminished at its source.

It is well-known that TTL is noisy. This is partly because the "totem pole" output stage structure acts as a short-circuit on the supply for a nanosecond or so during switching - giving rise to a large current spike, partly because the current flowing in the input changes, and changes quickly, between logic 0 and logic 1, and partly because the output swing, which takes place in a few nanoseconds, is several volts.

High speed CMOS does not have the change in input current (although there is a capacitance charging current pulse during switching, this is smaller) but may draw a supply current pulse during switching and certainly has a large output swing with a large dV/dT.

4000-Series CMOS is almost 20 years old and slow. It is also widely available, cheap, resistant to RFI, and quite remarkably noise free, since it has low output dV/dT and does not generate a supply current pulse.

LOGIC NOISE

- **TTL has large voltage swings; large, fast I/P & O/P current pulses and asymmetrical circuitry.**
- **HCMOS has large voltage swings; large, fast O/P current pulses and symmetrical circuitry.**
- **4000-Series CMOS is old, slow, cheap and very quiet.**
- **ECL has smaller voltage swings and smaller current surges than TTL & HCMOS even though it is faster.**
- **There is no single ideal logic family.**

Figure 11.70

ECL also draws almost constant current during switching (unless it is driving asymmetrical loads) and has much smaller output voltage swings than TTL or CMOS. Thus, although ECL is faster than TTL and CMOS, it tends to generate less noise.[9]

No single logic family is ideal for all applications (otherwise there would only be one logic family) but it is safe to conclude that TTL should not be used where its noise can corrupt precision analog circuitry but should be replaced by CMOS.

Where only low speeds are necessary 4000 CMOS has overwhelming noise advantages but may not be available in all necessary configurations, and does not interface well with TTL (although it will interface with high speed CMOS families).

In high speed systems where noise is important ECL may offer noise advantages at the interface between the analog and digital parts of the system, even though high speed CMOS is capable of the speeds being used. It is not necessary to use ECL throughout the system - just where its lower noise is advantageous.

Problem Areas

Limitations of SPICE modelling

As we have seen, real electronic circuits contain many "components" which were not present in the circuit diagram but which are there because of the physical properties of conductors, circuit boards, IC packages, etc. These components are difficult, if not impossible, to incorporate into computer modelling software and yet they have substantial effects on circuit performance at high resolutions, or high frequencies, or both.

It is therefore inadvisable to use SPICE modelling or similar software to predict the ultimate performance of such high performance analog circuits. After modelling is complete the performance must be verified by experiment.

This is not to say that SPICE modelling is valueless - far from it. Most modern high performance analog circuits could never have been developed without the aid of SPICE and similar programs, but it must be remembered that such simulations are only as good as the models used and these models are not perfect. We have seen the effects of parasitic components arising from the conductors, insulators and components on the PCB, but it is also necessary to appreciate that the models used within SPICE simulations are not perfect models.

Consider an operational amplifier. It contains some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE model will contain all these components and probably a few of the more important parasitic capacitances and spurious diodes formed by the diffusions in the op-amp chip. This is the model that the designer will have used to evaluate the device during his design. In simulations such a model will behave very like the actual op-amp, but not exactly.

However, this model is not published, as it contains too much information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing such models of a number of op-amps to reach a useful result. For these, and other, reasons

SPICE MODELLING

- **SPICE modelling is a powerful tool for predicting the performance of analog circuits.**

HOWEVER

- **Models omit real-life effects.**
- **No model can simulate all the parasitic effects of discrete components and a PCB layout.**

THEREFORE

- **Prototypes must be built and proven before production.**

Figure 11.71

the SPICE models of analog circuits published by manufacturers or software companies are "macro" models, which simulate the major features of the component but lack some of the fine detail. Consequently SPICE modelling does not always reproduce the exact performance of a circuit and should always be verified experimentally.

Sockets

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- **DON'T! (If at all possible)**
- **Use "Pin sockets" of "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).**
- **Always test the effect of sockets by comparing system performance with and without the use of sockets.**
- **Do not change the type of socket used without evaluating the effects of the change on performance.**

Figure 11.72

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon not to degrade the performance of high performance (high speed or high precision or, worst of all, both) devices, and as the socket ages and the board suffers vibration the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the least loss of performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. Nevertheless this approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multicard system.

PROTOTYPING
MIXED SIGNAL CIRCUITRY

- **NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).**
- **Wherever possible avoid the use of sockets for analog ICs.**
- **Use a prototype of your final PCB layout as early as possible.**

Figure 11.73

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient this is not essential), with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in the references at the end of this section.[10]

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

ADDITIONAL PROTOTYPING HINTS

- **Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.**
- **Verify performance as well as functionality at each stage of the design.**
- **For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mountadhesive PC pads if aerial point-to-point wiring seems too fraught with peril).**

Figure 11.74

REFERENCES

1. Albert Einstein
2. "E.S.D. Prevention Manual" Available free from Analog Devices.
3. For a discussion of these effects see pp I-11 et seq. "Linear Design Seminar" notes. Analog Devices, October 1987.
4. "Electricity & Magnetism" by B.I. & B. Bleaney. OUP 1957, pp 23,24, & 52.
5. "An I.C. Amplifier User's Guide to Decoupling, Grounding and Making Things Go Right for a Change" by Paul Brokaw. Available free of charge from Analog Devices.
6. "Avoiding Ground Problems in High Speed Circuits", Jeff Barrow "R.F. Design" July 1989. AND "Grounding for Low- and High-Frequency Circuits", Paul Brokaw & Jeff Barrow, "Analog Dialogue" 23-3 1989. Free from Analog Devices.
7. International EMI Emission Regulations

Canada	CSA C108.8-M1983	FDR	VDE 0871/VDE 0875
Japan	CISPR (VCCI)/PUB 22	USA	FCC-15 Part J

8. "Design & Layout of a Video Graphics System for Reduced EMI" Bill Slattery & John Wynne (E1309-15-10/89). Free from Analog Devices.
9. "MECL System Design Handbook" 4th Edition, 1983 - Motorola
10. Wainwright Instruments Inc.
P.O.Box 2203, Capistrano Beach, CA 92624. Tel: 714-248-2490

Wainwright Instruments GmbH, Widdersberger Strasse 14,
DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-2245