ANALOG DEVICES

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APPLICATION NOTE

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CMOS DACs and Op Amps Combine to Build Programmable Gain Amplifiers Part I

by John Wynne

The ability to software program the gain of an amplifier can be very useful to designers. Allied to this ability is the requirement for a large number of programmable gain levels and not simply 3 or 4 user selectable gain levels. CMOS DACs are a natural choice for control of a PGA circuit – not only do they satisfy the above two requirements but they are low cost and can be highly accurate. The traditional way of using CMOS DACs to build a PGA is to place the DAC in the feedback loop of a simple inverting op amp configuration. The DAC behaves as a programmable resistance and thus allows the circuit gain to be digitally controlled. High circuit gains require large values of effective feedback resistance. However, as the effective feedback resistance increases, its precise value becomes less and less defined. This results in a circuit whose gain accuracy decreases with increasing gain. This application note is published in two separate parts. Part I looks at the PGA circuits based upon a single DAC and analyzes the gain errors arising from such a configuration. It also includes an analysis of the dc error sources which limit the dc accuracy of the PGA. Two recently released CMOS DACs from Analog Devices, the AD7534 and AD7538, combine a number of features which make them suitable for use in a PGA circuit. The AD7534 is in a 20-pin, 0.3″ wide package and loads data in an 8+6 format. The AD7538 is in a 24-pin, 0.3″ wide package and has a 14-bit parallel loading format. Both have similar specifications. A detailed comparison is made between the performance of a PGA circuit based on the 14-bit AD7534 and one based on a 12-bit AD7545. In Part II of the application note, PGA circuits built with dual DACs are investigated. These circuits offer the advantage of greater accuracy over a wider dynamic range in comparison with a single DAC solution. Monolithic dual 8-bit (AD7528) and 12-bit (AD7537, AD7547 and AD7549) DACs are now available which make this a cost effective solution.

THE BASIC EQUATIONS

Turning a DAC into a PGA element simply involves placing the network in the feedback path as opposed to the input path of an inverting op amp circuit configuration. Both configurations are shown in Figure 1. The transfer function of Figure 1a is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_{FB}}{R_{EQ}} \quad (1)$$

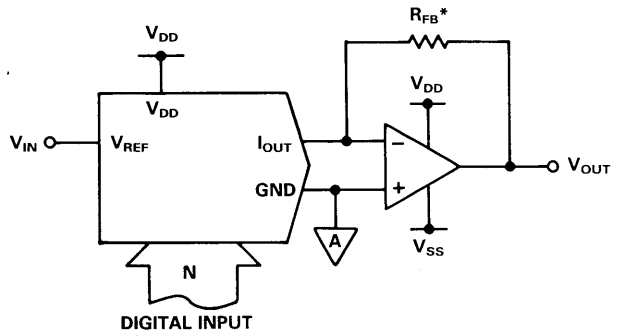

Figure 1a. Standard DAC Configuration to Provide Attenuation

R_{EQ} is the equivalent transfer impedance of the DAC from the V_{REF} pin to the I_{OUT} pin and can be expressed as

$$R_{EQ} = \frac{2^n R_{IN}}{N} \quad (2)$$

where: n is the resolution of the DAC

N is the DAC input code in decimal

R_{IN} is the constant input impedance of the DAC ($R_{IN} = R_{LAD}$ for an R-2R DAC)

Substituting this expression into Equation 1 and assuming zero gain error for the DAC ($R_{IN} = R_{FB}$) the transfer function simplifies to

$$\frac{V_{OUT}}{V_{IN}} = -\frac{N}{2^n} \quad (3)$$

This ratio is commonly represented by D and, as such, is a fractional representation of the digital input word, i.e.

$$\frac{V_{OUT}}{V_{IN}} = -D \quad (4)$$

When the DAC network and the feedback resistor R_{FB} are swopped around as in Figure 1b, the ideal transfer function is obviously the inverse of Equation 3 or

$$\text{GAIN IDEAL} = \frac{V_{OUT}}{V_{IN}} = \frac{-2^n}{N} = \frac{-1}{D} \qquad (5)$$

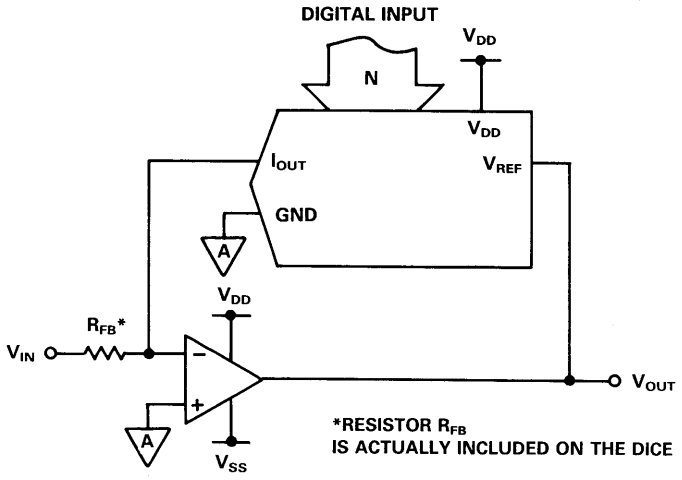

Figure 1b. Transposed DAC Configuration to Provide Gain

With an 8-bit DAC, Equation 5 indicates that the gain of the circuit can be varied from 256 (an input code of 00000001) down to unity (actually 256/255, an input code of all 1s) in 255 steps. The all 0s code is never applied. This avoids an open-loop condition thereby saturating the amplifier. With the all zeros on (all bits off) code excluded there remains $2^n - 1$ possible input codes allowing a choice of $2^n - 1$ output levels. In dB terms, the dynamic range is

$$20 \log_{10} (2^n - 1) \qquad (6)$$

For an 8-bit device the dynamic range is approximately 48dB. Increasing the resolution of the converter by 1 bit increases the dynamic range by 6dB. Thus a 12-bit device will have a maximum dynamic range of 72dB. Closely allied to the number of programmable gains available is their distribution over the gain range from minimum gain to maximum gain. Figure 2 is a graphical representation of Equation 5 with the circuit gain plotted in dB for an 8-bit DAC. The graph indicates that one half (128) of the total number of steps or LSBs available cover the 0 to +6dB range (gains from 1 to 2), one quarter (64) of the steps cover the next 6dB of gain (+6 dB to +12dB or gains from 2 to 4), one eighth(32) of the steps cover the next 6dB (+12dB to +18dB or gains of 4 to 8), etc. Figure 2 illustrates quite clearly the decreasing number of gain steps available as the circuit gain increases in 6dB bands. From Figure 2 it can be seen that the last 6dB gain band (+42dB to +48dB or gains of 128 to 256) is covered in just one step. This occurs when the DAC digital code changes from decimal 2 to decimal 1. Thus most of the programmable gain steps are concentrated at the lower end of the gain range offering tremendous resolution between adjoining gain settings (less than 0.05dB). Figure 2 might suggest that this step "bunching" is the only drawback of the PGA circuit. This is not so. When the various error sources are taken into account, the actual performance falls quite short of the ideal.

DEFINING THE ERRORS

The main culprit in the performance shortfall is the DAC Integral Linearity which causes a rapid deterioration in system accuracy with increasing gain. The reason is not hard to see. For example, with an 8-bit DAC and a required gain of 16, the DAC input code is decimal 16. If the DAC is 8-bit linear, i.e. ±0.2% F.S. or ±1/2LSB, then the effective input code can vary from 15.5 up to 16.5. This means the system gain of equation 5 can vary from 256/15.5 (or 16.51) down to 256/16.5 (or 15.51) – an error of ±3% even

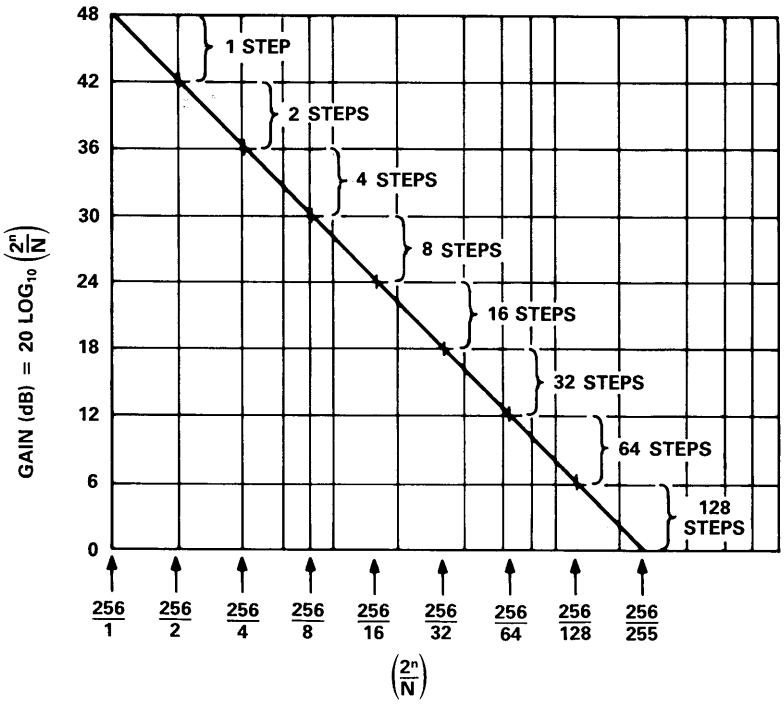

Figure 2. Step Distribution in dB vs. Digital Code for an 8-Bit DAC

though the DAC itself has a maximum error of ±0.2%. Higher gains produce correspondingly higher errors.

The transfer function of Equation 2 assumed that there was no gain error in the DAC. DAC gain error does exist, however, and it results in the ideal gain expression of Equation 5 being multiplied by a term close to unity. The smaller the gain error then the closer this multiplier term is to unity. When both linearity errors and gain errors are included, the system gain expression becomes

$$\text{GAIN ACTUAL} = \frac{V_{OUT}}{V_{IN}} = -\frac{2^n}{(N+X)(1+\Delta)} \qquad (7)$$

Where X is the linearity error in LSBs

$$\text{and } (1+\Delta) = \frac{R_{FB}}{R_{IN}}$$

The difference between the ideal gain and the actual gain can be expressed in percentage terms as

$$E(\%) = -\left[\frac{\Delta}{(1+\Delta)} + \frac{1}{(1+\Delta)}\left(\frac{X}{N+X}\right)\right]\cdot 100\% \qquad (8)$$

Since the gain error of a DAC can be trimmed to zero whereas nothing can be done to reduce the integral nonlinearity, it is instructive to consider the percentage gain error due to DAC nonlinearity alone and then to add the DAC gain error term.

Quick Rule-of-Thumb Helps

With zero DAC gain error equation 8 simplifies to

$$E(\%) = -\left(\frac{X}{N+X}\right)\cdot 100\% \qquad (9a)$$

This expression applies for all gain settings except unity when an additional error term must be added to Equation 9a. For any R-2R ladder network the maximum output current (with all 1s applied to the DAC) is always 1LSB less than the input current. The "missing" LSB worth of current flows through the ladder termination resistor to signal ground. Therefore, at a gain setting of unity, a unique error term equal to 1LSB in percent must be added to the percentage error expression of Equation 9a.

By rearranging Equation 9a, the percentage gain error can be usefully expressed in terms of the programmed gain and DAC linearity (accuracy) as

$$E(\%) = -\left(\frac{2^n}{N+X}\right)\left(\frac{X}{2^n}\cdot 100\%\right) \qquad (9b)$$

or, in words, the maximum percentage gain error is equal to the required gain times the DAC linearity in percent. This is a quick rule-of-thumb for estimating output error for gains greater than unity. The solid line in Figure 3 is a graphic representation of Equation 9a plotted for a 12-bit accurate, 12-bit resolution DAC and shows the increasing gain error with increasing gain. For comparison purposes, a plot for a 14-bit accurate, 14-bit resolution DAC is represented by the dotted line in Figure 3. Because the linearity error X can be either positive or negative, the vertical axis of Figure 3 is graduated in terms of ±E(%). Figure 3 is, however, an approximation, albeit a good one, of Equation 9a. The straight line representation of error versus gain in Figure 3 suggests that the maximum positive and negative gain errors are symmetrical over the entire gain range. In fact at very high gains the maximum gain errors become noticeably asymmetric and continue to be increasingly asymmetric with increasing gain.

This is due to the ±X linearity term in the denonimator of Equation 9a having an increasing impact with increasing gain (N reducing). The magnitude of the asymmetry can be seen from the results in Table A1 of Appendix 1 which shows computed values of Equation 9a for the AD7545LN

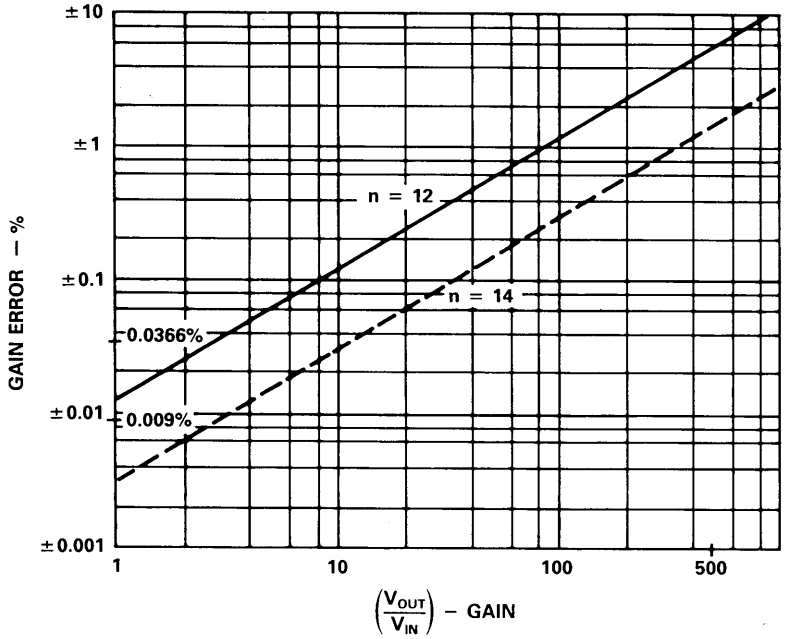

Figure 3. Comparison of Worst Case Gain Errors Between PGA Systems Based on a 12-Bit Resolution, 12-Bit Accurate DAC and a 14-Bit Resolution, 14-Bit Accurate DAC. DAC Gain Error is Zero in Both Cases.

using both positive and negative linearity terms. For instance, at a gain of 128, the maximum positive gain error is +1.587% and the maximum negative gain error is −1.538%, an imbalance or asymmetry of 0.049%. At a gain of 16 the gain error asymmetry is 0.008%, a vanishingly small number. For low gain settings, Figure 3 is thus a good approximation of the gain errors to be expected from a DAC-based PGA circuit with zero DAC gain error. At the all 1s or unity gain setting, the effect of the LSB worth of signal current "lost" in the ladder termination is to always increase the gain, albeit only slightly, over unity. For the computed AD7545LN values shown in Table A1, the X1 gain error figures include the additional term of 1LSB or +0.0244%.

DAC Gain Error Causes Skew

When a DAC with non-zero gain error is used, the more complete Equation 8 must now be used to compute the total error. From inspection of Equation 8, non-zero DAC gain error has two effects; the first is to multiply the error results of the previous analysis by a term $\frac{1}{(1+\Delta)}$ which is close to unity. The overall effect of this is small and serves only to increase or reduce the gain asymmetry error at any given gain setting. (Positive DAC gain error reduces the asymmetry.) The second and major effect of DAC gain error is to add an error term which is independent of gain setting. Since the term is constant, it has the greatest impact at low gain settings and serves to skew the transfer curve of Figure 3 either in a positive or negative direction. (Positive DAC gain error obviously causes a negative skew.) Table A2 in Appendix 1 shows computed values of Equation 8 for all combinations of DAC gain error and linearity error. The unity gain figures include an additional +0.0244% error term due to the ladder termination. The worst case values from this table are used to plot Figure 4. Shown dotted in this figure is the transfer curve of Figure 3. Thus even with a 12-bit resolution, 12-bit accurate DAC (X = ±1/2LSB) having a tight gain error specification of ±5 LSBs, the worst case system gain error can be as large as 0.159% for a gain of 1.

The gain error analysis leading to Figure 4 assumed that the loop gain of the system is sufficiently high so as to cause no appreciable error. With the AD OP-07 this is a valid assumption at dc and low frequencies if extreme gain settings are avoided. Exactly how the loop gain affects the gain error can be seen from the first term in expression A7 of Appendix A2. At high signal frequencies and high gain settings the finite loop gain can contribute to the gain error of the system. This topic is dealt with in greater detail in Part II of this application note.

ADDITIONAL ERROR SOURCES CAUSE DC OFFSET ERRORS

Gain errors such as these are not the only errors which affect the PGA circuit of Figure 1b. Additional error sources result in a gain-dependent dc offset voltage at the op amp output. The additional DAC-related error sources are code-dependent output resistance and output leakage current. Op amp-related error sources are input offset voltage, input bias current and finite open loop gain. Appendix 2 outlines the contribution of each individual error source to the output. Assume the requirement is for a PGA with gains from 1 to 64. Assume also that the components available are the AD7545LN and the AD OP-07E. The relevant specifications for these components at 25°C are shown in Tables I and II. When the min/max figures from Tables I & II are substituted into Equation A7, the worst case output voltage (occurring for $N = 64_{10}$, i.e. Gain of 64) is equal to

$$V_{OUT} = -64.58\,V_{IN} \pm 29.1\text{mV} \qquad (10)$$

Gain error is approximately 0.9%. Only 6.5mV of the total dc offset error term of 29.1mV is due to the input offset

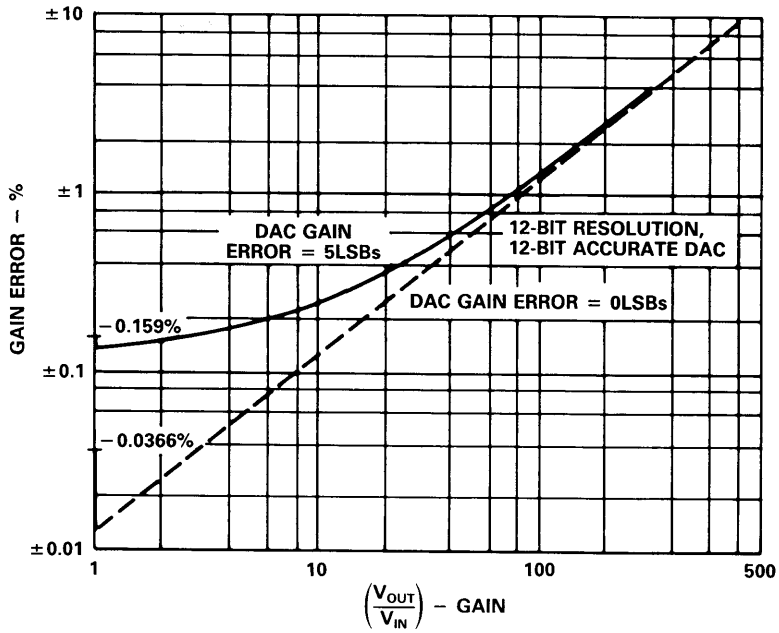

Figure 4. Theoretical Worst Case Gain Errors for AD7545-Based System with and without DAC Gain Error

voltage V_{OS}; the remainder is due to both DAC leakage current I_{LKG} (the major contributor at 16.1mV) and op amp input bias current $I_B(-)$. For the purpose of calculating the op amp input offset voltage error term, a value of $R_0 = 3$ R_{FB} was used in A7. If V_{IN} is a dc signal, then the dc offset error of 29.1mV will be indistinguishable from the output signal. Referring the dc offset error term to the system input results in an equivalent input error of 29.1/64mV or 0.455mV. The smallest input signal V_{IN} for less than, say, 1% error at the X64 gain setting is thus 45.5mV. This error is in addition to the gain error of 0.9%.

Errors Increase with Temperature

If the PGA is expected to perform accurately over a wide temperature range, the drift performance of the error sources with temperature will be important. To a greater or lesser extent all of the terms in Equation A7 are temperature sensitive. A similar analysis of the circuit at, say, 70°C using the data specifications indicates that the gain error will remain essentially unchanged but that the dc offset error can increase dramatically. Over this temperature range, the input offset voltage can increase by nearly 80%, the input bias current by 40%, but the already dominant component, DAC leakage current I_{LKG}, can increase by 400%. When these worst case percentage increases are translated into output voltages, the input offset voltage term can add 5.2mV; the input bias current term can add 2.5mV, but the DAC leakage current term can add 64mV. However, experience shows that the DAC leakage current really only begins to increase at temperatures greater than 85°C. A representative plot of DAC output leakage current versus temperature for a CMOS DAC is shown by the solid line in Figure 6. If the PGA circuit must operate over the military temperature range of −55°C to +125°C, then AD7545UD and AD OP-07H grade devices must be used in place of the previous commercial grades. Tables I and II show the relevant specifications of these high-temperature devices. Using these figures in Equation A7 the output voltage of the PGA at +125°C is

$$V_{OUT} = -64.59\,V_{IN} \pm 349.6\text{mV} \qquad (11)$$

Parameter	AD OP-07E $T_A = +25°C$	AD OP-07E $T_A = +70°C$	AD OP-07H $T_A = +125°C$
Open Loop Gain, A_{OL}	2.10^6 min	$1.8.10^6$ min	$1.5.10^6$ min
Input Bias Current, $I_B(-)$	4nA max	5.6nA max	6nA max
Input Offset Voltage, V_{OS}	75μV max	134μV	200μV max

NOTE: $V_{DD} = +15V$, $V_{SS} = -15V$

Table I. AD OP-07 Specifications at $T_A = +25°C$, +70°C & +125°C

Parameter	AD7545LN $T_A = +25°C$	AD7545LN $T_A = +70°C$	AD7545UD $T_A = +125°C$
Resolution, n	12-bits	12-bits	12-bits
Relative Accuracy, x (Integral Linearity)	±1/2LSB max	±1/2LSB max	±1/2LSB max
Gain Error	±5LSBs max	±6LSBs max	±6LSBs max
Output Leakage, I_{LKG}	10nA max	50nA max	200nA max
Input Resistance, R_{IN}	25kΩ max	25kΩ max	25kΩ max

NOTE: $V_{DD} = +5V$

Table II. AD7545 Specifications at $T_A = +25°C$, +70°C & +125°C

Programmed gain of the circuit is again 64. The gain error is virtually unchanged from its 25°C value as shown in equation 10. The dc offset errors, though, have increased by an order of magnitude. Of the 349.6mV, the op amp bias current contributes 9.7mV; the input offset voltage contributes 17.4mV, while DAC leakage current accounts for the remaining 322.5mV. Referring the 349.6mV to the system input results in an equivalent input error, for the X64 gain setting of 349.6/64mV or 5.5mV. The smallest dc input signal V_{IN} for less than 1% error at the X64 gain setting is thus 550mV. This is at +125°C and is an order of magnitude greater than the minimum input signal at +25°C. Table IVa lists the gain and dc offset errors derived from Equation A7 at +25°C, +70°C and +125°C when using the 12-bit AD7545.

REDUCING THE ERRORS

Gain Errors

From the graphical representation in Figure 4 a somewhat surprising conclusion can be drawn. In precision applications, DAC gain error is as significant a contributor to system error as is DAC integral linearity. This is because any DAC gain error results in a constant error term having the greatest impact on the most accurate gain settings. For example, at a gain setting of 1, the error from Figure 4 is ±0.159%. This is for a 12-bit resolution, 12-bit accurate DAC with a DAC gain error of ±5LSBs. If DAC gain error did not exist – dotted line in Figure 4 – the maximum system error would be ±0.036%, one fifth of its previous value. It is of course possible to trim the DAC gain error to zero by means of a potentiometer. However, the temperature coefficients of the trim components will differ from that of the thin-film ladder resistors of the DAC resulting in a change in DAC gain error over temperature. This topic of trimming CMOS DACs for minimum drift is dealt with extensively in Reference 1.

As the programmable gain setting is increased (N reducing), DAC integral nonlinearity becomes the dominant contributor to the system gain error. For example, at a gain setting of 64, the system error from Figure 4 is approximately ±0.9%, of which ±0.78% is due to DAC integral nonlinearity. In place of the single gain stage, two series-connected gain stages can be used to provide the same overall gain. Since the product of the gain settings of the individual stages is equal to the overall gain, individual stages can now have much lower gain settings and hence higher accuracy. If two stages are available, each having a similar performance to that shown in Figure 4, then for the same overall gain setting of 64 (individual gain settings of 8), the system gain error is approximately ±0.44%. More than half of this error is due to DAC gain error. In order to keep overall system cost, complexity and size to a minimum, monolithic dual 8-bit and 12-bit DACs are now available from Analog Devices which are well suited for this application. The AD7528 is a dual 8-bit DAC with a parallel loading structure. The AD7537, AD7547 and AD7549 are dual 12-bit DACs with 8+4, full-parallel and nibble (4-bits) loading structures respectively. The performance of these circuits is investigated in Part II of the application note.

DC Offset Errors

Depending on the application, the dc offset errors may or may not be significant. The most obvious solution to eliminating these dc voltages is to ac couple the output signal. However, this may not always be possible even in those applications where dc levels are unimportant. If the frequency of interest extends down to, say, a few Hertz, there will be a conflict between choosing a value (and hence, a physical size) for the coupling capacitor and suffering an increase in gain errors due to low frequency fall-off. Depending on the circuit performance required and on the specific application a designer can identify the most important circuit parameters and accordingly choose components for the most cost-effective solution.

DAC output leakage current is very much the major contributor to dc offset errors – especially at high temperatures. To date CMOS DACs with low output leakage currents over the military temperature range have not been available.

A SINGLE DAC SOLUTION

Two recently introduced high resolution CMOS DACs from Analog Devices boast specifications which are close to the ideal for a DAC operating in the PGA mode. The AD7534 and AD7538 are low-cost 14-bit resolution DACs with extremely tight DAC gain error specifications, ±4LSBs maximum. Coupled with 13-bit accuracy specifications and a patented low-leakage technique (US Pat No. 4,590,456) which maintains a very low-leakage current at high temperatures, both gain and dc offset errors are much reduced over the previous case. Table III shows the relevant specifications for the AD7534KN at +25°C. Figure 5 is a graphical representation of Equation 8 plotted for the AD7534KN. Shown dotted in the figure is the graphical representation of Equation 9 – where DAC gain error is assumed to be zero. These curves should be compared with those of Figure 4. Tables A3 and A4 in Appendix 1 show computed values of Equations 9 and 8 respectively for all combinations of DAC gain error and linearity error.

A dedicated pin (V_{SS}) is available on the AD7534 which can be tied either to 0V (normal DAC output leakage) or tied to −300mV (reduced DAC output leakage) to implement the patented low-leakage scheme. Figure 6 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low-leakage scheme. If the relevant specifications from Table III are substituted into equation A7 (using AD OP-07E specifications from Table I), the worst case output voltage at a gain of 64 (occurring for $N = 256_{10}$) is equal to

$$V_{OUT} = -64.264\,V_{IN} \pm 11.1mV \qquad (12)$$

Gain error is approximately 0.41%. This result is for 25°C, and it should be compared with the result in Equation 10. Both gain and dc offset errors have been at least halved.

Parameter	AD7534KN $T_A = +25°C$	AD7534KN $T_A = +70°C$	AD7534TD $T_A = +125°C$
Resolution, n	14-bits	14-bits	14-bits
Relative Accuracy, x (Integral Linearity)	±1LSB max	±1LSB max	±1LSB max
Gain Error	±4LSBs max	±4LSBs max	±4LSBs max
Output Leakage, I_{LKG}	±5nA max	±10nA max	±20nA max
Input Resistance, R_{IN}	10kΩ max	10kΩ max	10kΩ max

NOTE: $V_{DD} = +15V, V_{SS} = -0.3V$

Table III. AD7534 Specifications at $T_A = +25°C$, $+70°C$ & $+125°C$

For the purpose of calculating the op amp input offset voltage error term, a value of $R_0 = 15\,R_{FB}$ was used in A7. Table IVb shows the individual components of the dc offset error term. The analysis is repeated at +70°C and +125°C, and these results are also included in Table IVb. Comparing the results of Table IVa with Table IVb the effectiveness of the low leakage scheme on the AD7534 is immediately apparent – dc offset errors at +125°C are an

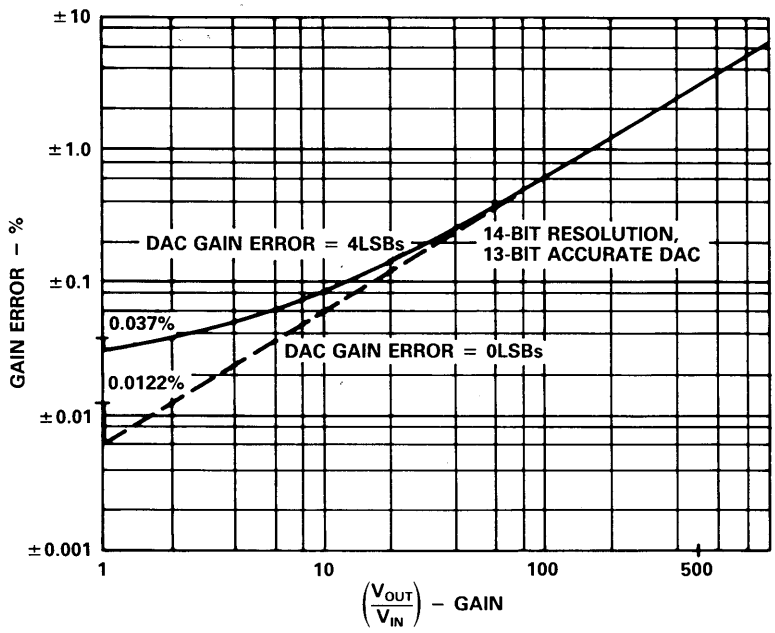

Figure 5. Theoretical Worst Case Gain Errors for AD7534-Based System with and without DAC Gain Error

order of magnitude less with the AD7534. The effectiveness of the low-leakage scheme is further demonstrated by the fact that, for identical gain settings, the equivalent input error voltage for the AD7534 at +125°C is approximately the same as the equivalent input error voltage for the AD7545 at +25°C.

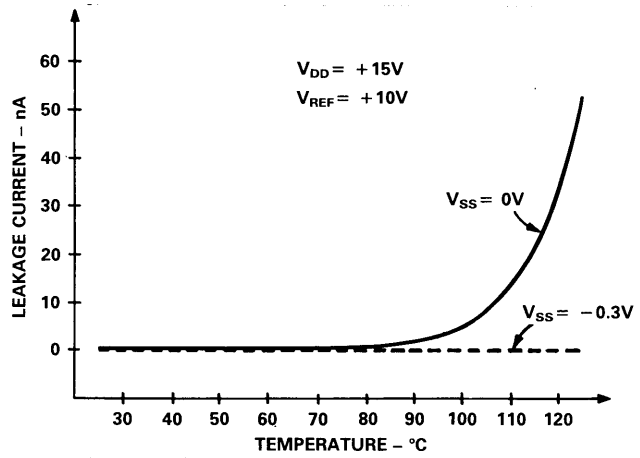

Figure 6. Graph of Typical Leakage Current vs. Temperature

NOISE GAIN

A fundamental requirement of any PGA circuit is that it be monotonic, i.e. if the DAC digital code is changed to increase the gain, then the circuit gain does in fact increase or, at the very least, the circuit gain does not decrease. If the linearity of the DAC is concomitant with the resolution, i.e. 12-bit resolution DAC with 12-bit accuracy, then the DAC is inherently monotonic, and ideally all possible input codes are usable for gain setting. However, if the linearity is less than the resolution, so to speak, i.e. 11-bit accurate but 12-bit resolution DAC, then adjoining codes may overlap causing nonmonotonic operation. In the case of the 11-bit accurate, 12-bit resolution DAC every second code should be avoided, i.e. adjacent codes should not be used. If the DAC specification is more extreme, i.e. 10-bit accurate but still 12-bit resolution, only every fourth code should be used. Thus the number of programmable (and guaranteed monotonic) gain settings is now one quarter of the total number of steps.

The AD7534KN is a 14-bit resolution DAC with 13-bit relative accuracy. Additionally, it is guaranteed monotonic to 14-bits over temperature. This means that ideally all 16, 384 codes are usable for gain setting. However, there is another error source which must be taken into account. The contribution of the input offset voltage, V_{OS}, to the dc offset errors (via the circuits noise gain) has already been mentioned. This noise gain results in a dc term being added to or subtracted from the op amp output. The greatest likelihood of the system becoming nonmonotonic occurs when the DAC input code changes from one code setting to the next adjacent code setting. Adjacent code transitions which are the most critical are those which change the DAC output impedance, R_O, from a low value to a higher value. However, even at the most critical code transition, a nonmonotonic step can still be avoided if the analog input signal voltage, V_{IN}, is sufficiently large with respect to the op amp input offset voltage, V_{OS}. Analysis of the AD7534 over the X1 – X64 gain range in integer steps shows that the worst case code transition is the last code transition. The output impedance R_O changes from $R_O = 6.7\ R_{FB}$ at X63 gain setting ($N = 260_{10}$) to $R_O = 15\ R_{FB}$ at X64 gain setting ($N = 256_{10}$). Simultaneously solving expression A7 at this worst case code transition yields a minimum value for V_{IN} which is the threshold value for possible nonmonotonic operation. This value is 6 V_{OS}. Input signal levels greater than this value will avoid any nonmonotonic transitions occurring. For integer gains which are not integer powers of 2 e.g. X3, X5, X6 etc., the nearest 14-bit code was chosen in each case. Table A5 in Appendix 3 lists both the digital input code used and the resulting $\left(1 + \frac{R_{FB}}{R_O}\right)$ ratio for each integer gain setting in the X1 – X64 gain range.

In some applications, such as closed-loop servo systems, the requirement is for very fine gain adjustment rather than integer gain increments. As Figure 2 suggests, half of the total number of codes, or 2^{n-1}, cover the gain range from X1 to X2. For the AD7534 this means that 8192 codes are available for gain setting between X1 and X2, allowing extremely fine gain adjustment. Between the X1 and X64 gain settings there are just over 16,000 possible gain settings. However, in return for having so many gain settings available, there is a price to be paid in terms of the minimum V_{IN}/V_{OS} ratio required for monotonicity. Computer analysis shows that in order to avoid a nonmonotonic transition between any adjacent code pair over the full X1

		DC ERRORS			
TEMPERATURE	GAIN ERROR	I_{LKG}	$I_B(-)$	V_{OS}	TOTAL
T_A = +25°C	0.91%	16.1mV	6.5mV	6.5mV	29.1mV
T_A = +70°C	0.91%	80.1mV	9mV	11.7mV	100.8mV
T_A = +125°C	0.92%	322.5mV	9.7mV	17.4mV	349.6mV

Table IVa. Error Analysis Over Temperature with AD7545, Gain = 64

		DC ERRORS			
TEMPERATURE	GAIN ERROR	I_{LKG}	$I_B(-)$	V_{OS}	TOTAL
T_A = +25°C	0.41%	3.2mV	2.6mV	5.3mV	11.1mV
T_A = +70°C	0.41%	6.4mV	3.6mV	9.5mV	19.5mV
T_A = +125°C	0.41%	12.8mV	3.8mV	14.1mV	30.7mV

Table IVb. Error Analysis Over Temperature with AD7534, Gain = 64

– X64 code table, the minimum analog input voltage, V_{IN}, should be greater than 1350 V_{OS}. At first glance this is a surprisingly large ratio but, on reflection, should be expected. When adjacent 14-bit codes are used, the percentage increase in gain is a tiny fraction of a percentage point. This is especially true at the lower gain settings. However, the percentage change in noise gain for the same code transition can be orders of magnitude greater. For instance, for the code transition $16{,}379_{10}$ to $16{,}378_{10}$, the signal gain increases by 0.006% whereas the noise gain changes by 0.775%. The ratio of V_{IN} to V_{OS} required to ensure monotonicity at this code transition is 400.

Noise gain is usually assumed to contribute a dc error term only; acting only on the op amps input offset voltage, V_{OS}. However, expression A1 in Appendix 2 shows that the noise gain also contributes to the gain error of the system. The very high open-loop gain of the AD OP-07, however, ensures that any contribution is at a negligible level.

TEST RESULTS

DC measurements were taken on a number of AD7534KN/AD OP-07E combinations at +25°C and a representative result is indicated in Figure 7. The "starred" points indicate the measured errors at the selected gain settings between X1 and X256. At each gain setting the dc input signal level was adjusted to provide a 5V output signal level. As a comparison, the theoretical worst-case error curves from Figure 5 are reproduced again in Figure 7. No adjustments were made to either DAC gain error or op amp input offset voltage. Since the measurements taken were dc, the representative error curve in Figure 7 includes the offset errors at +25°C. However, these were measured at approximately 40μV and were considered negligible in comparison to the input test signal level.

With a gain of 64 the 3dB bandwidth of the system is typically 7kHz. In order to avoid gain errors due to op amp roll-off the signal bandwidth should be restricted to an appropriate limit. For instance, restricting the signal bandwidth to below 100Hz (1/70th of 3dB frequency) ensures that additional gain errors due to roll-off are below 0.01% (a simple, single pole roll-off is assumed). Wider bandwidth op amps than the AD OP-07 can be used in order to increase the signal bandwidth but possibly at the expense of increasing one or more of the error sources. At a gain of X1 the 3dB bandwidth is approximately 500kHz.

The output voltage settling time will be limited by the slew rate of the AD OP-07. Output voltage settling time was measured for a step input change at two fixed gain settings (X1, X64). The output response is shown in the oscilloscope photographs of Figure 8a and 8b.

For Figure 8a (X1 Gain) the input step size is ±200mV, and for Figure 8b (X64 Gain) it is ±154mV. The input signal rise time in either case from the 10% to 90% points was 1μs. Settling time to within ±0.01% for the X1 case is less than 30μs, whereas settling time for the X64 case is less than 300μs. Output voltage settling time was also measured for a change in gain settings (i.e. DAC code) with a steady input signal. The oscilloscope photograph of Figure 8c shows the output response when changing from a X1 setting to a X64 setting. The input signal level was a constant −154mV. The output voltage settling time to within ±0.01% is approximately 300μs going from X1 to X64, while going from X64 to X1 it is approximately 60μs. The dynamic response of the AD7545LN & AD OP-07 PGA combination was similarly measured and found to be indistinguishable from the above.

When ac signals are to be amplified the nonlinearity or distortion of the system becomes important. CMOS DACs are manufactured with high quality, thin-film resistors having very low noise and very small voltage coefficient. In addition, very little of the input signal voltage is developed across the signal-steering switches of the ladder network; hence most of the distortion in the output signal

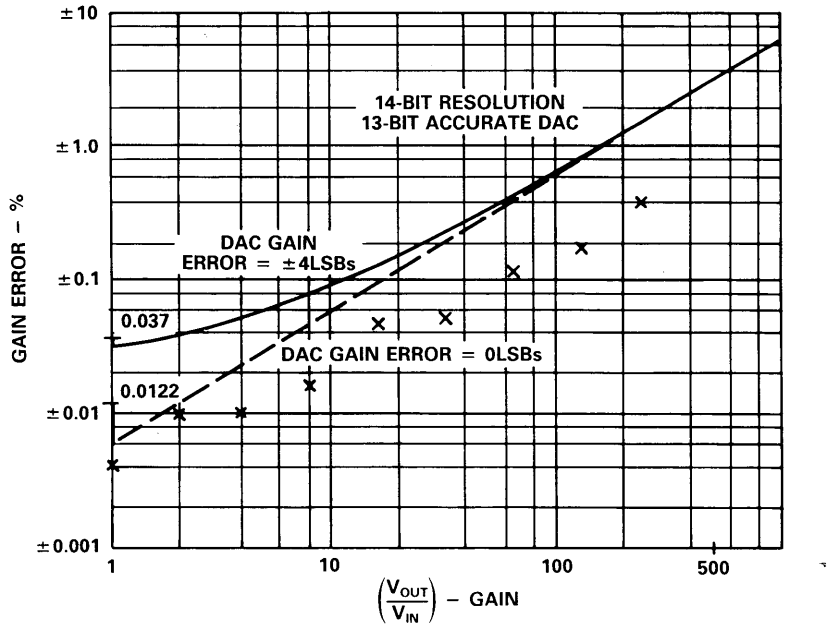

Figure 7. Measured vs. Theoretical Worst Case Gain Errors for AD7534-Based System

is due to the op amp. Table V compares the performance of the 12-bit AD7545LN with the 14-bit AD7534KN in terms of harmonic distortion. In both cases, at any particular gain setting, the input signal level was adjusted to provide a 6V rms output signal level. The test frequency was 200Hz, and distortion levels were measured using a Hewlett Packard HP339A Distortion Measurement Set with it's 3rd order, 30kHz low pass filter function switched into the signal path. Results for the two PGA systems are very similar. Table VI compares the two systems in terms of voltage noise performance over a bandwidth from 22Hz to 22kHz. To help the comparison, the same low noise AD OP-27 op amp was used in both circuits. The superior performance of the AD7534-based system is due to the lower value of DAC ladder resistance compared with the AD7545.

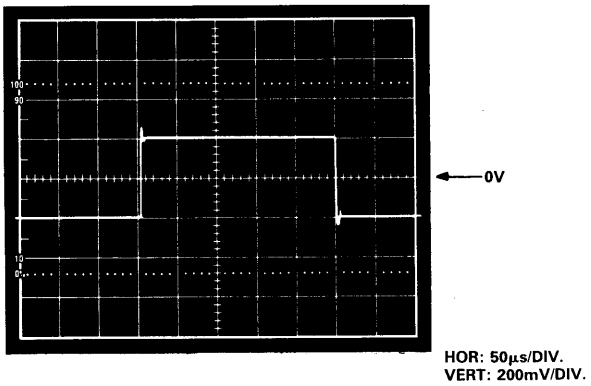

Figure 8a. Gain of 1. Output Response to ±200mV Step Input AD7534 System

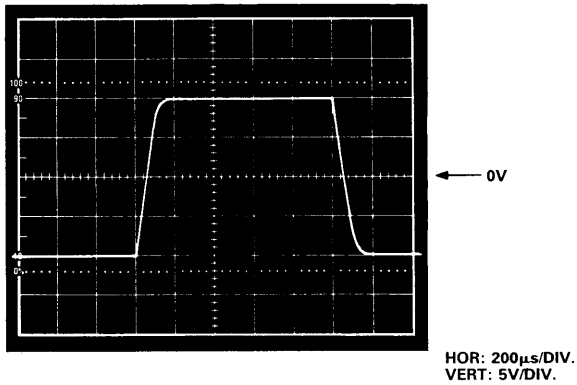

Figure 8b. Gain of 64. Output Response to ±154mV Step Input, AD7534 System

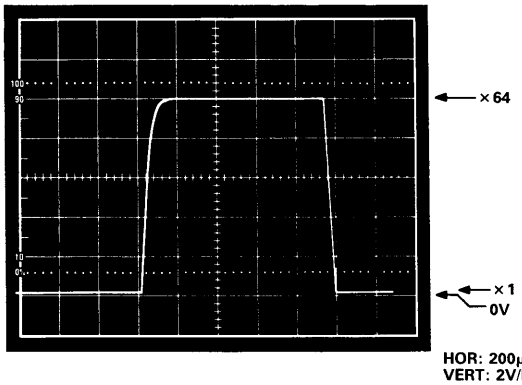

Figure 8c. Output Response when Gain Switching between ×1 and ×64. Constant Input Signal of −154mV. AD7534 System

GAIN	AD7545LN & AD OP-27	AD7534KN & AD OP-27
X 1	5.5µV	4.5µV
X 2	9µV	7µV
X 4	18µV	12µV
X 8	35µV	23µV
X 16	72µV	45µV
X 32	145µV	89µV
X 64	285µV	175µV

Table VI. Output Voltage Noise vs. Gain Settings. Readings are rms, 22Hz to 22kHz.

GAIN	AD7545LN & AD OP-07	AD7534KN & AD OP-07
X 1	<−90dB	<−90dB
X 2	<−90dB	<−90dB
X 4	<−90dB	<−90dB
X 8	−89dB	−88dB
X 16	−86dB	−86dB
X 32	−82dB	−83dB
X 64	−76dB	−79dB

Table V. Total Harmonic Distortion Levels vs. Gain Settings for a Constant 6V rms Output Signal

REFERENCES

1. Application Note; "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton. Available from Analog Devices, Publication No. E630c-5-3/86.
2. Handbook; "CMOS DAC Application Guide." Available from Analog Devices, Publication No. G872a-15-4/86.
3. Clayton, G.B., "Operational Amplifiers, Second Edition," Butterworths (1979).
4. Transaction Brief; "Expression for the Output Resistance of a Switched R-2R Ladder Network" by E. David Erb and Gregory M. Wierzba. IEEE Trans. Circuits & Systems, Vol CAS-30, No 3, March 1983, p167-169.

APPENDIX 1

		SYSTEM GAIN ERROR	
GAIN	CODE N	RELATIVE ACCURACY X = +0.5	RELATIVE ACCURACY X = −0.5
1	4095	+0.0122%	+0.0366%
2	2048	−0.0244%	+0.0244%
4	1024	−0.0488%	+0.0489%
8	512	−0.0976%	+0.0978%
16	256	−0.195 %	+0.1957%
32	128	−0.389 %	+0.3922%
64	64	−0.775 %	+0.7874%
128	32	−1.539 %	+1.587 %
256	16	−3.03 %	+3.226 %
512	8	−5.88 %	+6.666 %

$$\text{Error}(\%) = -\left(\frac{X}{N+X}\right)\cdot 100\% \qquad (9a)$$

Table A1. Computed Values for Equation 9a for 12-Bit Resolution (n = 12), 12-Bit Accurate (X = ±0.5LSBs) DAC with Zero DAC Gain Error. The Unity Gain Values Include an Additional +0.0244% Error Term as Discussed in the Text.

		SYSTEM GAIN ERROR	
GAIN	CODE N	RELATIVE ACCURACY X = +1	RELATIVE ACCURACY X = −1
1	16383	0%	+0.0122%
2	8192	−0.0122%	+0.0122%
4	4096	−0.0244%	+0.0244%
8	2048	−0.0488%	+0.0488%
16	1024	−0.0976%	+0.0978%
32	512	−0.195 %	+0.1957%
64	256	−0.389 %	+0.3922%
128	128	−0.775 %	+0.7874%
256	64	−1.539 %	+1.587 %
512	32	−3.03 %	+3.226 %

$$\text{Error}(\%) = -\left(\frac{X}{N+X}\right)\cdot 100\% \qquad (9a)$$

Table A3. Computed Values for Equation 9a for 14-Bit Resolution (n = 14), 13-Bit Accurate (X = ±1LSBs) DAC with Zero DAC Gain Error. The Unity Gain Values Include an Additional +0.0061% Error Term as Discussed in the Text.

		SYSTEM GAIN ERRORS			
		DAC GAIN ERROR, Δ = +0.0012		DAC GAIN ERROR, Δ = −0.0012	
GAIN	CODE N	REL. ACCURACY X = +0.5	REL. ACCURACY X = −0.5	REL. ACCURACY X = + 0.5	REL. ACCURACY X = −0.5
1	4095	−0.109%	−0.085%	+0.134%	+0.159%
2	2048	−0.146%	−0.098%	+0.096%	+0.145%
4	1024	−0.171%	−0.073%	+0.071%	+0.169%
8	512	−0.219%	−0.024%	+0.022%	+0.218%
16	256	−0.317%	+0.074%	− 0.075%	+0.318%
32	128	−0.511%	+0.270%	−0.270%	+0.513%
64	64	−0.896%	+0.665%	− 0.656%	+0.908%
128	32	−1.658%	+1.464%	−1.420%	+1.709%
256	16	−3.148%	+3.1 %	−2.914%	+3.349%
512	8	−5.977%	+6.537%	− 5.769%	+6.795%

$$\text{Error}(\%) = -\left[\left(\frac{\Delta}{1+\Delta}\right)+\left(\frac{1}{1+\Delta}\right)\left(\frac{X}{N+X}\right)\right]\cdot 100\% \qquad (8)$$

Table A2. Computed Values for Equation 8 for 12-Bit Resolution (n = 12), 12-Bit Accurate (X = ±0.5LSBs) DAC with DAC Gain Error of ±5LSBs (Δ = ±5/4096). The Unity Gain Values Include an Additional +0.0244% Error Term as Discussed in the Text.

SYSTEM GAIN ERRORS

		DAC GAIN ERROR, Δ = +0.000244		DAC GAIN ERROR, Δ = −0.000244	
GAIN	CODE N	REL. ACCURACY X = +1.0	REL. ACCURACY X = −1.0	REL. ACCURACY X = +1.0	REL. ACCURACY X = −1.0
1	16383	−0.025%	−0.012%	+0.024%	+0.037%
2	8192	−0.037%	−0.012%	+0.012%	+0.037%
4	4096	−0.049%	0 %	0 %	+0.049%
8	2048	−0.073%	−0.024%	−0.024%	+0.073%
16	1024	−0.122%	+0.073%	− 0.073%	+0.122%
32	512	−0.219%	+0.171%	−0.171%	+0.22 %
64	256	−0.413%	+0.368%	− 0.365%	+0.417%
128	128	−0.799%	+0.763%	−0.751%	+0.812%
256	64	−1.562%	+1.563%	−1.514%	+1.612%
512	32	−3.054%	+3.2 %	− 3.007%	+3.251%

$$\text{Error (\%)} = -\left[\left(\frac{\Delta}{1+\Delta}\right)+\left(\frac{1}{1+\Delta}\right)\left(\frac{X}{N+X}\right)\right]\cdot 100\% \qquad (8)$$

Table A4. Computed Values for Equation 8 for 14-Bit Resolution (n = 14), 13-Bit Accurate (X = ±1LSBs) DAC with Gain Error of ±4LSBs (Δ = ±4/16,384). The Unity Gain Values Include an Additional +0.0061% Error Term as Discussed in the Text.

APPENDIX 2

The DAC-related error sources, in addition to linearity error, are code-dependent output resistance, leakage current and gain error. Op amp-related error sources are input offset voltage, input bias current and finite open loop gain. Putting all the error sources together results in a complete but somewhat unwieldly expression for the output voltage. For a more complete treatment of the error sources the reader is referred to References 2, 3. If the op amp of Figure 1b has an open loop gain of A_{OL}, then the output voltage of the circuit is

$$V_{OUT} = -V_{IN}\cdot\frac{R_{EQ}}{R_{FB}}\cdot\left\{\frac{1}{1+\left(\frac{1}{A_{OL}}\right)\left(1+\frac{R_{EQ}}{R_{FB}\parallel R_0}\right)}\right\} \qquad (A1)$$

The $\left(1+\frac{R_{EQ}}{(R_{FB}\parallel R_0)}\right)$ term in this expression is called the noise gain G_N or closed loop gain $\frac{1}{\beta}$ of the circuit. R_O is the code-dependent output resistance of the DAC which appears between the op amp summing junction and AGND.

The output voltage due to the DAC leakage current I_{LKG}, op amp input offset voltage V_{OS} and input bias current $I_B(-)$ is conveniently found by combining these separate error sources into a single input offset error source E_{OS}. The output voltage due to this error source is thus

$$\left(\frac{1}{\beta}\right)\cdot E_{OS} = G_N\cdot E_{OS}$$

$$\text{Where } E_{OS} = \pm V_{OS} \pm I_{LKG}\cdot R \pm I_B(-)\cdot R \qquad (A2)$$

R is the effective source impedance seen by the inverting input to AGND, i.e.,

$$R = R_{FB}\parallel R_O\parallel R_{EQ}$$

or

$$R = \frac{R_{EQ}}{G_N} \qquad (A3)$$

The output voltage due to E_{OS} is thus

$$\pm V_{OS}\cdot G_N \pm I_{LKG}\cdot R_{EQ} \pm I_B(-)\cdot R_{EQ}$$

or

$$\pm V_{OS}\cdot G_N + (I_{LKG} + I_B(-))\cdot R_{EQ} \qquad (A4)$$

The noise gain G_N (or closed loop gain $\frac{1}{\beta}$) is a function of the DAC output rsistance. This resistance is quite a complex function of the digital input code, roughly increasing from a minimum value to a maximum value as the DAC code changes from all ones to all zeros respectively. [Reference 4].

The DAC output resistance is also influenced by the type of ladder network used in the DAC design. The two DACs in comparison here use two different networks; the AD7545 is a straight R-2R ladder design while the AD7534 uses a segmented design. This means that the noise gain term will be different for both DACs.

When all of these components are summed together the output voltage expression becomes

$$V_{OUT} = -V_{IN}\cdot\frac{R_{EQ}}{R_{FB}}\left\{\frac{1}{1+\left(\frac{1}{A_{OL}}\right)\left(1+\frac{R_{EQ}(R_{FB}+R_0)}{R_{FB}\cdot R_0}\right)}\right\}$$

$$\pm (I_{LKG} + I_B(-))\cdot R_{EQ}$$

$$\pm V_{OS}\cdot\left(1+\frac{R_{EQ}(R_{FB}+R_0)}{R_{FB}\cdot R_0}\right) \qquad (A5)$$

When R_{EQ} is replaced by $\frac{2^n R_{IN}}{N+x}$ and the DAC gain error is taken into account by letting

$$\frac{R_{FB}}{R_{IN}} = (1+\Delta)$$

$$\text{where } \Delta = \frac{R_{FB}-R_{IN}}{R_{IN}} \qquad (A6)$$

the output expression becomes

$$V_{OUT} = -V_{IN} \cdot \frac{2^n}{(N+x)(1+\Delta)} \left\{ \frac{1}{1+\left(\frac{1}{A_{OL}}\right)\left\{1+\left(\frac{2^n}{(N+x)(1+\Delta)}\right)\left(1+\frac{R_{FB}}{R_0}\right)\right\}} \right\}$$

$$\pm (I_{LKG} + I_B(-)) \cdot \frac{2^n R_{IN}}{N+x}$$

$$\pm V_{OS}\left\{1+\left(\frac{2^n}{(N+x)(1+\Delta)}\right)\left(1+\frac{R_{FB}}{R_0}\right)\right\} \qquad \text{(A7)}$$

Expression A7 can be simplified since the effect of DAC linearity and DAC gain error on the error sources is almost negligible. Similarly, for the system gains under consideration, the gain error factor in expression A1 can reasonably be assumed to be unity, i.e.,

$$\frac{1}{1+\left(\frac{1}{A_{OL}}\right)G_N} \approx 1 \qquad \text{(A8)}$$

When these assumptions are made, expression A7 simplifies to

$$V_{OUT} = -V_{IN}\frac{2^n}{(N+X)(1+\Delta)}$$

$$\pm \{I_{LKG} + IB(-)\} \cdot R_{IN} \cdot (\text{SYSTEM GAIN})$$

$$\pm V_{OS}\left\{1+(\text{SYSTEM GAIN})\left(1+\frac{R_{FB}}{R_O}\right)\right\} \qquad \text{(A9)}$$

As the system gain is increased, so too are the dc offset errors due to leakage currents and input offset voltage.

APPENDIX 3

SYSTEM GAIN	$CODE_{10}$	$(1+R_{FB}/R_O)$	SYSTEM GAIN	$CODE_{10}$	$(1+R_{FB}/R_O)$	SYSTEM GAIN	$CODE_{10}$	$(1+R_{FB}/R_O)$
1	16383	1.08	24	683	1.31	47	349	1.27
2	8192	1.00	25	655	1.25	48	341	1.30
3	5461	1.31	26	630	1.25	49	334	1.25
4	4096	1.00	27	607	1.24	50	328	1.20
5	3277	1.28	28	585	1.27	51	321	1.21
6	2731	1.31	29	565	1.28	52	315	1.26
7	2341	1.21	30	546	1.21	53	309	1.28
8	2048	1.00	31	529	1.14	54	303	1.25
9	1820	1.20	32	512	1.06	55	298	1.26
10	1638	1.25	33	496	1.13	56	293	1.27
11	1489	1.25	34	482	1.20	57	287	1.22
12	1365	1.31	35	468	1.22	58	282	1.24
13	1260	1.22	36	455	1.25	59	278	1.24
14	1170	1.24	37	443	1.26	60	273	1.22
15	1092	1.18	38	431	1.26	61	269	1.24
16	1024	1.03	39	420	1.22	62	264	1.15
17	964	1.18	40	410	1.25	63	260	1.15
18	910	1.23	41	400	1.17	64	256	1.07
19	862	1.23	42	390	1.22			
20	819	1.28	43	381	1.23			
21	780	1.20	44	372	1.22			
22	745	1.27	45	364	1.23			
23	712	1.21	46	356	1.22			

Table A5. Digital Input Codes and Resulting $(1+R_{FB}/R_O)$ Ratio vs. System Gain for the AD7534