ANALOG DEVICES

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APPLICATION NOTE

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A WiMax Double Downconversion IF Sampling Receiver Design

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INTRODUCTION

This application note describes an intermediate frequency (IF) sampling receiver intended for use in the wireless communication services (WCS) band from 2.3 GHz to 2.36 GHz and the unlicensed ISM band from 2.4 GHz to 2.48 GHz. The receiver is designed for broadband Orthogonal Frequency Division Multiplexing (OFDM) systems, as described according to IEEE 802.16 standards documentation. The design approach and implementation procedures are presented to allow designers to easily modify the receiver chain to address other bands such as Wireless Broadband (WiBro) and other cellular standards such as TDS-CDMA. The presented design is capable of addressing channel bandwidths as wide as 10 MHz using the depicted surface acoustic wave (SAW) filter; however, larger bandwidths can be addressed using wider bandwidth channel-select filters and increased sampling rates.

BACKGROUND

OFDM is the modulation scheme used in the next emerging WiMax standard. OFDM utilizes multiple subcarriers of various IQ modulations to achieve a high aggregate data rate that has inherent immunity to multipath propagation. The baseband information is spread among subcarriers so that little information is lost if multiple propagation paths result in destructive interference and heavily attenuate a portion of the transmitted spectrum. The variability in the subcarrier modulation schemes allows for an adaptive signaling approach that propagates lower data rates at the greatest distances, while the highest data rates can be utilized when the received signal-to-noise ratio (SNR) is high.

The variety of subcarrier modulation schemes and coding results in different SNR requirements at the receiver. The reference sensitivity of a WiMax receiver is defined in the IEEE Std. 802.16-2004 to be −91 dBm for a 1.5 MHz channel using ½ coding rate QPSK, and −65 dBm for a 20 MHz channel using ¾ coding rate 64-QAM. This results in a receiver NF requirement of 7 dB with 5 dB of implementation margin.

The 802.16 standard defines a maximum input power level of −30 dBm for successful detection, with a maximum tolerated power level of 0 dBm. While the base station or subscriber station is not expected to decode a 0 dBm input level successfully, the equipment must be able to withstand the large 0 dBm input without damage.

The 802.16 standard describes an adjacent channel rejection requirement for the receiver. The following adjacent and nonadjacent channel interferer to desired channel power ratios must be achieved while maintaining a 10^{-6} bit error rate (BER) while the desired signal is no more than 3 dB above the specified reference sensitivity.

Table 1. Adjacent and Nonadjacent Channel Rejection Requirements as Described in the 802.16-2004 Standard

Modulation/Coding	Adjacent Channel Rejection (dB)	Nonadjacent Channel Rejection (dB)
16-QAM-¾	−11	−30
64-QAM-¾	−4	−23

ARCHITECTURE

Figure 1 depicts a classic double downconversion IF sampling receiver. IF sampling architectures are quite appropriate when dealing with large signal bandwidths as employed in WiMax, or even multicarrier systems. By using multiple down conversions, it is possible to employ several channel select filters that help to improve the selectivity of the receiver and improve immunity to blocking signals that would otherwise degrade receiver sensitivity. The double downconversion also allows the use of a high enough first IF where the image frequency band falls out of the passband of the front-end, band-select RF filter.

The receiver architecture described in this application note is based on a 14-bit ADC. A 12-bit ADC could be used to address the 802.16 receiver requirements, although it is recommended to use a 14-bit ADC for single-down conversion or for multicarrier architectures in order to compensate for the less efficient selectivity and avoid the saturation of the ADC in presence of high interferer levels. In order to design a receiver capable of successfully addressing the multiple data rate options available, it is necessary to select IF center frequencies carefully and ensure that appropriate SAW filter selections are available.

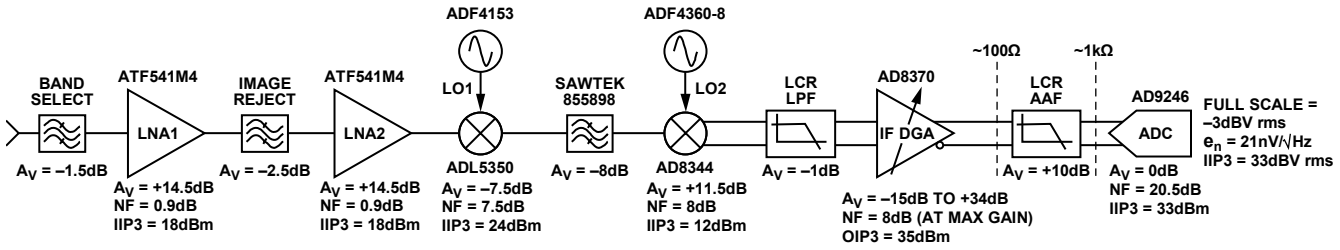

Figure 1. Double Downconversion IF Sampling Receiver Chain

Figure 2 shows the spurious trajectories for a downconverting mixer using low-side LO injection. In order to cover the 2.3 GHz to 2.4 GHz bands while minimizing the number of spurious mixer components that can interfere with the desired signal, inspection of the spurious trajectories indicates that the first IF should be within a range of 210 MHz to 400 MHz. The grey shaded area indicates the fractional bandwidth bounded by f_{RF}/f_{LO} and f_{IF}/f_{LO} for a 374 MHz IF using a low-side LO (LO1 = 1926 MHz to 2026 MHz). It is possible to substitute other IF center frequencies, but caution must be taken to ensure that the spurious responses of the first mixer do not cause in-channel interference. For this design, a first IF of 374 MHz is selected. There are several commercially available SAW filters of various bandwidths from Sawtek, as well as other manufacturers, that address this center frequency.

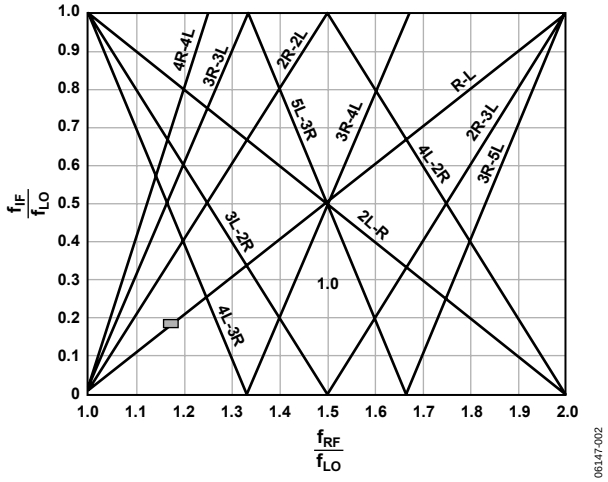

Figure 2. Spurious Trajectories for a Down Converting Mixer Using Low-Side LO Injection (Note that the grey box indicates the fractional bandwidth boundaries for a 374 MHz IF using low-side LO injection for the 2.3 GHz to 2.4 GHz WiBro frequency band.)

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Next it is necessary to consider the final IF. The second down converting mixer has the benefit of a narrower input bandwidth, typically no more than 20 MHz. This allows several possible second IFs to be considered, with ranges from 10 MHz to 70 MHz and higher IF frequency bands centered at 107 MHz and 140 MHz. A 70 MHz IF is selected in order to avoid higher order LO harmonics that can leak back to the antenna receive port and fall in the desired receive band. Additionally, the 70 MHz IF allows for a wide selection of commonplace SAW filters to be applied, or alternatively, practically lumped element LC passive filters.

After establishing the target IF frequencies it is possible to consider the cascaded performance. Table 2 depicts the anticipated dynamic performance of the double downconversion receiver from the output of the band-select filter down to the ADC interface.

Table 2. Anticipated Dynamic Performance of Receiver Signal Chain depicted in Figure 1

Gain (dB)	IIP3 (dBm)	NF (dB)
65.5	−32.8	2.6
58.5	−26	2.7
48.5	−14.5	3.5
37	−7.7	4.6
23.5	−5.6	9.7

IMPLEMENTATION

The first component in the receiver chain is a band-select filter. Several manufacturers, such as Anatech Electronics, Inc., K & L Microwave Inc., and Digital Communications Inc., provide cavity- and ceramic-based filters that address the WCS and unlicensed ISM frequency bands utilized for 2.3 GHz to 2.5 GHz WiMax deployments. The cavity-based filters are capable of low insertion loss of less than 2 dB with up to 60 dB of stop-band rejection at only 25 MHz offset from the center of the pass band. The lower cost ceramic-based filters offer closer to ~50 dB of stop-band rejection at 150 MHz offsets. The choice of band select filter strongly depends on the image rejection performance of the receiver and the expected magnitude of the interfering signals present in the vicinity of the band of operation. For this demonstration, a Digital Communications Inc. 10-section band-pass cavity filter is selected at a center frequency of 2350 MHz.

The first LNA stage follows the front-end, band-select filter. The insertion loss of the filter and the noise figure of the first stage dominate the overall cascaded sensitivity of the receiver. As a result, it is critical to achieve very low noise figure in the first LNA stage. The ATF541M4 GaAs E-mode pHEMT was selected from Agilent Technologies for its low noise and high OIP3. The circuit implementation for the first and second stage LNAs is presented in Figure 3, along with the measured gain and NF performance in Figure 4.

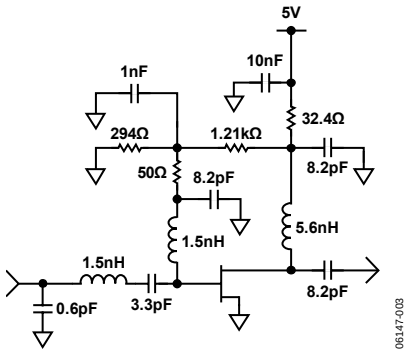

Figure 3. Basic LNA Implementation Schematic

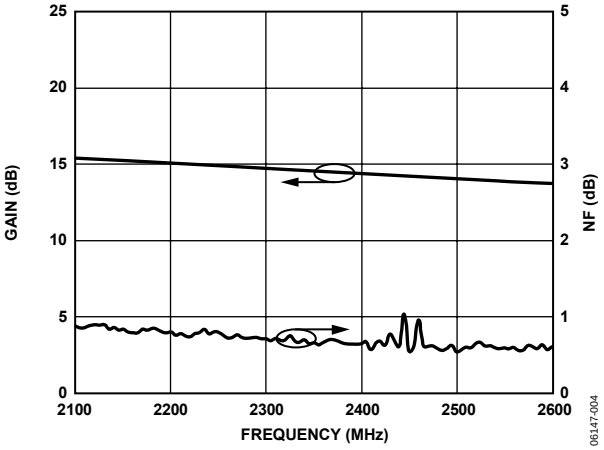

Figure 4. ATF541M4 Gain and NF, Input Return Loss is Measured to be –8 dB with an IIP3 of 18 dBm

In order to help improve the image rejection of the front-end design and to minimize the presented broadband noise to the first mixer, a simple high-pass filter was used between the first and second LNA. The rejection requirement is not very critical considering the first band-select filter provides >60 dB rejection of unwanted signals appearing at the image frequency. Using a 374 MHz IF with low-side LO injection, the fundamental image band is from 1552 MHz to 1652 MHz for a 2.3 GHz to 2.4 GHz input frequency range. A simple 3-pole lumped element filter was designed between the first and second LNA stages. The filter provides better than 20 dB of image band rejection and less than 2.5 dB of insertion loss in the desired pass band. The measured frequency response and circuit implementation is depicted in Figure 5.

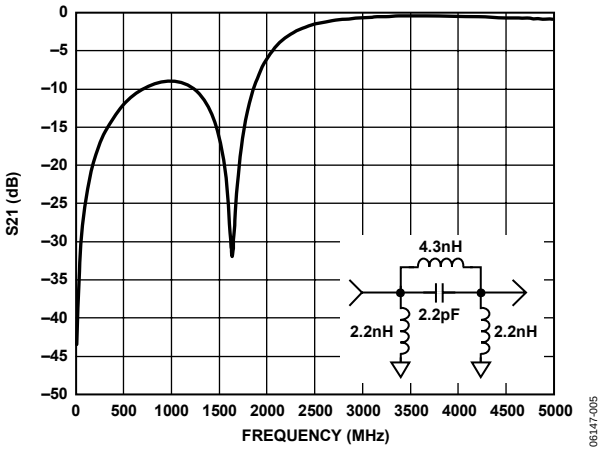

Figure 5. Simple Lumped Element Image Reject Filter Implementation and Measured Response

After the second LNA stage, the signal is downconverted to a fixed high IF of 374 MHz using the ADL5350 mixer. The ADL5350 is a single-ended passive mixer with an onboard LO buffer amplifier. The mixer relies on off-chip filtering networks to isolate the RF and IF ports. The subcircuit depicted in Figure 7 includes the ADL5350 mixer, external filter networks, and an external LO buffer to provide sufficient drive into the LOIN pin.

The additional AD8353 gain stage is needed to amplify the output power of the PLL/VCO synthesizer circuit to ~4 dBm drive level at the LOIN pin. There is additional filtering applied to the LO input to help reduce harmonic content coming from the LO synthesizer. The filter is a simple 3-pole, low-pass filter constructed using lumped element components. Without the filter the second harmonic of the LO would cause some additional high frequency noise power to be downconverted to the desired IF, degrading the reference sensitivity of the receiver. The measured dynamic performance of the ADL5350, including the external LO buffer and filter networks, is presented in Figure 6. The mixer provides better than 24 dBm input IIP3 with ~8 dB conversion loss and single-sideband NF.

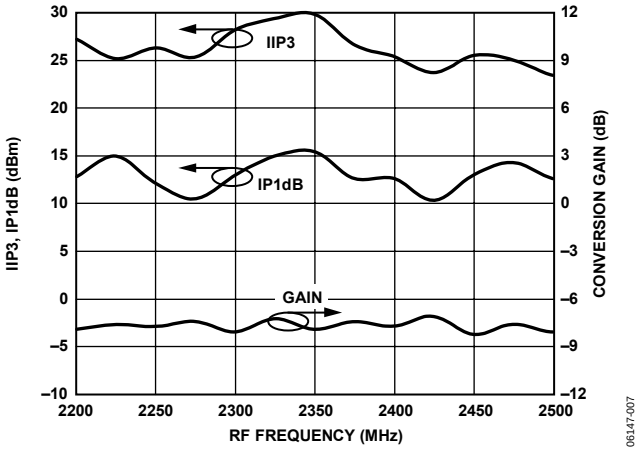

Figure 6. Measured Performance of ADL5350 Mixer

During the downconversion, the phase noise of the PLL is imposed onto each subcarrier of the OFDM modulated signal through convolution. To minimize the impact on the receiver sensitivity level, the first agile PLL for the generation of LO1 is a fractional-N PLL. It is designed with the ADF4153 synthesizer. The closed loop bandwidth is about 30 kHz and the estimated phase jitter is 0.3 degrees.

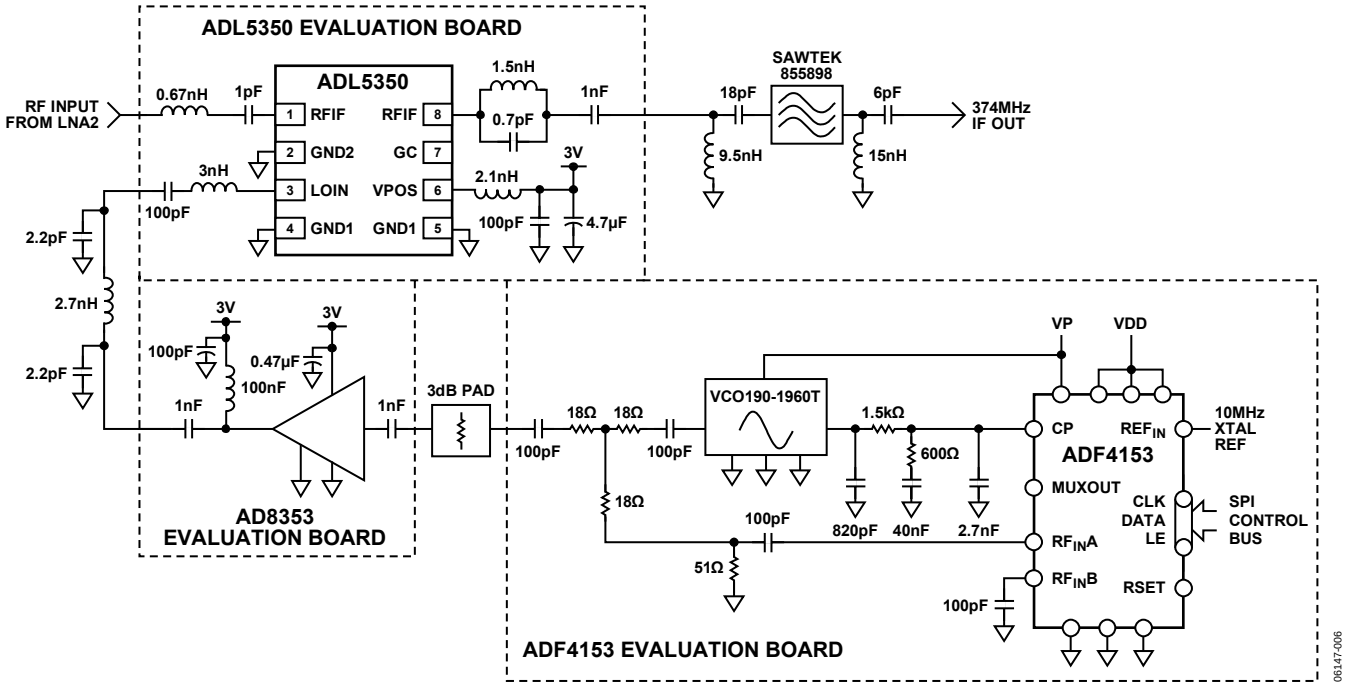

Figure 7. First Mix-Down Stage

The first IF is then passed through a 374 MHz SAW filter for channel selection. The excellent stop-band rejection of the Sawtek 855898 SAW filter allows the receiver to have exceptional selectivity, improving immunity to adjacent interfering signals. The filter is matched to 50 Ω using the external LC component indicated in Figure 7. The filters frequency response characteristic is presented in Figure 8.

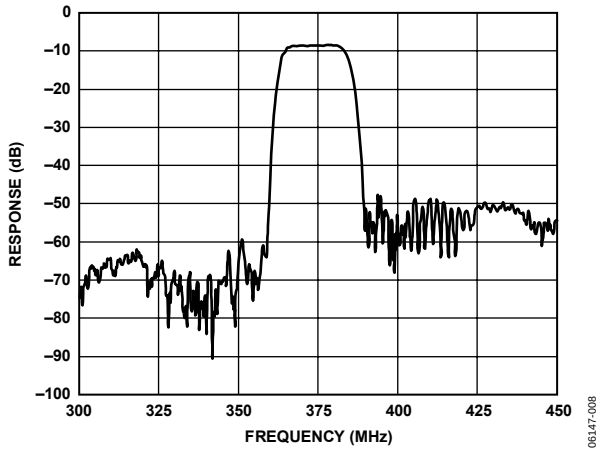

Figure 8. Sawtek 855898 Frequency Response

The first filtered IF signal is then downconverted to the second IF of 70 MHz using the AD8344 active mixer. A low-side LO injection scheme was used to ensure optimal spurious response rejection and to achieve greater gain in the mixer. In general, the AD8344 offers slightly higher conversion gain when using a low-side LO. The 304 MHz LO is provided by the ADF4360-8. This is an integrated PLL + VCO providing good cost and board space savings over discrete solutions. Two external inductors that are the tank inductors of the on-chip VCO set the center frequency. The differential outputs of the ADF4360-8 are combined in a balun. Using a 304 MHz LO the AD8344 offers a conversion gain of ~11 dB, with 12 dBm IIP3 and 8 dB SSB NF. The 70 MHz output is then passed through a fourth order low-pass filter to help reject LO feedthrough and higher frequency mixer spurii.

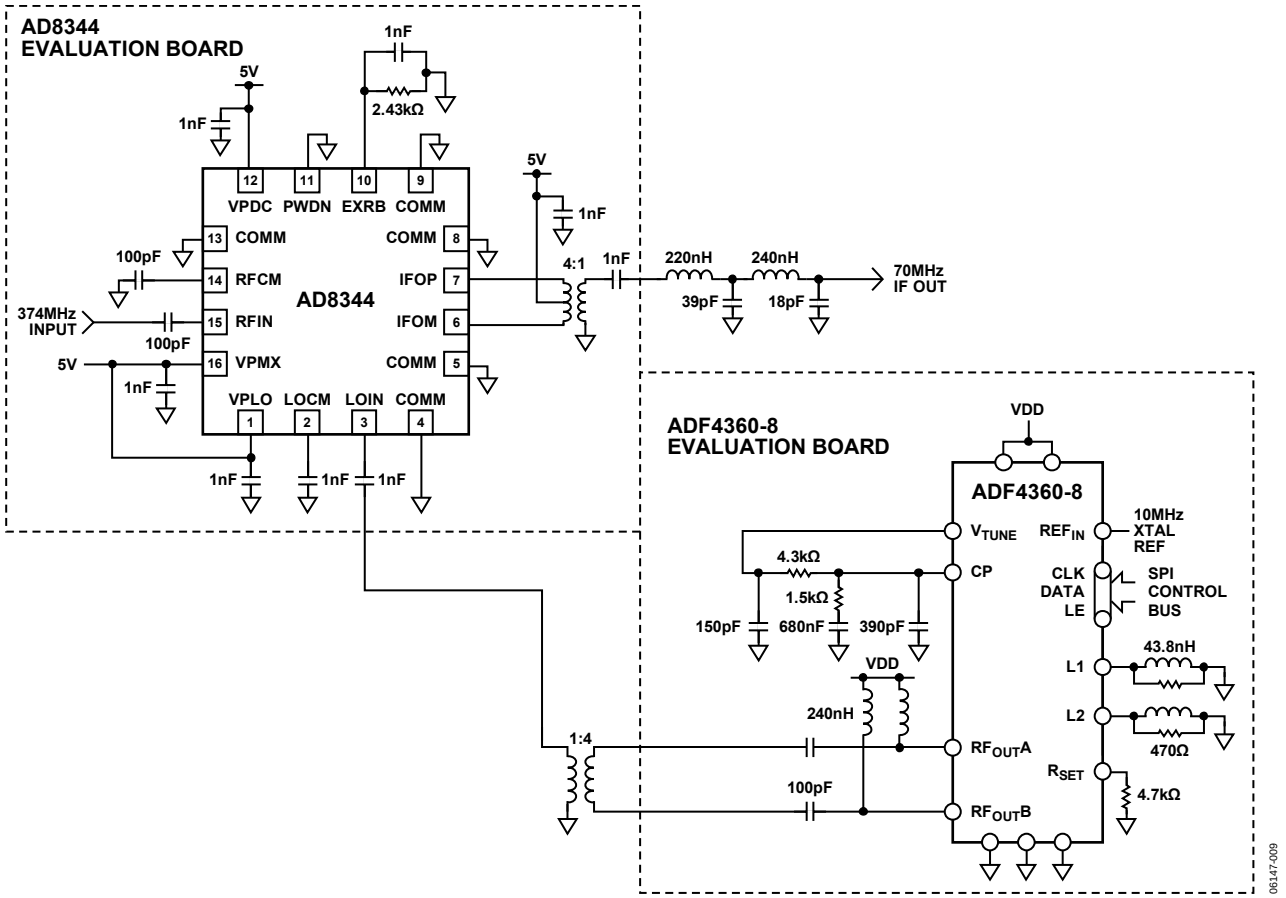

Figure 9. The AD8344 Active Mixer Driven by the ADF4360-8 Through an External 1:4 Impedance Ratio Balun

The final 70 MHz IF signal is then passed through the AD8370 digitally controlled variable gain amplifier before being IF sampled by the AD9246. The AD8370 provides a high output IIP3 and greater than 40 dB gain adjustment range. This allows the overall receiver conversion gain to adjust and tailor the cascaded input dynamic range to accommodate widely varying input signal powers.

The selected ADC provides excellent spurious free dynamic range out to greater than 200 MHz IF frequencies while only consuming ~250 mW. The high analog input bandwidth of 650 MHz allows the AD9246 to be applied to higher IF frequencies. In this demonstration a 70 MHz IF was selected using an 80 MSPS sampling clock, placing the IF in the second Nyquist zone of the ADC.

In order to prevent degradation of the ADC's sensitivity level it was necessary to employ an anti-aliasing filter. The anti-aliasing filter helps to reject higher frequency spurious signals such as LO leakage from degrading the perceived noise floor of the ADC. Additionally the anti-aliasing filter helps to reject wideband noise generated by the driving amplifier stages that would otherwise alias additional noise into the desired Nyquist band. Elliptical low-pass architecture is selected to help provide better rejection of strong spurious components in the higher Nyquist zones. A resonant parallel tank network is formed by the 72 nH bias inductors in combination with the total presented input capacitance. The resonant tank network helps to raise the presented loading impedance at the desired IF frequency. The filter network provides an impedance transformation from 100 Ω to 600 Ω and has the effect of stepping up the voltage by ~8 dB. The step-up transformation needs to be accounted for when analyzing the receiver line-up. For more information regarding the design approach used to yield the driver/ADC interface, please refer to AN-827, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*. The key details of the AD8370 and AD9246 network interface are captured in Figure 11. The simulated filter response is plotted against the measured response through the ADC in Figure 10.

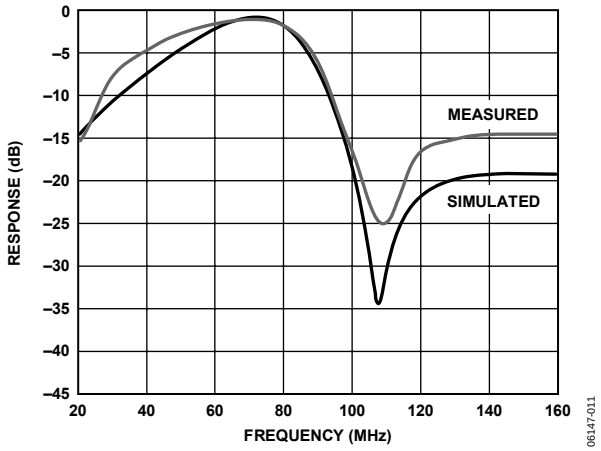

Figure 10. Simulated and Measured Response of the Anti-Aliasing Filter into the AD9246 ADC

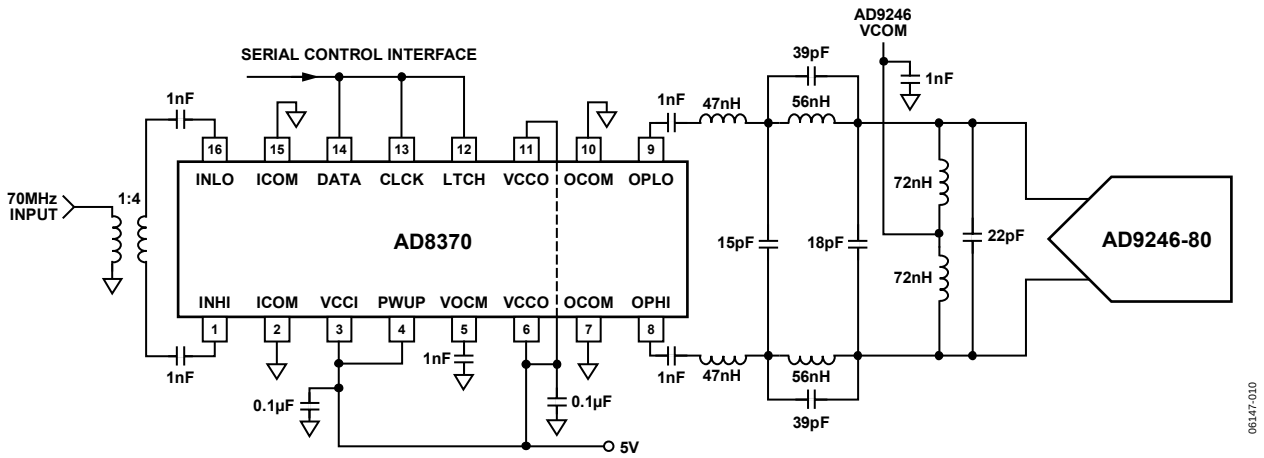

Figure 11. Circuit Interface Between the VGA and ADC

SUMMARY OF COMPLETE RECEIVER PERFORMANCE

While attempting to verify the overall cascaded performance of the full receiver, it is necessary to capture the sampled data from the AD9246 ADC using the Analog Devices high speed ADC FIFO USB evaluation kit. The additional first-in-first-out (FIFO) daughtercard serves as a data buffer to allow capture of long data output strings generated by the ADC at the sampling rate. The FIFO can then transmit the captured data to the PC at a lower data rate that can be supported via a standard USB interface. The ADC evaluation hardware is controlled by Analog Devices ADC Analyzer™ software. The ADC Analyzer allows for time domain and frequency domain analysis. The single-tone and two-tone distortion performance is readily captured using ADC Analyzer, and the results are presented in Figure 12 and Figure 13. Note the discontinuity in Figure 13 around 48 dB of signal gain. This is where the AD8370 VGA transitions from a low gain mode to a high gain mode. The discontinuity does not result in any notable degradation of the BER performance of the full receiver.

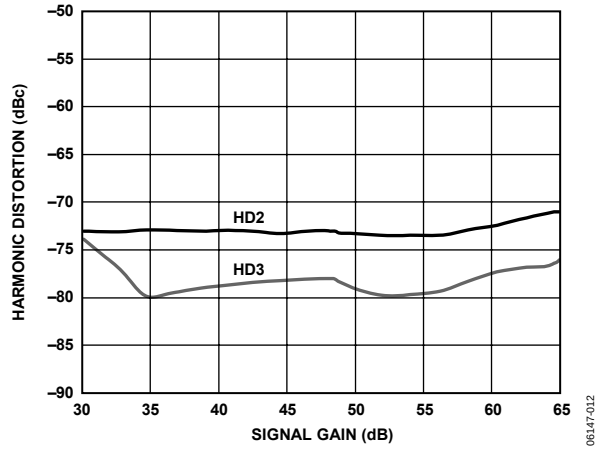

Figure 12. Second and Third Harmonic Distortion for the Full Receiver Cascade Measured at −1 dBFS Input Levels at the AD9246 Input

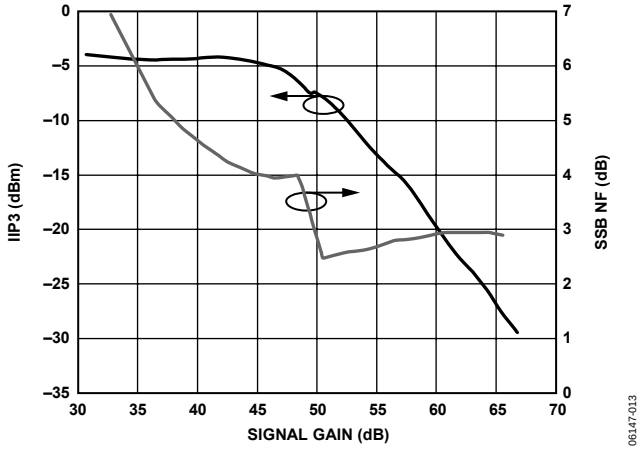

Figure 13. Two-Tone IIP3 and Single-Sideband NF for the Full Receiver Cascade Measured vs. Receiver Conversion Gain

Suitable BER test equipment for an 802.16 OFDM waveform was not available at the time of the evaluation. However, error vector magnitude (EVM) analysis allows for a fair estimate of the receiver performance and available dynamic range. In order to perform EVM analysis on OFDM 802.16 test signals it was necessary to use a FIFO card with an extended memory depth of at least 65 kb. This allows capture of a complete RF burst.

The captured integer vectors range from 0 to 65,536 (2^{16}) with a midscale value of 32,768. Note that the AD9246 is a 14-bit ADC, and that the data output words are 16-bit representation. The captured integer vectors were post-processed in the Advanced Design System (ADS) 2006A from Agilent. The ADS program divides the 16-bit represented IF vector by four to yield a 2^{14} integer representation. The vector is then shifted and scaled in magnitude to yield a zero-mean value waveform with ±1 V peak magnitude. The signal is then demodulated using an ideal IQ demodulator. The IQ vectors are then decimated in time to yield baseband vectors at ¼ the original sampling rate.

The processed IQ vectors are then fed into the 89600 Vector Signal Analyzer software from Agilent to reveal the EVM performance. The measured EVM performance vs. input power is depicted in Figure 14 for a 64-QAM OFDM signal with a 10 MHz modulation bandwidth and ¾ coding rate. The EVM is plotted with and without the ADF4153 and ADF4360 PLLs to provide a comparison of the performance degradation due to phase noise.

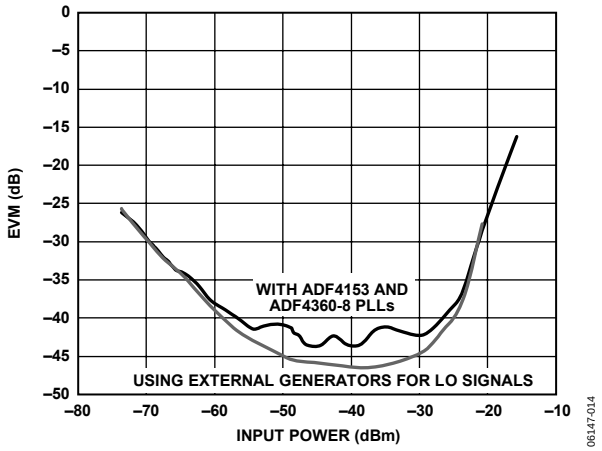

Figure 14. EVM Performance Measured Through the Full Receiver for 64-QAM ¾ Rate Coding, 10 MHz OFDM Signaling

In order to access the selectivity of the receiver, it is necessary to measure the relative response for single-tone inputs swept over a reasonable input frequency range. Figure 15 presents the selectivity of the full receiver in the absence of the front-end band-select filter. The frequency selective nature of the double downconversion receiver provides very high immunity to nearby interferers. With the addition of the front-end band-select filter, greater than 60 dB rejection can be achieved at adjacent RF frequency bands.

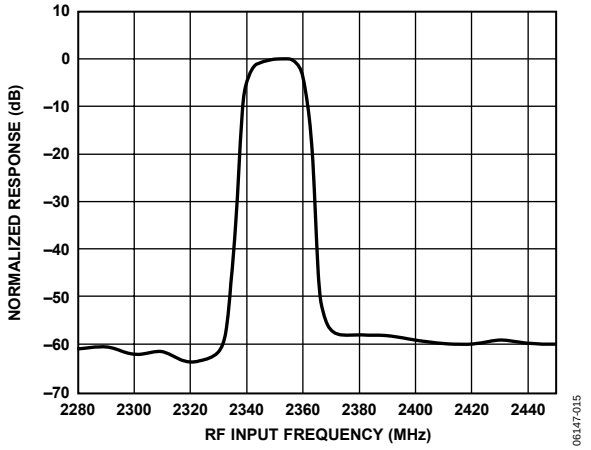

Figure 15. Receiver Selectivity vs. Input Frequency, Local Oscillators Tuned for 2350 MHz Input Signal (f_{LO1} = 1976 MHz, f_{LO2} = 304 MHz)

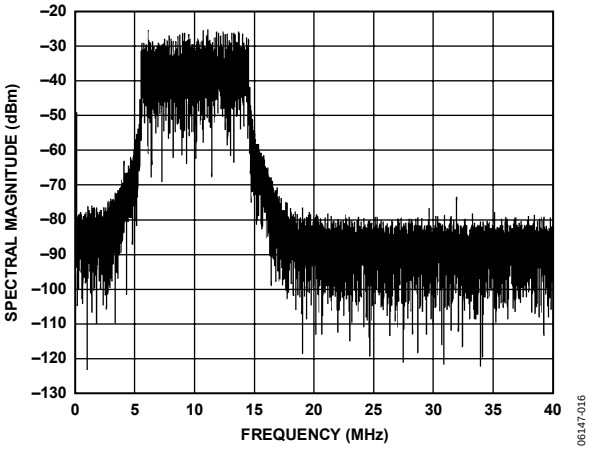

Figure 16. FFT Plot of ADC Spectrum at Mid-Gain for a 64-QAM ¾ Rate Coded, 10 MHz Bandwidth OFDM Input at 2.342 GHz (Note that the signal appears as a 10 MHz IF but is actually a 70 MHz input in the second Nyquist zone of the converter.)

The typical spectral characteristics of the full receiver is depicted in Figure 16. By using the ADC Analyzer software, it is easy to see the instantaneous spectrum and capture time domain data for later signal processing. Whereas the IF is at 70 MHz with an 80 MSPS sampling clock, the signal appears as a 10 MHz signal in the first Nyquist zone. The ADC Analyzer software makes it possible to quickly analyze and debug spurious clock and LO signal components that can otherwise compromise in-band receiver performance. The multiple IF filter stages and LO filters helped to minimize spurious clutter to negligible levels. Note the weak spur at 32 MHz. This is the LO to IF leakage of the first mixer.

A complete summary of the receiver's performance is provided in Table 3. The design provides better than −25 dB EVM performance for input signals greater than −74 dBm, with more than 60 dB image rejection and excellent adjacent and nonadjacent channel rejection.

Table 3. Performance Summary (measured with 64-QAM ¾ rate coding OFDM 10 MHz bandwidth input signal)

Parameter	Measured Performance
Gain Range	30 dB to 67 dB
EVM from −74 dBm to −20 dBm Input Power	<−25 dB
IIP3 at Mid-Gain (Av = 48 dB)	>−8 dBm
NF at Mid-Gain (Av = 48 dB)	<4 dB
Image Rejection	>60 dB
Adjacent Channel Rejection	>58 dB
Power Dissipation (from LNA to ADC, including PLLs)	~2.2 Watts

REFERENCES

Newman, Eric and Reeder, Rob. 2006. "A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs." Application Note AN-827. Analog Devices, Inc. (January)

IEEE Std 802.16-2004. *IEEE Standard for Local and Metropolitan Area Networks - Part 16: Air Interface for Fixed Broadband Wireless Access Systems*. Institute of Electrical and Electronics Engineers, Inc. (June).

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