

Comparators

COMPARATOR BASICS

A comparator is similar to an op amp. It has two inputs, inverting and non-inverting and an output (see Figure 1). But it is specifically designed to compare the voltages between its two inputs. Therefore it operates in a non-linear fashion. The comparator operates open-loop, providing a two-state logic output voltage. These two states represent the sign of the net difference between the two inputs (including the effects of the comparator input offset voltage). Therefore, the comparator's output will be a logic "1" if the input signal on the non-inverting input exceeds the signal on the inverting input (plus the offset voltage, V_{os}) and a logic "0" for the opposite case. A comparator is normally used in applications where some varying signal level is compared to a fixed level (usually a voltage reference). Since it is, in effect, a 1-bit analog-to-digital converter (ADC), the comparator is a basic element in all ADCs. (See [MT-011](#) for details of comparator operation as an ADC building block).

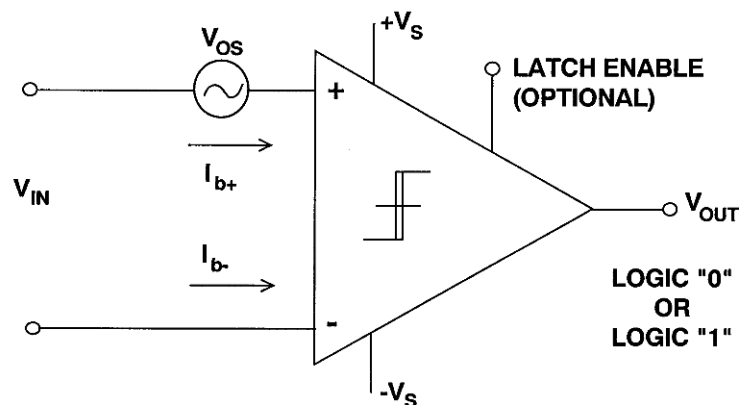


Figure 1: Comparator Symbol

Comparator dc specifications are similar to those of op amps: *input offset voltage, input bias current, offset and drift, common-mode input range, gain, CMR, and PSR*. Standard logic-related dc, timing, and interface specs are associated with the comparator outputs.

The key comparator ac specification is *propagation delay* (see Figure 2): it is the time required for the output to reach the 50% point of a transition, after the differential input signal crosses the offset voltage—when driven by a square wave (typically 100 mV in amplitude) to a prescribed value of input overdrive (usually 5 mV or 10 mV).

The propagation delay in practical comparators decreases somewhat as the input overdrive is increased. This variation in propagation delay as a function of overdrive is called *dispersion* as shown in Figure 3.

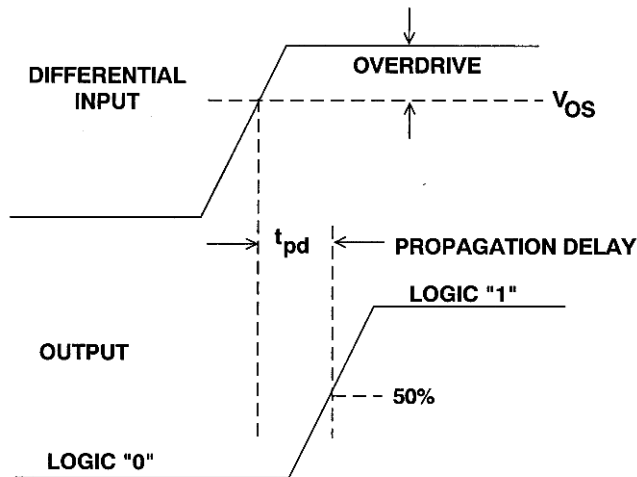


Figure 2: Comparator Propagation Delay

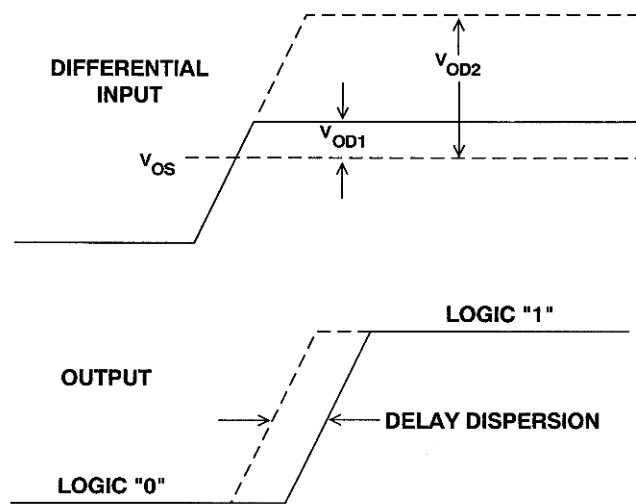


Figure 3: Comparator Delay Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis, which is application of a small amount of positive feedback, to a comparator's transfer function is often useful in a noisy environment, or where it is undesirable for the comparator to toggle continuously between states when the input signal is at or near the switching threshold. This is true when a relatively slowly changing input is compared to a dc level. Noise can cause the output to toggle between the output levels many times. The transfer function for a comparator with hysteresis is shown in Figure 4.

If the input voltage approaches the switching threshold (V_{OS}) from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses $V_{OS} + V_H/2$. The "new" switching threshold now becomes $V_{OS} - V_H/2$. The comparator output will remain in a "1" state until the threshold $V_{OS} - V_H/2$ is crossed, coming from the positive direction. Input noise centered around V_{OS} will not cause the comparator to switch states unless it exceeds the region bounded by $V_{OS} \pm V_H/2$.

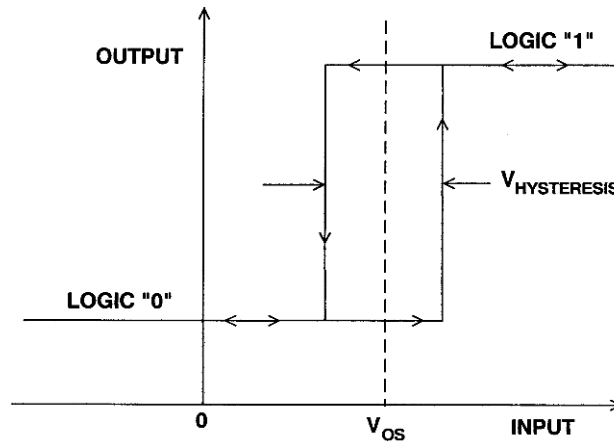
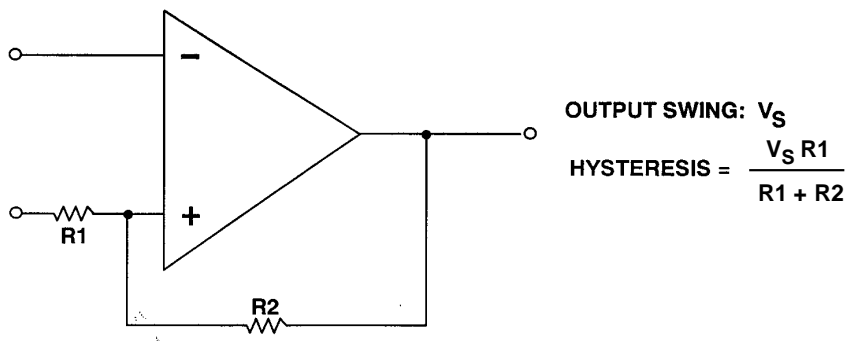


Figure 4: Effects of Hysteresis

Hysteresis can be accomplished with two resistors (see Figure 5), and the amount of hysteresis is proportional to the resistors' ratio. The signal input to the comparator may be applied to either the inverting or the non-inverting input, but if it is applied to the inverting input its source impedance must be low enough to have insignificant effect on R1 (of course if the source impedance is sufficiently predictable it may be used as R1).



- Input signal may be applied to either input but its source impedance must be low if it is applied to R1

Figure 5: Application of Hysteresis

If the trip voltage is midway between the two comparator output voltages (as is the case with a symmetrical power supply and a ground reference) then the introduction of hysteresis will move

the positive and negative thresholds equal distances from the trip point voltage, but if the trip point is nearer to one output than to the other the thresholds will be asymmetrically placed about the trip point voltage.

To calculate the hysteresis, assume the comparator output voltages are V_P and V_N respectively. The comparator trip point voltage is V_{TP} . The negative threshold is:

$$\text{NEGATIVE THRESHOLD} = \frac{(R1 + R2)V_{TP} - R1V_N}{R2} \quad \text{Eq. 1}$$

And the positive threshold voltage is:

$$\text{POSITIVE THRESHOLD} = \frac{(R1 + R2)V_{TP} - R1V_P}{R2} \quad \text{Eq. 2}$$

An example of how external hysteresis improves comparator response is shown in Figure 6.

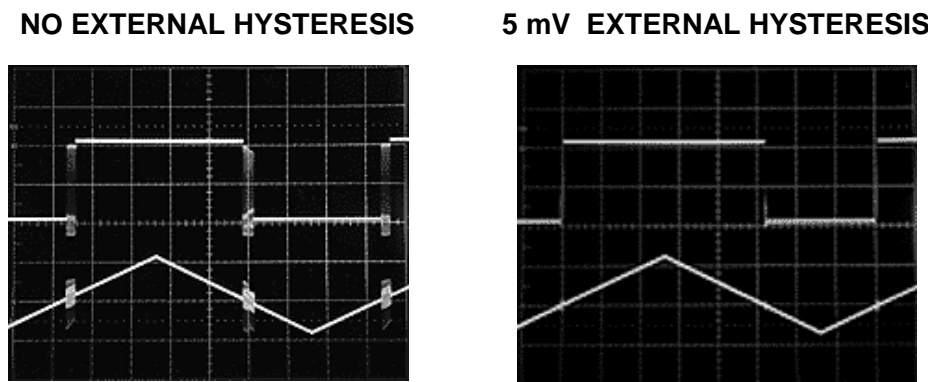


Figure 6: Hysteresis Helps Clean Up Comparator Response

A problem encountered with external hysteresis is that the output voltage depends on supply voltage and loading. This means the hysteresis voltage can vary from application to application; though this affects resolution, it need not be a serious problem, since the hysteresis is usually a very small fraction of the range and can tolerate a safety margin of two or three (or more) times what one might calculate. Swapping in a few comparators can help confidence in the safety margin. Don't use wirewound resistors for feedback; their inductance can make matters worse.

Don't forget that adding additional hysteresis to a comparator also reduces the comparators effective resolution. The minimum resolvable signal is equal to the difference in the threshold voltages, $V_P - V_N$.

Some comparators have hysteresis built in an example of this is the [AD790](#) (see Figure 7). The hysteresis voltage is nominally 500 μV . This, of course, can be overridden by applying external hysteresis.

The AD790 has an additional advantage. The supplies on the input (analog) side are not necessarily those on the output. The output swing is from V_{LOGIC} to GND. The input supplies can be ± 15 V down to +5 V and Ground.

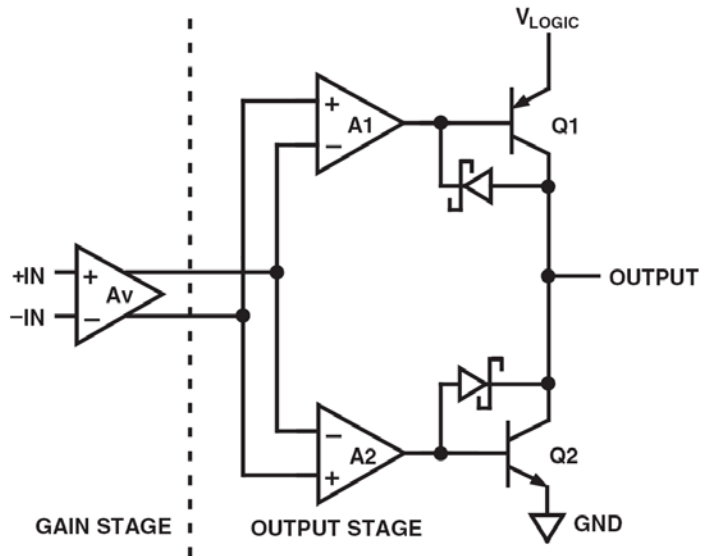


Figure 7: AD790 Block Diagram.

It is quite common for the output of a comparator to be open collector (TTL logic) or open drain (CMOS logic). This allows interfacing to whatever logic level is appropriate to the following circuitry. Note that the maximum allowable output voltage must be observed, but this is usually not too great an issue.

WINDOW COMPARATORS

A window comparator makes use of two comparators with different reference voltages and a common input voltage. The comparators are connected to logic in such a way that the final output logic level is asserted when the input signal falls between the two reference voltages as shown in Figure 8.

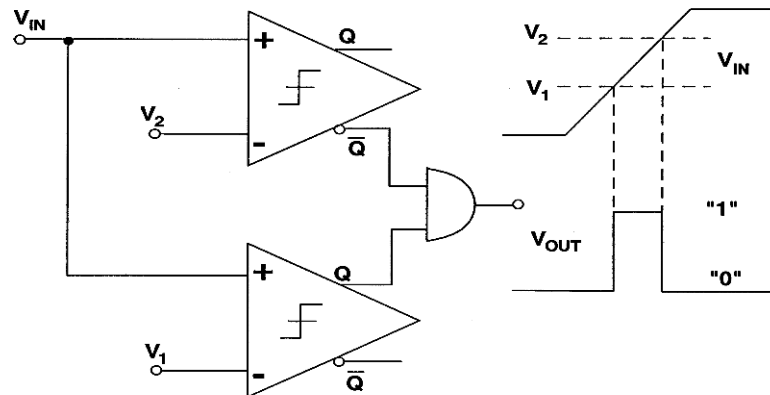


Figure 8: Window Comparator

LATCH ENABLE FUNCTION

Many comparators have an internal latch. The latch-enable signal has two states: *compare* (track) and *latch* (hold). When the latch-enable signal is in the compare state, the comparator output continuously responds to the sign of the net differential input signal. When the latch-enable signal transitions to the latch state, the comparator output goes to either a logic "1" or a logic "0", depending on the sign of the differential input signal at the instant of the transition (at this point, we are neglecting the setup and hold-time, as well as the output propagation delay associated with the latch-enable function). Even though many comparators have a latch-enable function, they are often operated only in the *compare* mode.

The comparator internal latch-enable function is particularly useful in ADC applications because it allows the comparator decision to be recorded *at a known instant of time*. Flash converters make use of this concept and are constructed of many parallel comparators which share a common latch-enable line. Typical timing associated with the latch-enable function is shown in Figure 9.

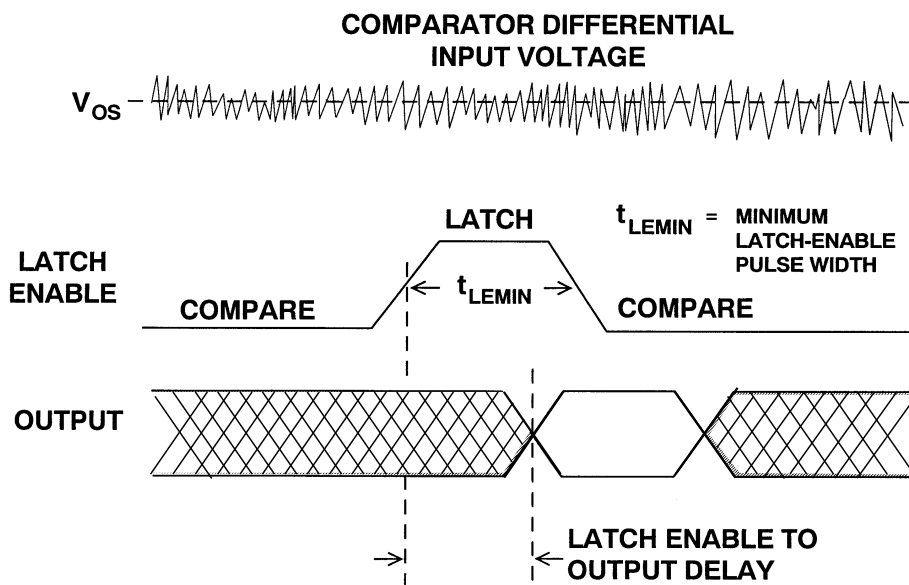


Figure 9: Effects of Output Latch

The delay between the assertion of latch-enable and the 50% point of the output logic swing is referred to as *latch-enable to output delay*. It may be different for positive and negative-going outputs. The other key specification associated with the latch-enable function is the minimum allowable latch-enable pulse width. This specification determines the maximum frequency at which the comparator can be strobed.

Fast comparators are somewhat difficult to apply because of their high gain and bandwidth. Proper application of high speed layout, grounding, decoupling, and signal routing is mandatory when using comparators. This can not be over emphasized. The biggest problem is their

tendency to oscillate when the input signal is very near to or equal to the switching threshold. This can also happen when a slow signal is compared to a dc reference. Hysteresis and the use of a narrow latch-enable pulse will generally help these conditions. TTL or CMOS output comparators are more likely to oscillate than ECL ones because of their large output swings and fast edges, often combined with power supply current spikes as the output changes state. This can feedback to the input in the form of noise.

REFERENCES:

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as [Linear Circuit Design Handbook](#), Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 4.
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3. [Analog Devices' Comparator Portfolio](#)

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