Our new ultralow noise, integer-N frequency synthesizers provide best-in-class phase noise and spurious performance. The LTC6946 is a complete frequency synthesizer that includes a high performance, low noise, 5.7GHz phase-locked loop (PLL) with a fully integrated, low phase noise VCO. The LTC6945 separates the low 1/f corner PLL core for use with an external VCO up to 6GHz. The free, easy-to-use PLLWizard™ CAD tool quickly and accurately simulates synthesizer performance to ensure an optimal design.

Features

- 350MHz to 6GHz VCO Input Range (LTC6945)
- Low –226dBc/Hz Normalized In-Band Phase Noise Floor
- –157dBc/Hz Wideband Output Phase Noise Floor
- Industry's Lowest –274dBc/Hz Normalized In-Band 1/f Noise
- Spurious Levels < –100dBc
- High Current 11mA Output Charge Pump Minimizes Loop Compensation Thermal Noise
- Programmable Output Divider for Wide Operating Frequency Range
- 28-Pin (4mm × 5mm) QFN Packages

<table>
<thead>
<tr>
<th>Frequency Coverage Options</th>
<th>LTC6946-1</th>
<th>LTC6946-2</th>
<th>LTC6946-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO Frequency (GHz)</td>
<td>2.240 to 3.740</td>
<td>3.080 to 4.910</td>
<td>3.840 to 5.790</td>
</tr>
<tr>
<td>OUT DIV = 1</td>
<td>2.240 to 3.740</td>
<td>3.080 to 4.910</td>
<td>3.840 to 5.790</td>
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<tr>
<td>OUT DIV = 2</td>
<td>1.120 to 1.870</td>
<td>1.540 to 2.455</td>
<td>1.920 to 2.895</td>
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<tr>
<td>OUT DIV = 3</td>
<td>0.747 to 1.247</td>
<td>1.027 to 1.637</td>
<td>1.280 to 1.930</td>
</tr>
<tr>
<td>OUT DIV = 4</td>
<td>0.560 to 0.935</td>
<td>0.770 to 1.228</td>
<td>0.960 to 1.448</td>
</tr>
<tr>
<td>OUT DIV = 5</td>
<td>0.448 to 0.748</td>
<td>0.616 to 0.982</td>
<td>0.768 to 1.158</td>
</tr>
<tr>
<td>OUT DIV = 6</td>
<td>0.373 to 0.623</td>
<td>0.513 to 0.818</td>
<td>0.640 to 0.965</td>
</tr>
</tbody>
</table>

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LTC6946-X Frequency Synthesizer Block Diagram

Design Features
- Find Part Parameters Based on Your Frequency Plan
- Design Noise-Optimized Loop Filters
- Simulate Loop Frequency Response and Stability
- Simulate VCO and Reference Source Noise
- Simulate Output Noise Characteristics and Statistics

Evaluation Features
- Read and Write All Device Registers
- Configure Using a Block Diagram Programming Interface
- Troubleshoot Common Set-Up Problems
- Receive Alerts Due to Programming Errors

PLLWizard Tool Provides Design Support

Design Features
- Proprietary noise-limiting input section delivers optimal phase noise performance with sine wave input signals.
- Buffered REF OUT (10MHz to 250MHz)
- SPI Serial Port
- Configurable Status Output
- Programmable output divider settable to any integer from 1 to 6.
- Output is always 50% duty cycle.

Evaluation Features
- On-chip temperature-compensated VCO (external on LTC6945).
- Never needs recalibration.
- Low noise charge pump with programmable output current up to 11mA
- Normalized in-band phase noise floor = –226dBc/Hz
- Proprietary noise-limiting input section delivers optimal phase noise performance with sine wave input signals.

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