

# I<sup>2</sup>C Quick Guide



## I<sup>2</sup>C Standard

The I<sup>2</sup>C (inter-IC) bus is a 2-wire, multi-drop, digital communications link for ICs that has become the defacto standard for many embedded applications. Serial, 8-bit, bidirectional data transfer can occur at speeds up to 3.4Mbps, though 400kHz is usually sufficient. Since only two bus lines are required, a serial data line (SDA) and serial clock line (SCL), building a system with multiple master or slave devices is relatively simple. The number of I<sup>2</sup>C devices that can be connected to a single I<sup>2</sup>C bus segment is limited only by a maximum bus capacitance (400pF) and address space.

### I<sup>2</sup>C vs SMBus vs PMBus

Specification		I <sup>2</sup> C	SMBus		PMBus
			High Power	Low Power	
Signaling	Packet Error Checking (Optional)	–			•
	SMBALERT (Optional)	–			•
	Block Size Limit	–	32 bytes		255 bytes
Timing	Data Rate (Standard Mode)		100kbps		
	Data Rate (Fast Mode)	400kbps	–	–	400kbps
	Data Rate (Fast Mode Plus)	1Mbps	–	–	–
	Data Rate (High Speed Mode)	3.4Mbps	–	–	–
	Clock Speed	0Hz to 3.4MHz	10kHz to 100kHz		10kHz to 400kHz
	Bus Timeout	–	25ms to 35ms		
	Bus Master Request Delay (Min)	–	50µs		
	SCL Hold Time (Max)	–	2ms		
Data Hold Time (Min)	–	300ns			
Electrical	Capacitance Load per Bus Segment (Max)	400pF		–	400pF
	Rise Time (Max)	1µs at 100kHz, 300ns at 400kHz	1µs		1µs at 100kHz, 300ns at 400kHz
	Pull-Up Current at 0.4V (Max)	3mA (Standard Mode and Fast Mode)	4mA	350µA	4mA
	Leakage Current per Device (Max)	±10µA		±5µA	±10µA
	V <sub>IL</sub> Input Logic Low Threshold (Max)	0.3V <sub>DD</sub> or 1.5V	0.8V		
	V <sub>IH</sub> Input Logic High Threshold (Min)	0.7V <sub>DD</sub> or 3V	2.1V		
	V <sub>OL</sub> Output Logic Low Threshold (Max)		0.4V		

### Frequently Asked Questions

#### Q1) How are I<sup>2</sup>C, SMBus and PMBus related?

Answer: Originally developed to facilitate battery management systems, SMBus uses I<sup>2</sup>C hardware but adds second-level software, which ultimately allows devices to be hot swapped without restarting the system. PMBus extends SMBus by defining a set of device commands specifically designed to manage power converters, exposing device attributes such as measured voltage, current, temperature and more. In general, I<sup>2</sup>C, SMBus and PMBus devices can share a bus without any major issues.

#### Q2) How do I build a large system and still meet bus capacitance and rise time specifications?

Answer: Linear Technology's bus buffers resolve common electrical limitations posed by specifications, thereby allowing more devices to be added to the bus. These devices break up large busses into several smaller I<sup>2</sup>C compliant (<400pF) pieces, while still providing simultaneous communications to all bus segments and optionally injecting a boosted pull-up current during positive bus transitions to quickly slew large bus capacitances.

#### Q3) How do I resolve a stuck bus?

Answer: Other than having a host try to manually fix a bus stuck low, Linear Technology's bus buffers provide stuck bus protection which recovers a stuck bus by automatically generating pulses on SCLOUT in an attempt to unstick the bus. Otherwise, a hard reset is required.

#### Q4) How do I increase the number of I<sup>2</sup>C addresses available?

Answer: Linear Technology's software and hardware controlled I<sup>2</sup>C multiplexers provide the ability to address one of multiple identical devices or simply increase fan-out, thus resolving address conflict issues, while also providing Hot Swap™ capabilities, bus buffering, rise time acceleration and stuck bus protection.



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# I<sup>2</sup>C Checklist ✓

Linear Technology provides a comprehensive family of I<sup>2</sup>C-enabled devices for a variety of applications. From Hot Swap™ controllers to bus isolators, these devices provide on-the-fly adjustability, enhance I<sup>2</sup>C performance or simply enable designers to easily manage key system parameters.

