LT1813: 100MHz, 750V/µs Amplifier Draws Only 3mA

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Introduction

The LT1813 is a 100MHz dual operational amplifier that has been optimized for supply voltages under 12V. It features an easy-to-use voltage feedback topology with high impedance inputs, yet it slews 750V/µs with only 3mA supply current. DC performance has not been neglected —the device has a 1.5mV maximum V_{OS} and a 400nA maximum I_{OS}.

Performance

A summary of important specifications of the LT1813, compared to its higher voltage brethren, is shown in Table 1. A key figure of merit is the ratio of gain bandwidth to supply current (GBW/I_{SUPPLY}, expressed in units of MHz/mA). The new process employed by the LT1813 forsakes high supply voltage operation for a 3×–4× increase in MHz/mA compared to the LT1361 and LT1364. Blazing speed from such a modest amount of supply current is extremely attractive for low power applications. The LT1813 also propagates the family traits of matched, high input impedance inputs and low V_{OS}, I_B, I_{OS} and input noise. The improved common mode input range of the LT1813 adds to its utility in low supply voltage applications. Stability with capacitive loading is another distinctive and desirable feature. Although the LT1813 is not stable with unlimited capacitive loads, it is stable with nearly two orders of magnitude more capacitance than competitors' high speed amplifiers. The small-signal transient response in unity gain with C_{LOAD} =100pF, 500pF and 1000pF is shown in Figure 1.

Table 1. Comparison of dual, high speed op amps (V_S = ±5V, 25°C)

	LT1813	LT1364	LT1361
Gain Bandwidth	100MHz	50MHz	37MHz
Supply Current per Amplifier	3.0mA	6.0mA	3.8mA
GBW/I_{SUPPLY}	33.3MHz/mA	8.3MHz/mA	9.7MHz/mA
Slew Rate	750V/µs	450V/µs	350V/µs
Input Common Mode Range	±4.0V	+3.4V, –3.2V	+3.4V, –3.2V
Output Swing	±4.0V	±4.1V	±4.0V
Output Current (V_{OUT} = ±3V)	60mA	45mA	38mA
V_{OS} (Max)	1.5mV	1.5mV	1.0mV
I_B (Max)	4.0µA	2.0µA	1.0µA
I_{OS} (Max)	400nA	350nA	250nA
A_{VOL} (Min)	1.5V/mV	3.5V/mV	3V/mV
Input Noise Voltage	8nV/√Hz	9nV/√Hz	9nV/√Hz
Input Noise Curent	1pA/√Hz	1pA/√Hz	0.9pA/√Hz
C_{LOAD}	1000pF	∞	∞
Max Supply Voltage (V^+ to V^-)	12.6V	36V	36V

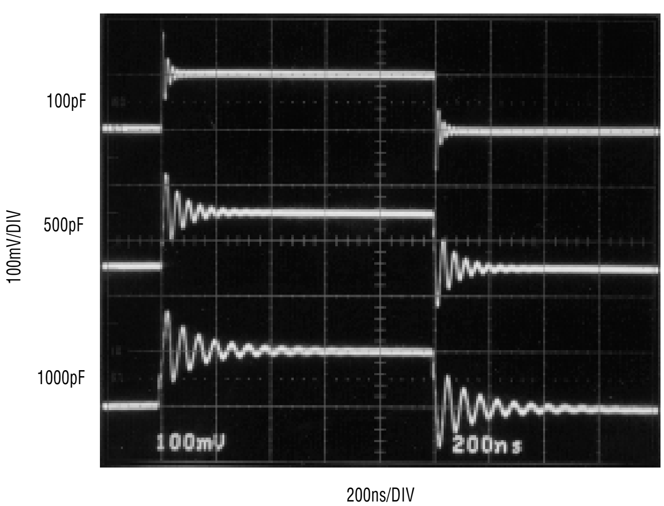

Figure 1. LT1813 in a gain-of-one configuration, no R_L; C_L = 100pF, 500pF or 1000pF

The LT1813 extends the frequency response of applications such as active filters, instrumentation amplifiers and buffers. Figure 2 shows the LT1813 converting a single-ended signal to a differential drive for the LTC1417 14-bit analog-to-digital converter (ADC). Note that the top amplifier provides unity voltage gain, but the amplifier is configured in a noise-gain of 2 to match the phase response of the bottom amplifier, which has a gain of –1. The filter in front of the ADC reduces broadband noise. The spurious free dynamic range (SFDR) of this circuit is –79dB for a 425kHz, $2V_{P-P}$ input.

Circuit Design

A simplified schematic of the circuit is shown in Figure 3. The circuit looks similar to a current feedback amplifier, but both inputs are high impedance as in a traditional voltage feedback amplifier. A complementary cascade of emitter followers, Q1–Q4, buffers the noninverting input and drives one side of resistor R1. The other side of the resistor is driven by Q5–Q8, which form a buffer for the inverting input. The input voltage appears across the resistor, generating currents in Q3 and Q4 that are mirrored by Q9–Q11 and Q13–Q15 into the high impedance node. Transistors Q17–Q24 form the output stage. Bandwidth is set by R1, the g_m's of Q3, Q4, Q7 and Q8 and the compensation capacitor, C_T.

The voltage drops of Q1–Q4 and the diodes Q10 and Q14 set the input common mode range of the amplifier. The emitters of Q3 and Q4 follow the noninverting input. As the input approaches either supply rail, the limiting voltage is determined by the saturation of Q3 or Q4, which occurs at approximately a V_{BE} plus a V_{SAT} from the supply rail. Typically, the input common mode range is 1V from either supply rail, and is guaranteed by the CMRR specification to be 1.5V from either rail. This excellent input range is achieved without compromising the output impedance of the mirrors Q9–Q11 and Q13–Q15, because Q25 and Q26 provide floating bias points for cascode devices Q9 and Q13. Lower bandwidth processes cannot successfully use this technique and maintain high bandwidth, due to phase shift in the mirror.

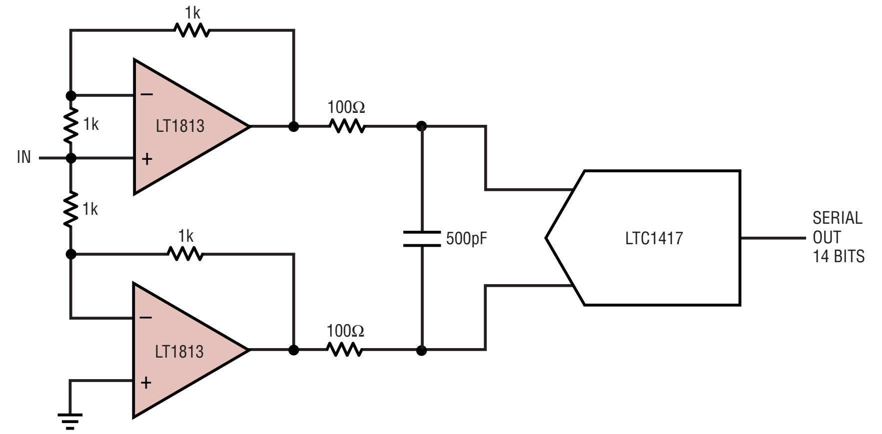

Figure 2. Single-ended to differential ADC buffer: $2V_{P-P}$ input at 425kHz yields –79dB SFDR

The current available to slew compensation capacitor C_T is proportional to the voltage that appears across R1. This method of “slew boost” achieves low distortion due to its inherent linearity with input step size. Large slew currents can be generated without increasing quiescent current. A low value for R1 reduces the input noise voltage to $8nV/\sqrt{Hz}$ and helps reduce input offset voltage and drift. The LT1813 is built with small-geometry, multi-GHz transistors that produce abundant bandwidth with meager operating currents and allow for further reduction of idling supply current.

The output stage buffers the high impedance node from the load by providing current gain. The simplest output stage would be two pairs of complementary emitter followers, which would provide a current gain of $Beta_{NPN} \times Beta_{PNP}$. Unfortunately, this gain is insufficient for driving even modest loads. Adding another emitter-follower or a Darlington configuration reduces output swing and creates instability with large capacitive loads.

The solution used on the LT1813 was to create a pair of composite transistors formed by transistors Q19–Q21 and Q22–Q24. The current mirrors attached to the collectors of emitter followers Q19 and Q22 provide additional current gain. The ratio of transistor geometries Q20 to Q21 and Q23 to Q24 increase the current gain by approximately fifteen. There

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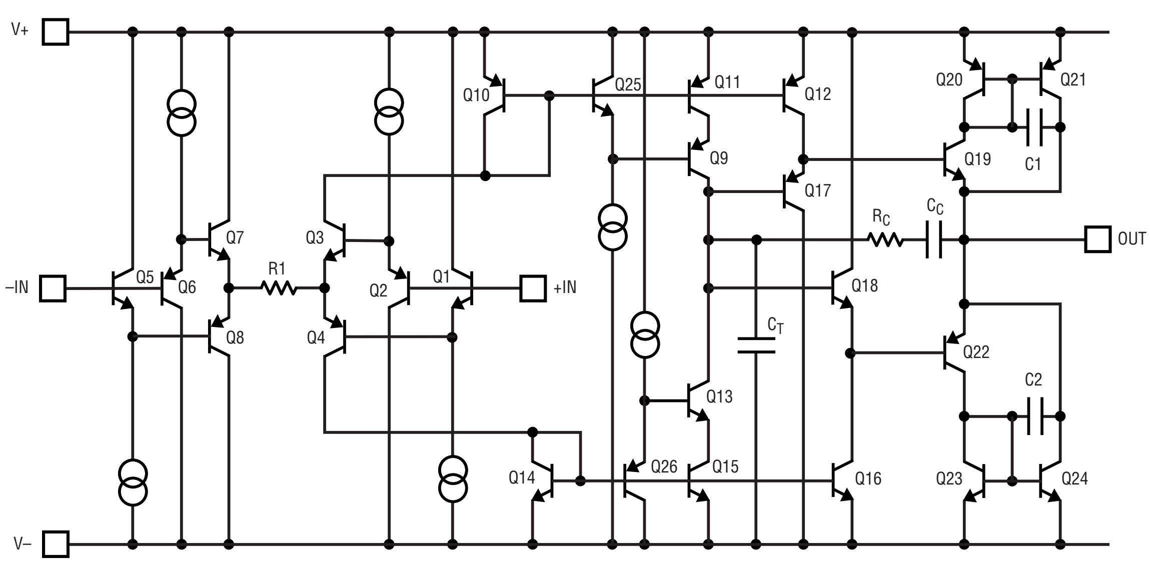

Figure 3. LT1813 simplified schematic

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is no output swing penalty as the swing is limited at the collectors of Q9 and Q13. The dynamics of the composites are not as benign as those of emitter followers, so compensation is required and is provided by C1 and C2.

The stability with capacitive loads is provided by the R_C, C_C network between the output stage and the gain node. When the amplifier is driving a light or moderate load, the output can follow the high impedance node and the network is bootstrapped and has no effect. When driving a heavy load such as a capacitor or small-value resistor, the network is incompletely bootstrapped and adds to the compensation provided by C_T. The added capacitance provided by C_C slows down the amplifier and the zero created by R_C adds phase margin to increase stability.

Conclusion

The combination of a high slew rate, DC accuracy and a frugal 3mA-per-amplifier supply current make the LT1813 a compelling choice for low voltage and low power, high speed applications.