LINEAR TECHNOLOGY

DESIGN NOTES

Low Voltage Hot Swap Controller Ignores Backplane Noise and Surges – Design Note 319

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First generation single supply Hot Swap™ controllers, such as the LTC®1422, combine the features of various discrete inrush limiting circuits into a single IC, including an electronic circuit breaker, adjustable power-up rate, reset output, high side MOSFET gate drive, undervoltage lockout and a wide operating voltage range. The LTC4211 advances these features by adding a dual level, dual response time electronic circuit breaker, adjustable soft-start with inrush current limiting, fault detection, faster response time to severe overloads and operation from 2.5V to 16.5V—all in a small 10-lead MSOP package.

Control 25W with a 10-Lead MS Package

Figure 1 shows a 5V, 5A Hot Swap application designed for inclusion on a removable circuit board. As is customary, the circuit board ground and V_{CC} planes are wired to long connector pins, eliminating reliability problems associated with pin-to-receptacle arcing. Until the PC board is firmly seated in the backplane, the MOSFET switch remains safely off and isolates C_{LOAD} (typically 100µF or more) from the backplane. Once the connector is fully seated, the R1-R2 divider which serves both as a connection sense and an undervoltage lockout, activates the LTC4211. When activated, the LTC4211 waits one TIMER pin period as set by C_{TIMER} and then turns on the MOSFET. $\overline{\text{RESET}}$ signals a successful start-up as measured by divider R3-R4 and the FB pin.

Dual Level Current Control

Advanced current control features separate the LTC4211 from other Hot Swap controllers. The SENSE pin monitors load current and shuts off the MOSFET in the event the current exceeds 50mV/R_{SENSE}. Instead of using a simple circuit breaker approach, the SENSE pin has two thresholds: a slow 50mV trip point whose timing is governed by C_{FILTER} at the FILTER pin, and a fast 150mV (3×) trip point which triggers in just 300ns to interrupt the flow of current in the event a catastrophic fault occurs on the output. Thus, the LTC4211 ignores temporary surges and overloads but responds quickly when a genuine fault is detected.

Inrush Limiting

Conspicuous by its absence in Figure 1 is a gate capacitor which might otherwise define the ramp rate and therefore the inrush current of the output during start-up. Instead, the 50mV SENSE pin threshold is used to servo the inrush current to a value of 50mV/R_{SENSE}. The 50mV threshold circuit breaker function is suspended during this critical period, but the 150mV SENSE threshold remains active to catch catastrophic faults. Once the soft-start period is over, the 50mV circuit breaker is armed.

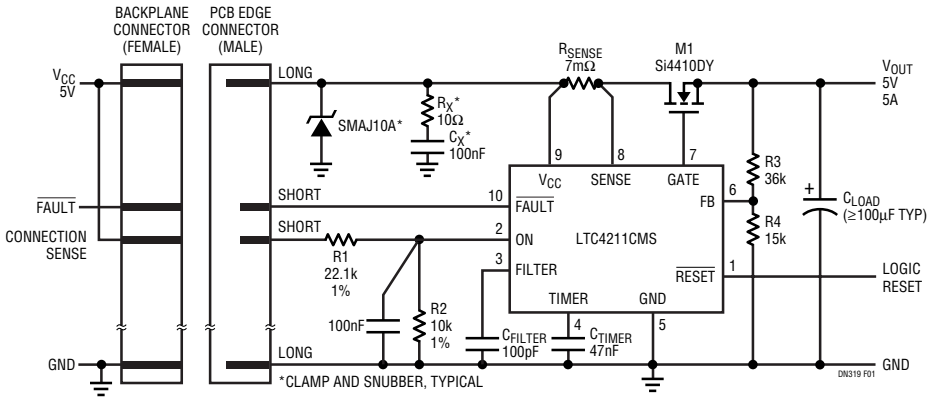

Figure 1. Single Channel 5V Hot Swap Controller in 10-Lead MS with Dual Level Current Control

There are several advantages to dispensing with the usual gate capacitor including the elimination of an external component and the elimination of the turn-off delay inherent in discharging that capacitor during a fault. Even so, the LTC4211 is not restricted to using its internal current control mode at start-up—an external capacitor can still be employed in the ordinary way, integrating the 10µA GATE pin current to produce a well-controlled soft-start ramp. An 8-pin version, the LTC4211CS8 is available as a backwards-compatible upgrade to the LTC1422CS8 in applications demanding current limited start-up.

Adaptive Response to Overloads

During start-up, the LTC4211 operates in the aforementioned 50mV/R_{SENSE} current limit mode (regardless of whether a gate capacitor is included in the design) at any time the 50mV threshold is exceeded. For example, if the LTC4211 attempts to start up into a short circuit, the current is first limited to 50mV/R_{SENSE} and then cut off after the expiration of one TIMER pin cycle.

After successful start-up, the timed circuit breaker function takes over. The 50mV threshold still applies, but instead of instantly tripping on an overcurrent condition, the FILTER circuit delays turn-off, thereby rejecting temporary surges and spikes. This prevents minor backplane disturbances from interrupting delivery of power to critical subsystems and memory.

Figure 2 illustrates the action of the FILTER pin. An overload of approximately 8A is drawn from the 5V output which exceeds the 50mV/7mΩ SENSE pin threshold. C_{FILTER} delays shutdown 100µs. A shorter duration overload would have been rejected. Extreme overloads must be recognized and cleared immediately to prevent collateral damage. The 150mV SENSE pin threshold reacts to these overloads in just 300ns, bypassing the FILTER pin delay.

Figure 2 also shows the importance of input clamping in high current applications. Readily recognized is the di/dt dip at the input, V_{CC}, precipitated by the ≈1A/µs load current slew rate coupled with a backplane/wiring harness inductance of nearly 3µH. There is no input bypassing. Upon commutation of the 8A load current, a potentially destructive consequence of the inductive feedpoint impedance rears its ugly head: a voltage spike limited only by the input clamp. The LTC4211's high absolute maximum V_{CC} rating of 17V eases selection of an appropriate clamp, as these devices tend to have wide tolerances.

Recovery from Faults

Once the circuit breaker has tripped, for whatever reason, the LTC4211 safely latches off and helps guard against any damage to the MOSFET or affected circuitry. The $\overline{FAULT}$ pin then alerts the system controller for further action. The circuit breaker can be reset by either cycling the ON pin low under microprocessor control or by allowing the chip to reset itself (by tying $\overline{FAULT}$ back to the ON pin).

$\overline{FAULT}$ also serves as an input. If $\overline{FAULT}$ is pulled low externally by another open drain logic signal, the LTC4211 circuit breaker trips and turns off the output. This feature allows multiple supplies to shut down simultaneously when a short circuit occurs on any one output. The $\overline{FAULT}$ pin of each LTC4211 is wired to a common point, so that a fault on one is communicated to the others.

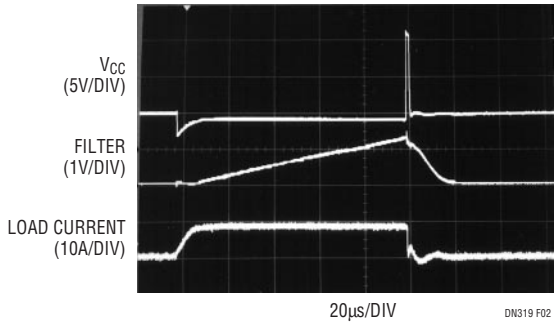

Figure 2. Temporary Surges and Spikes are Rejected During the Time Set by the FILTER Pin. A Persistent Overload of ≈8A Trips the Circuit Breaker After a 100µs FILTER Delay

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