Dual DC/DC Controller for DDR Power with Differential V_{DDQ} Sensing and \pm 50mA V_{TT} Reference

Design Note 503
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Introduction
The LTC®3876 is a complete DDR power solution, compatible with DDR1, DDR2, DDR3 and DDR4 lower voltage standards. The IC includes V_{DDQ} and V_{TT} DC/DC controllers and a precision linear V_{TT} reference. A differential output sense amplifier and precision internal reference combine to offer an accurate V_{DDQ} supply. The V_{TT} controller tracks the precision VTTR linear reference with less than 20mV total error. The precision VTTR reference maintains 1.2% regulation accuracy, tracking one-half V_{DDQ} over temperature for a \pm 50mA reference load.

The LTC3876 features controlled on-time, valley current mode control, allowing it to accept a wide 4.5V to 38V input range, while supporting V_{DDQ} outputs from 1.0V to 2.5V, and V_{TT} and VTTR outputs from 0.5V to 1.25V. Its phase-locked loop (PLL) can be synchronized to an external clock between 200kHz and 2MHz. It also features voltage-tracking soft-start, PGOOD and fault protection.

High Efficiency, 4.5V to 14V Input, Dual Output DDR Power Supply
Figure 1 shows a DDR3 power supply that operates from a 4.5V to 14V input. Figure 2 shows efficiency curves for discontinuous and forced continuous modes of operation.

Load-Release Transient Detection
As output voltages drop, a major challenge for switching regulators is to limit the overshoot in V_{OUT} during a load-release transient. The LTC3876 uses the DTR pin to monitor the first derivative of the ITH voltage to detect load release transients. Figure 3 shows how this pin is used for transient detection.

The two R_{ITH} resistors establish a voltage divider from INTV_{CC} to SGND, and bias the DC voltage on the DTR pin (at steady-state load or ITH voltage) slightly above half of INTV_{CC}. For a given C_{ITH1}, this divider does not

Figure 1. 1.5V V_{DDQ}/20A 0.75V V_{TT}/10A DDR3 Power Supply

Figure 2. Efficiency of Circuit in Figure 1 (V_{DDQ} = 1.5V, f_{SW} = 400kHz, L = 470nH)
change compensation performance as long as $R_{ITH1}/R_{ITH2}$ equals $R_{ITH}$ that would normally be used in conventional single-resistor OPTI-LOOP® compensation.

The divider sets the RC time constant needed for the DTR duration. The DTR sensitivity can be adjusted by the DC bias voltage difference between DTR and half INTVCC. This difference could be set as low as 100mV, as long as the ITH ripple voltage with DC load current does not trigger the DTR. If the load transient is fast enough that the DTR voltage drops below half of INTVCC, a load release event is detected. The bottom gate (BG) is turned off, so that the inductor current flows through the body diode in the bottom MOSFET.

Note that the DTR feature causes additional losses on the bottom MOSFET, due to its body diode conduction. The bottom FET temperature may be higher with a load of frequent and large load steps—an important design consideration. Test results show a 20°C increase when a continuous 100%-to-50% load step pulse chain with 50% duty cycle and 100kHz frequency is applied to the output.

**VTT Reference (VTTR)**

The linear VTT reference, VTTR, is specifically designed for large DDR memory systems by providing superior accuracy and load regulation for up to ±50mA output load. VTTR is the buffered output of the VTT differential reference resistor divider. VTTR is a high output linear reference, which tracks the VTT differential reference resistor divider and equals half of the remote-sense VDDQ voltage.

Connect VTTR directly to the DDR memory VREF input. Both input and output supply decoupling are important to performance and accuracy. A 2.2μF output capacitor is recommended for most typical applications. It is suggested to use no less than 1μF and no more than 47μF on the VTTR output. The VTTR power comes from the VTTRVCC pin. The typical recommended input VTTRVCC RC decoupling filter is 2.2μF and 1Ω. When VDDQSNS is tied to INTVCC, the VTTR linear reference output is 3-stated and VTTR becomes a reference input pin, with voltage from another LTC3876 in a multiphase application.

**VTT Supply**

The $V_{TT}$ supply reference is connected internally to the output of the VTTR $V_{TT}$ reference output. The $V_{TT}$ supply operates in forced continuous mode and tracks $V_{DDQ}$ in start-up and in normal operation regardless of the MODE/PLLIN settings. In start-up, the $V_{TT}$ supply is enabled coincident with the $V_{DDQ}$ supply. Operating the $V_{TT}$ supply in forced continuous mode allows accurate tracking in start-up and under all operating conditions.

**Conclusion**

The LTC3876 is a complete high efficiency and high accuracy solution for DDR memory power supplies. The unique controlled on-time architecture allows extremely low step-down ratios while maintaining a fast, constant switching frequency. The wide input voltage range of 4.5V–38V and programmable, synchronizable switching frequency from 200kHz to 2MHz gives designers the flexibility needed to optimize their systems.

For applications help, call (408) 432-1900, Ext. 3598