4M x 16bit CMOS Dynamic RAM with Fast Page Mode

DESCRIPTION

This is a family of 4,194,304 x 16 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx16 Fast Page Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- **Part Identification**

  - K4F661612B-TC/L(3.3V, 8K Ref., TSOP)
  - K4F641612B-TC/L(3.3V, 4K Ref., TSOP)

- **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	360	468
-50	324	432
-60	288	396

- **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4F661612B*	8K	64ms	128ms
K4F641612B	4K		

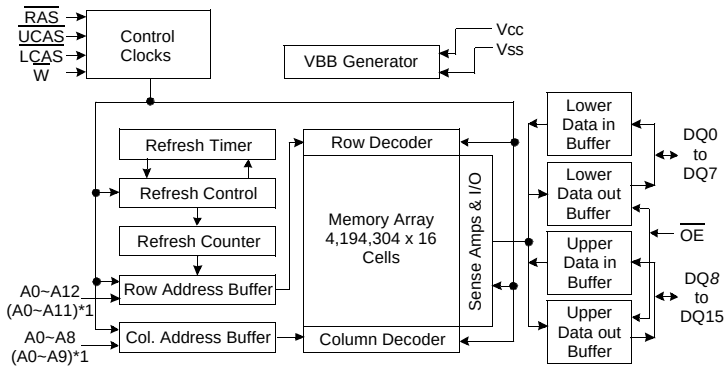
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

- **Performance Range**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
-45	45ns	12ns	80ns	31ns
-50	50ns	13ns	90ns	35ns
-60	60ns	15ns	110ns	40ns

- Fast Page Mode operation
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- +3.3V±0.3V power supply

FUNCTIONAL BLOCK DIAGRAM



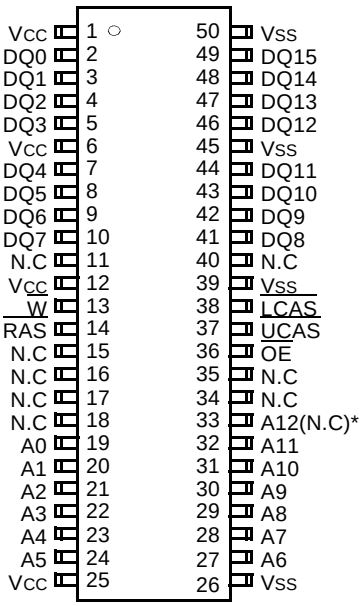
Note) *1 : 4K Refresh

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PIN CONFIGURATION (Top Views)

• **K4F661612B-T**
• **K4F641612B-T**



(400mil TSOP(II))

*(N.C) : N.C for 4K Refresh Product

Pin Name	Pin function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 15	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+3.3V)
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 to +6.5	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	+5.5*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : 6.5V at pulse width ≤15ns which is measured at V_{CC}
*2 : -1.3 at pulse width ≤15ns which is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

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DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4F661612B	K4F641612B	
I_{CC1}	Don't care	-45 -50 -60	100 90 80	130 120 110	mA mA mA
I_{CC2}	Normal L	Don't care	2 2	2 2	mA mA
I_{CC3}	Don't care	-45 -50 -60	100 90 80	130 120 110	mA mA mA
I_{CC4}	Don't care	-45 -50 -60	70 60 50	80 70 60	mA mA mA
I_{CC5}	Normal L	Don't care	500 300	500 300	uA uA
I_{CC6}	Don't care	-45 -50 -60	100 90 80	130 120 110	mA mA mA
I_{CC7}	L	Don't care	400	400	uA
I_{CCS}	L	Don't care	400	400	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @t_{PC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @t_{RC}=min)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V, $\overline{W}$, $\overline{OE}$=V_{IH}, Address=Don't care DQ=Open, T_{RC}=31.25us

I_{CCS} : Self Refresh Current

$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11)=V_{CC}-0.2V or 0.2V, DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

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CAPACITANCE (T_A=25°C, V_{CC}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition : V_{CC}=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	80		90		110		ns	
Read-modify-write cycle time	t_{RWC}	115		133		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		45		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		12		13		15	ns	3,4,5
Access time from column address	t_{AA}		23		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	13	0	13	ns	6
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	25		30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	45	10K	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	12		13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	13	10K	15	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	33	20	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	13	22	15	25	15	30	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	8		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	13
Column address hold time	t_{CAH}	8		10		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	23		25		30		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	8		10		10		ns	
Write command pulse width	t_{WP}	8		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	12		13		15		ns	16
Data set-up time	t_{DS}	0		0		0		ns	9,19
Data hold time	t_{DH}	10		10		10		ns	9,19

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	32		36		38		ns	7,15
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	67		73		83		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	43		48		53		ns	7
$\overline{CAS}$ precharge $\overline{W}$ delay time	t_{CPWD}	48		53		60		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		26		30		35	ns	3
Fast Page mode cycle time	t_{PC}	31		35		40		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	70		76		85		ns	
$\overline{CAS}$ precharge time (Fast page cycle)	t_{CP}	9		10		10		ns	14
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	45	200K	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	28		30		35		ns	
$\overline{OE}$ access time	t_{OEA}		12		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	12		13		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	13	0	13	0	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	12		13		15		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	11
Write command hold time (Test mode in)	t_{WTH}	15		15		15		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{WRH}	10		10		10		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RASS}	100		100		100		us	20,21,22
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{RPS}	80		90		110		ns	20,21,22
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	t_{CHS}	-50		-50		-50		ns	20,21,22

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TEST MODE CYCLE

(Note 11)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	85		95		115		ns	
Read-modify-write cycle time	t_{RWC}	120		138		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		55		65	ns	3,4,10,12
Access time from $\overline{CAS}$	t_{CAC}		17		18		20	ns	3,4,5,12
Access time from column address	t_{AA}		28		30		35	ns	3,10,12
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	55	10K	65	10K	ns	
$\overline{CAS}$ pulse width	t_{CAS}	17	10K	18	10K	20	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		55		65		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	28		30		35		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	37		41		43		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	72		78		88		ns	7
Column Address to $\overline{W}$ delay time	t_{AWD}	48		53		58		ns	7
Fast Page mode cycle time	t_{PC}	36		40		45		ns	
Fast Page mode read-modify-write cycle time	t_{PRWC}	75		81		90		ns	
$\overline{RAS}$ pulse width (Fast page cycle)	t_{RASP}	50	200K	55	200K	65	200K	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		31		35		40	ns	3
$\overline{OE}$ access time	t_{OEA}		17		18		20	ns	
$\overline{OE}$ to data delay	t_{OED}	17		18		18		ns	
$\overline{OE}$ command hold time	t_{OEH}	17		18		20		ns	

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NOTES

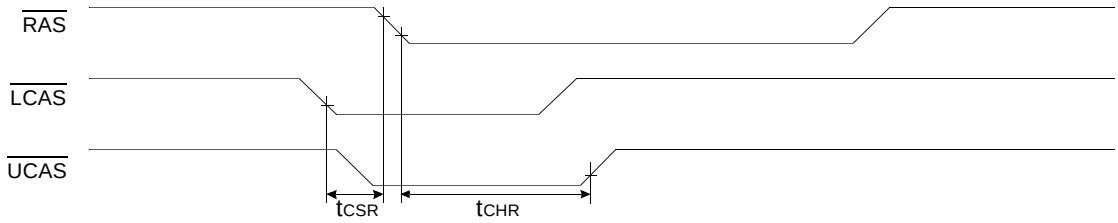
1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. t_{OFF}(min)and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{W}$ falling edge in read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

K4F64(6)1612B Truth Table

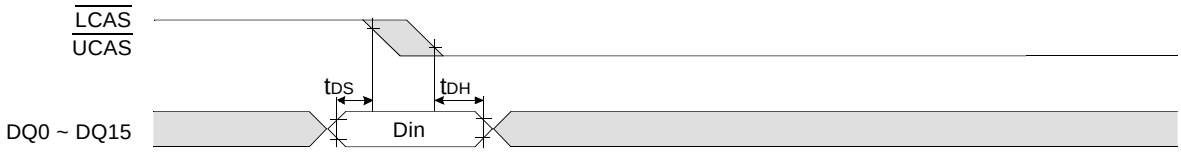
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

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13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
14. t_{CP} is specified from the later $\overline{CAS}$ rising edge in the previous cycle to the earlier $\overline{CAS}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. t_{CSR} is referenced to the earlier $\overline{CAS}$ falling edge before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising edge after $\overline{RAS}$ transition low.



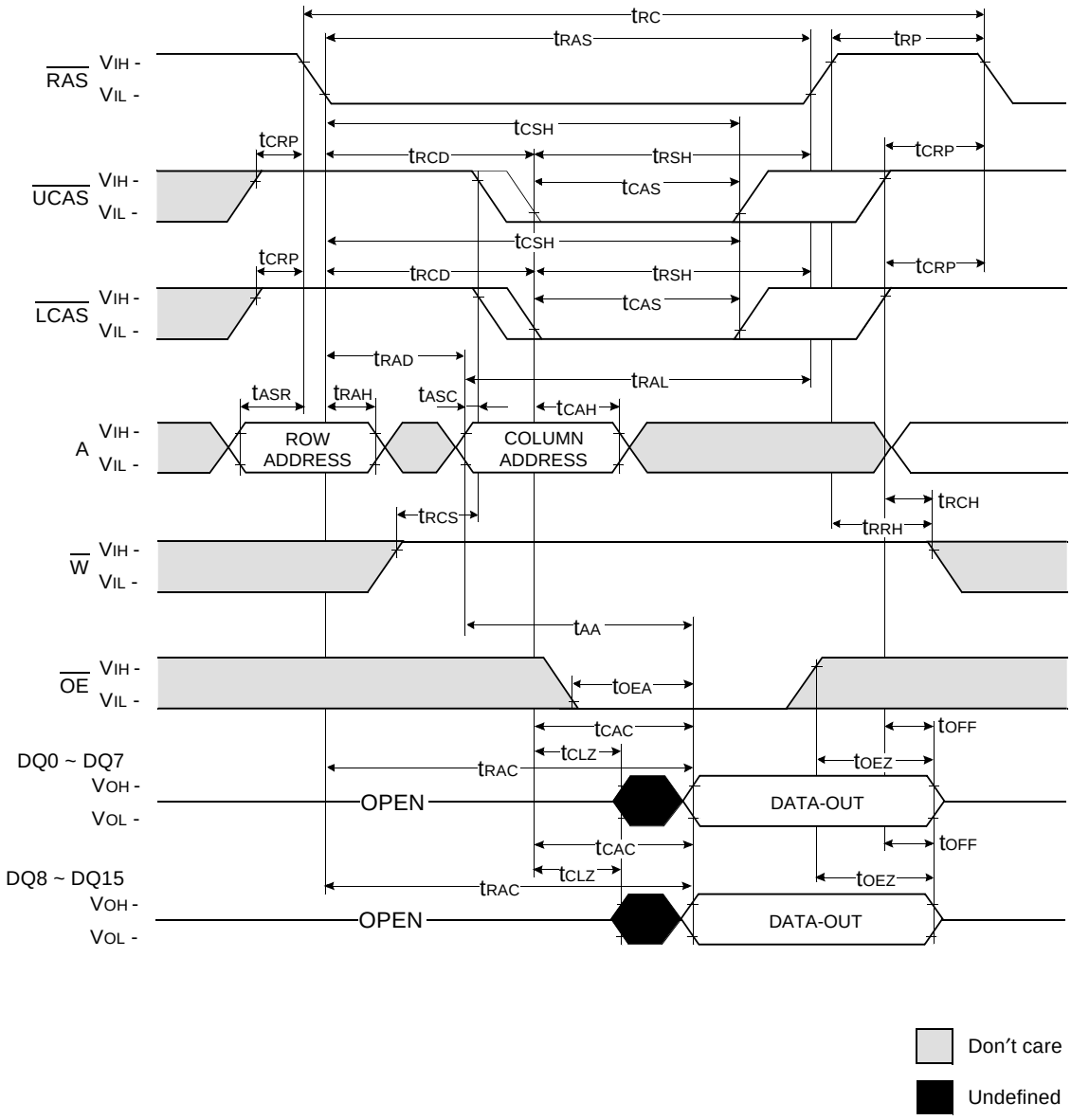
19. t_{DS} is specified for the earlier $\overline{CAS}$ falling edge and t_{DH} is specified by the later $\overline{CAS}$ falling edge.



20. If $t_{RASS} \geq 100us$, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
21. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(4K/8K) cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
22. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

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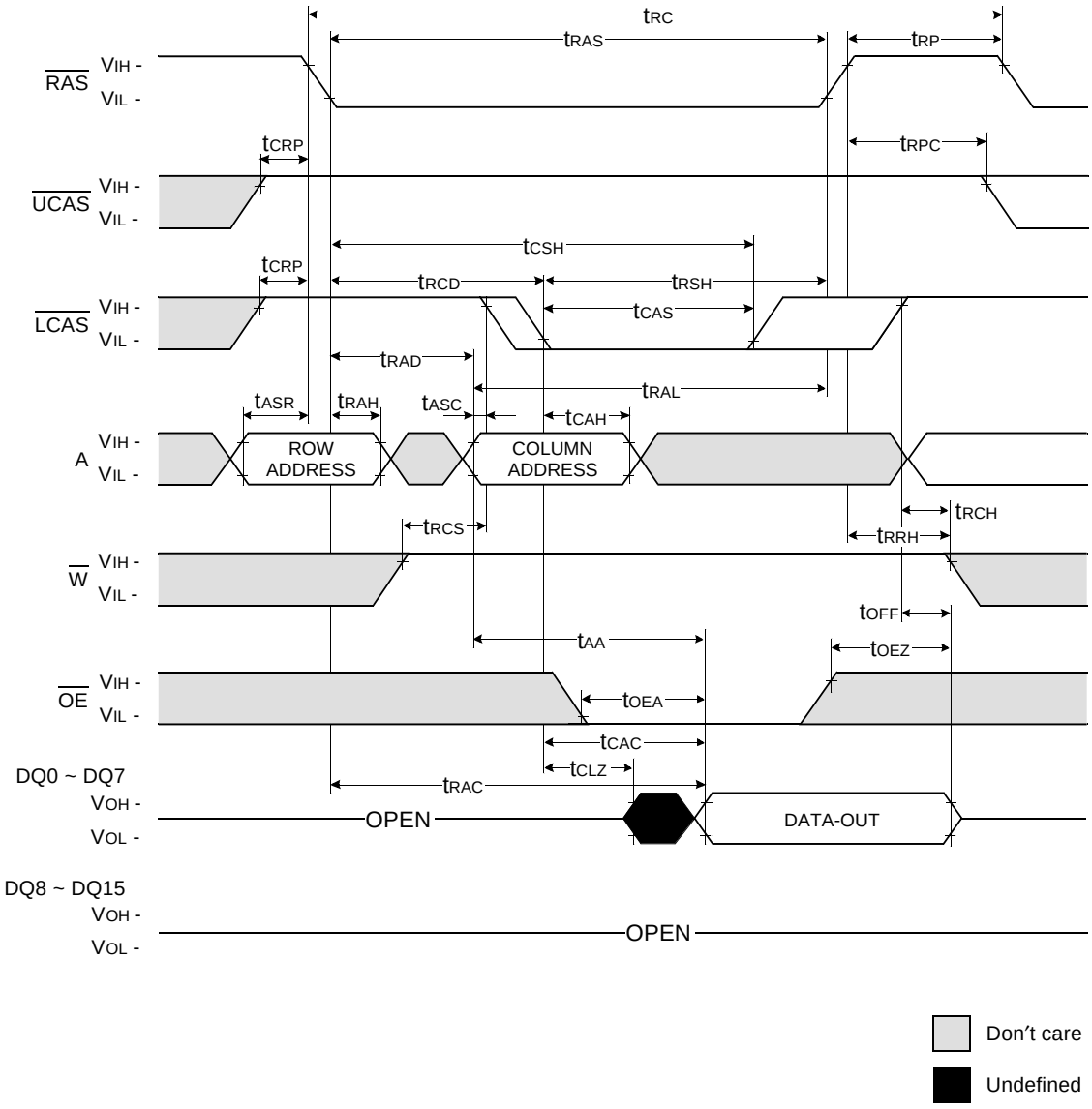
WORD READ CYCLE



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LOWER BYTE READ CYCLE

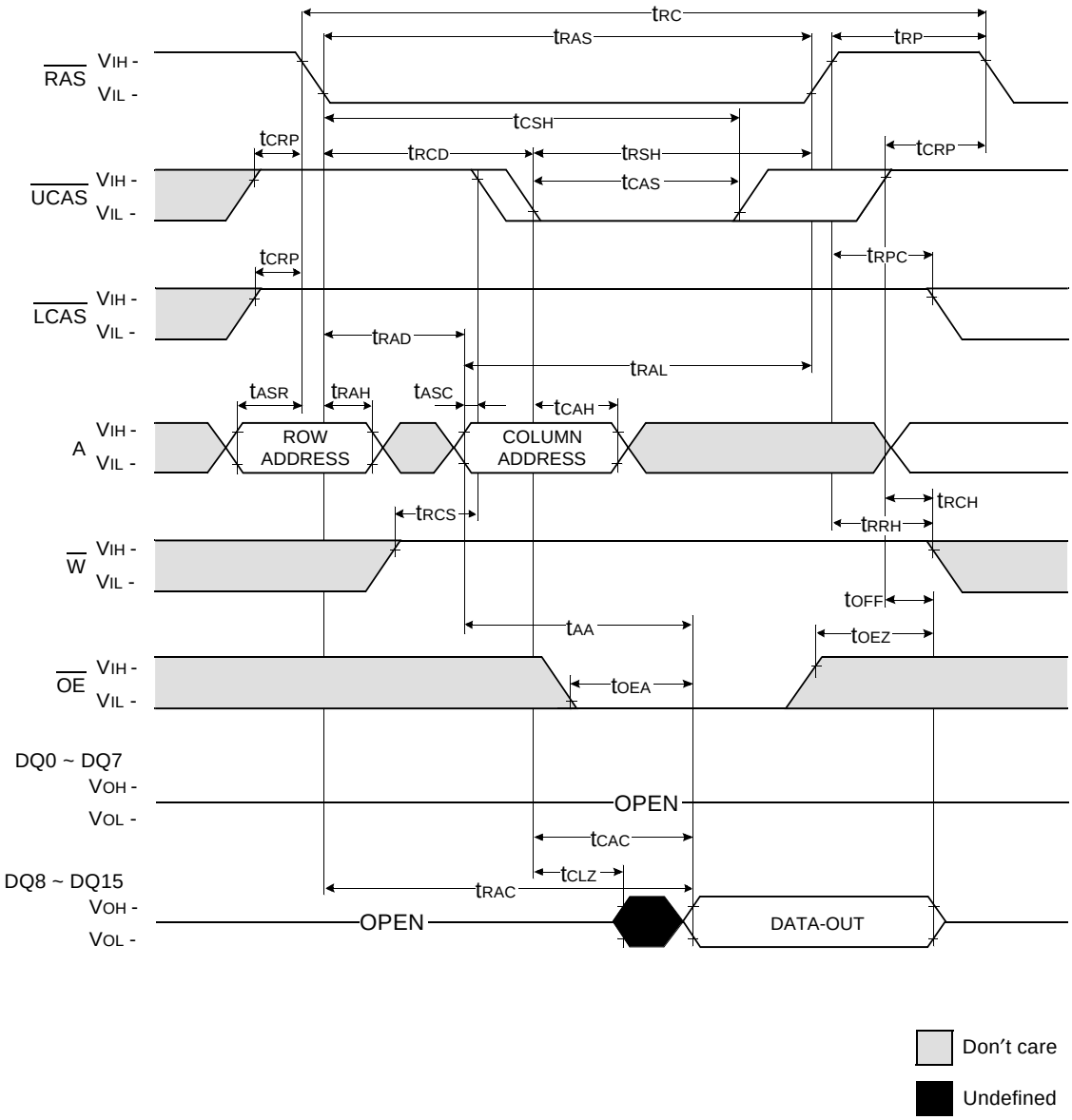
NOTE : DIN = OPEN



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UPPER BYTE READ CYCLE

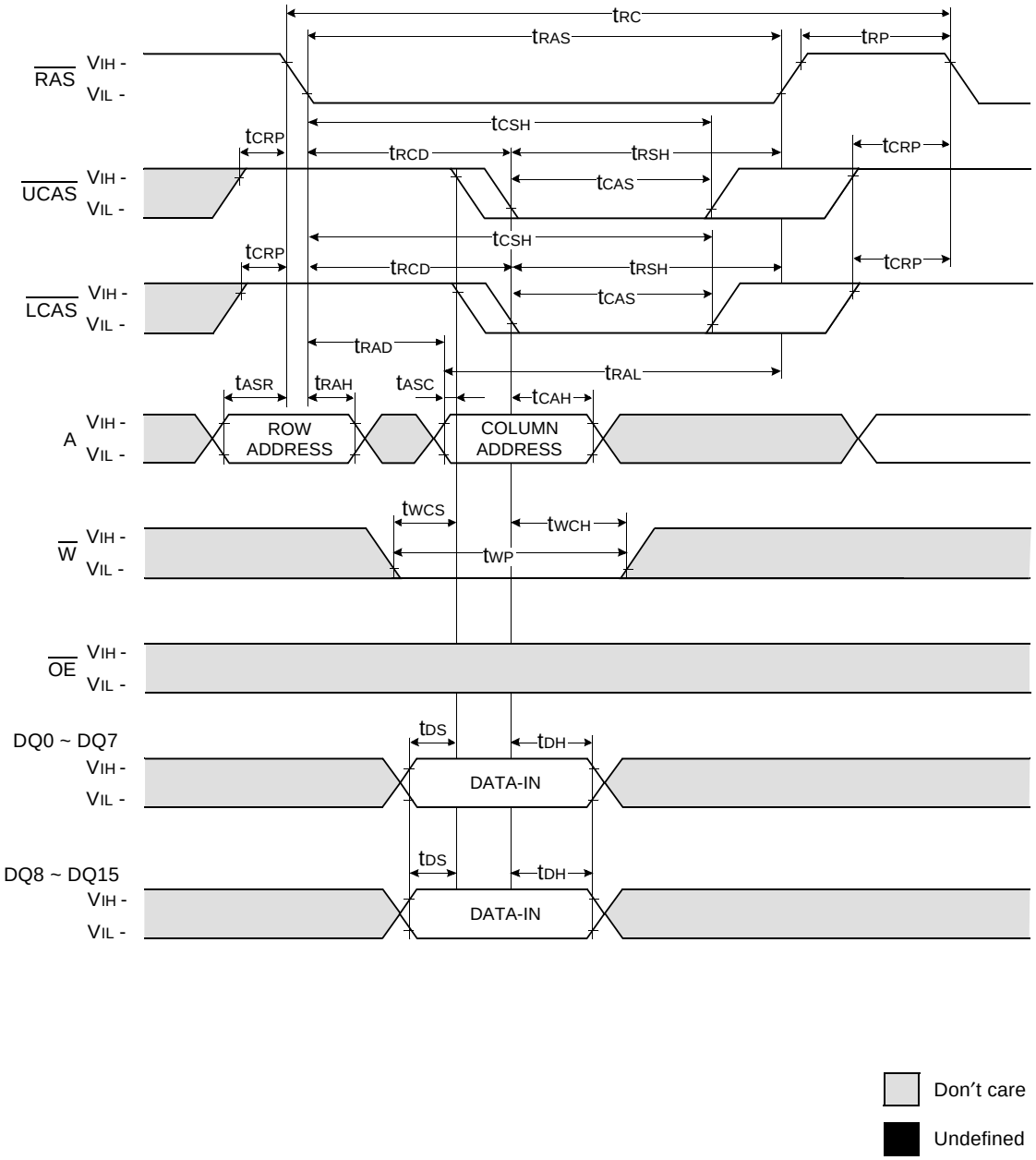
NOTE : DIN = OPEN



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WORD WRITE CYCLE (EARLY WRITE)

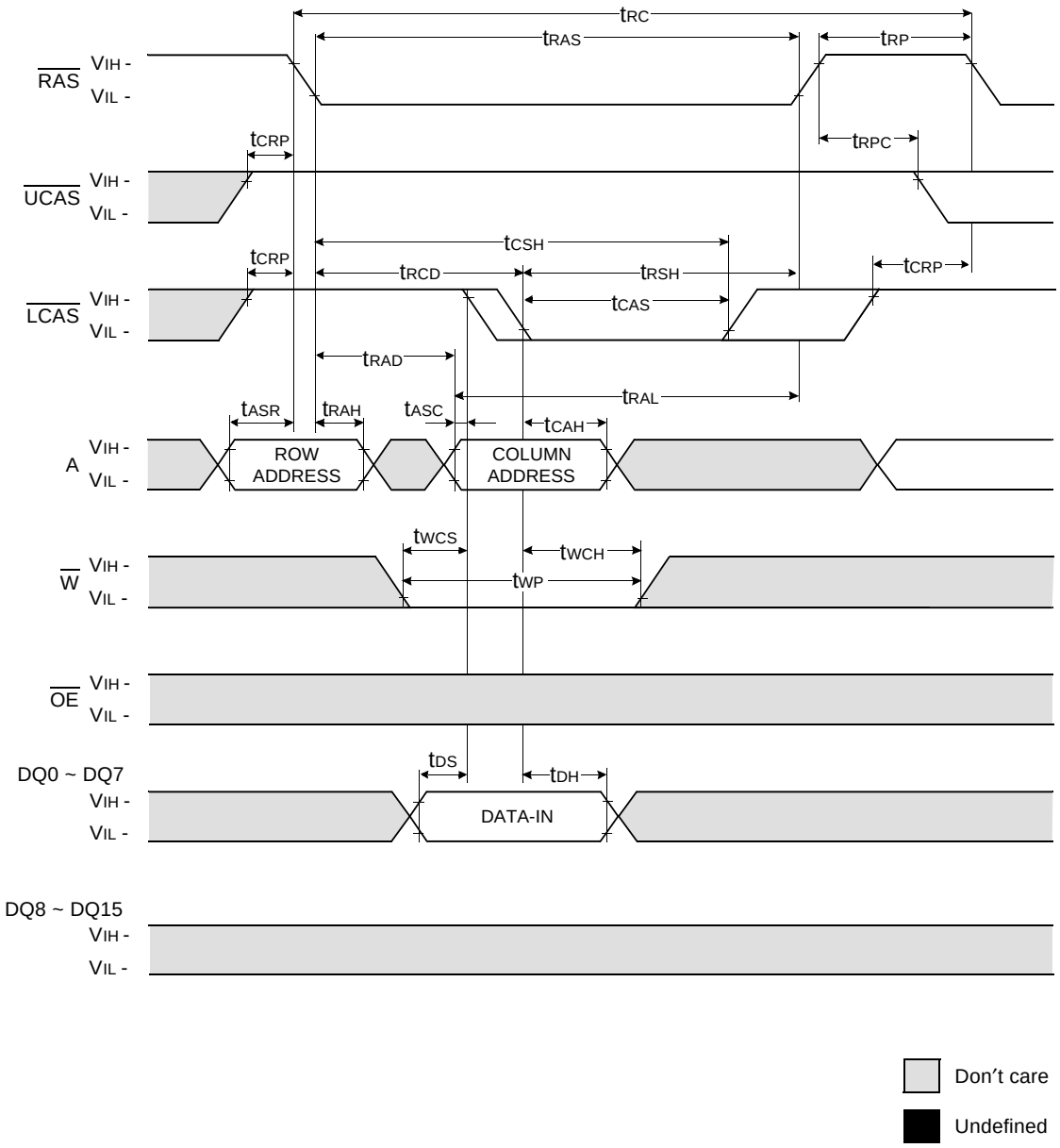
NOTE : DOUT = OPEN



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LOWER BYTE WRITE CYCLE (EARLY WRITE)

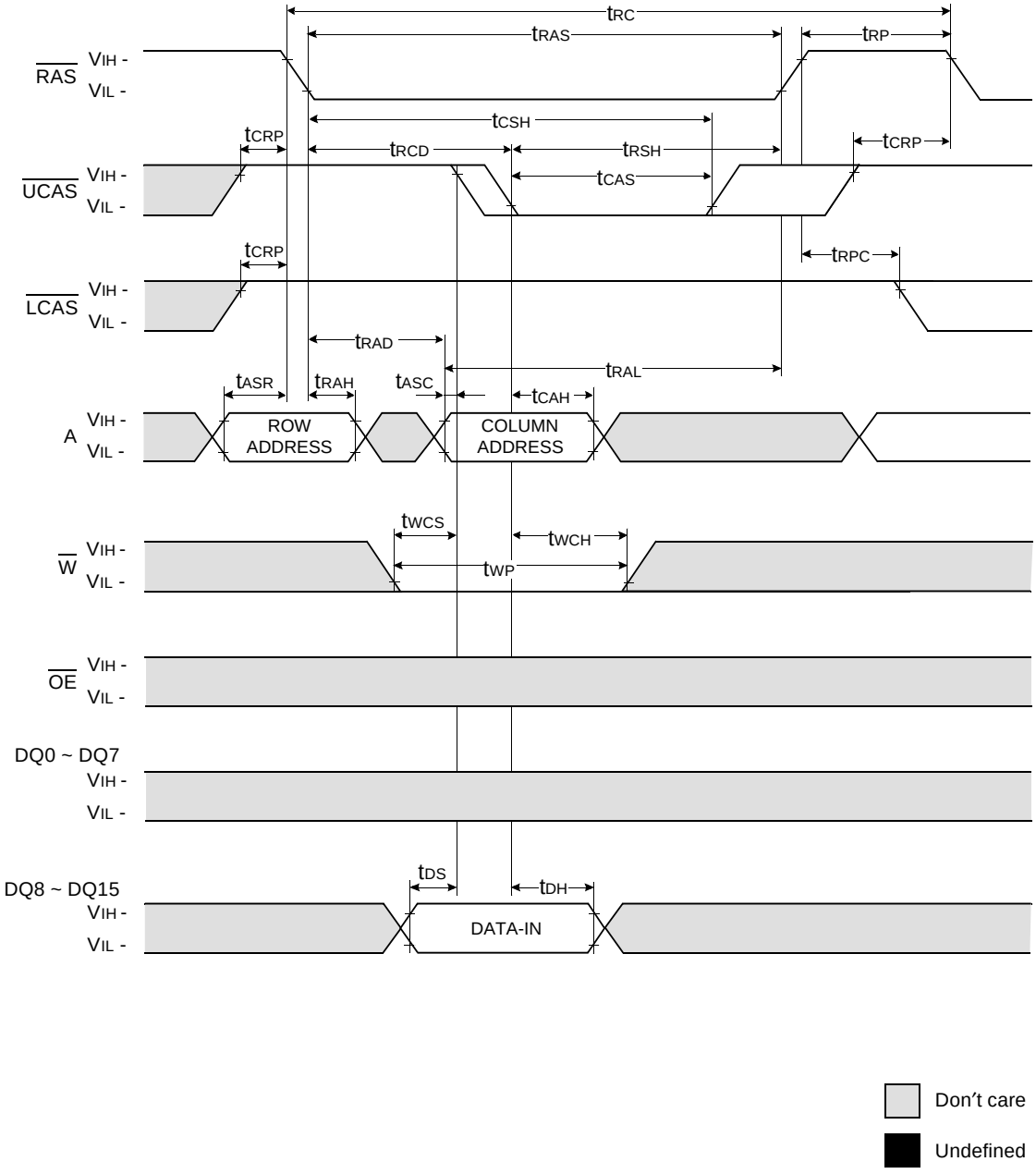
NOTE : DOUT = OPEN



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UPPER BYTE WRITE CYCLE (EARLY WRITE)

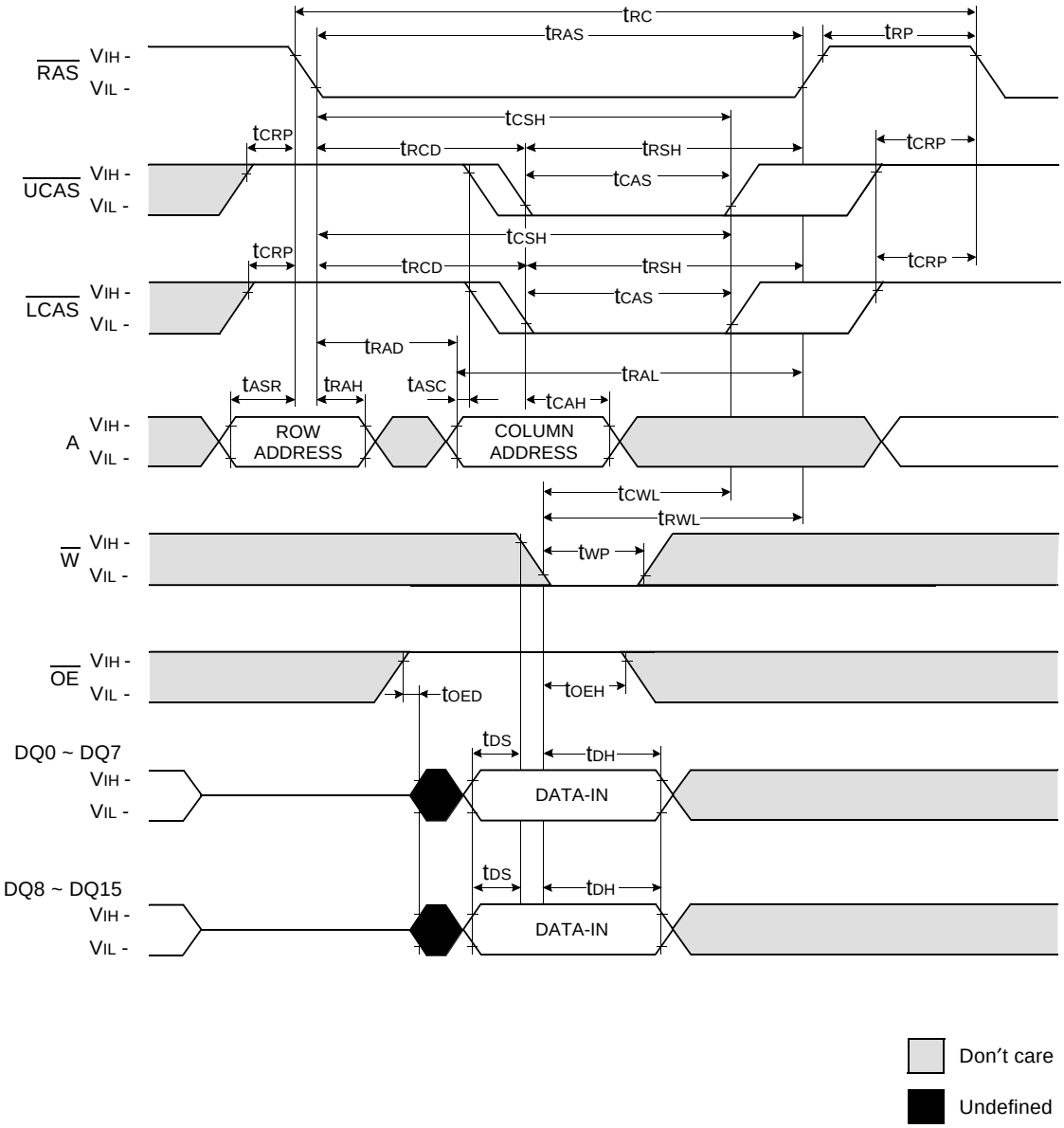
NOTE : DOUT = OPEN



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WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

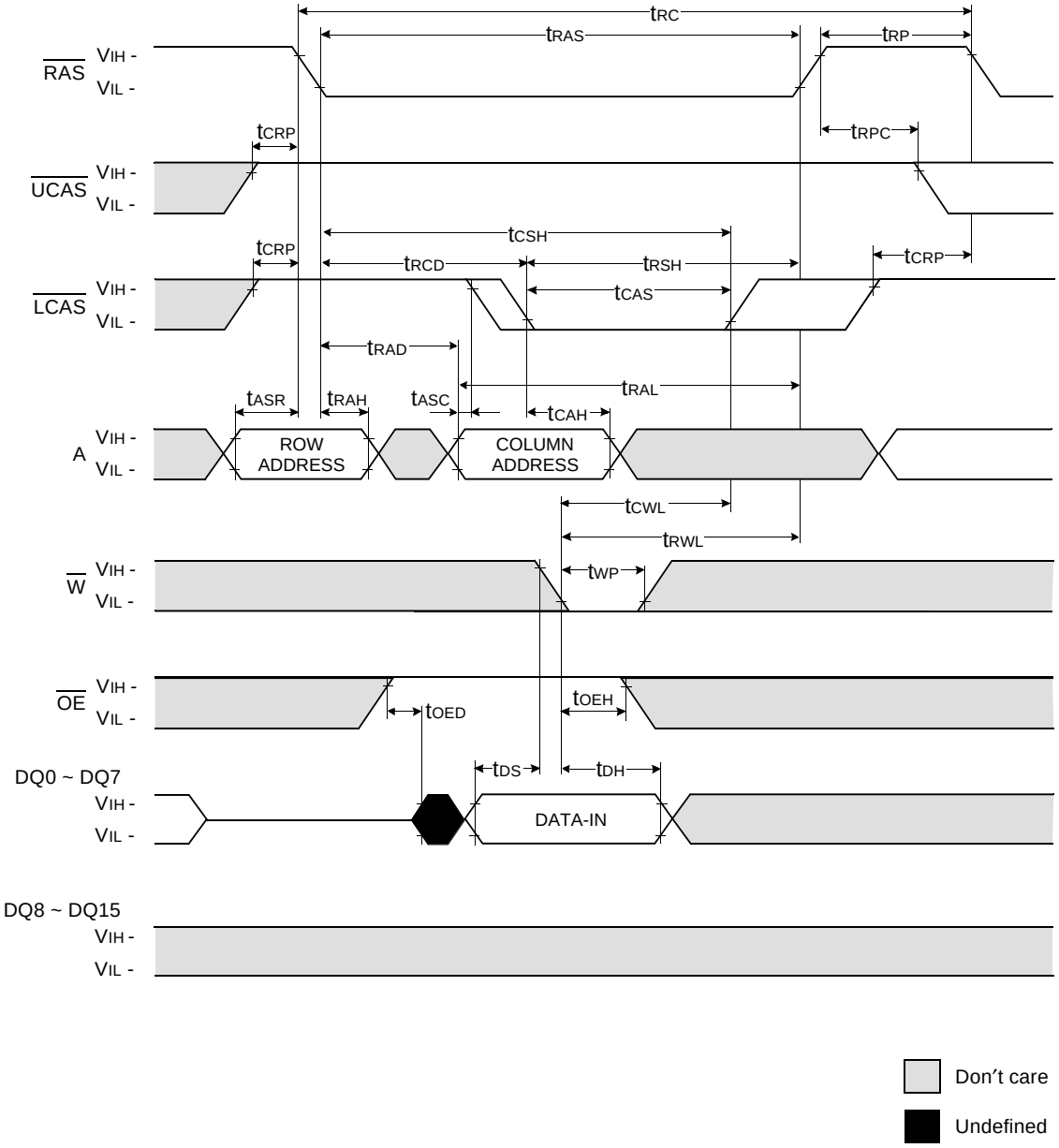
NOTE : DOUT = OPEN



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LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

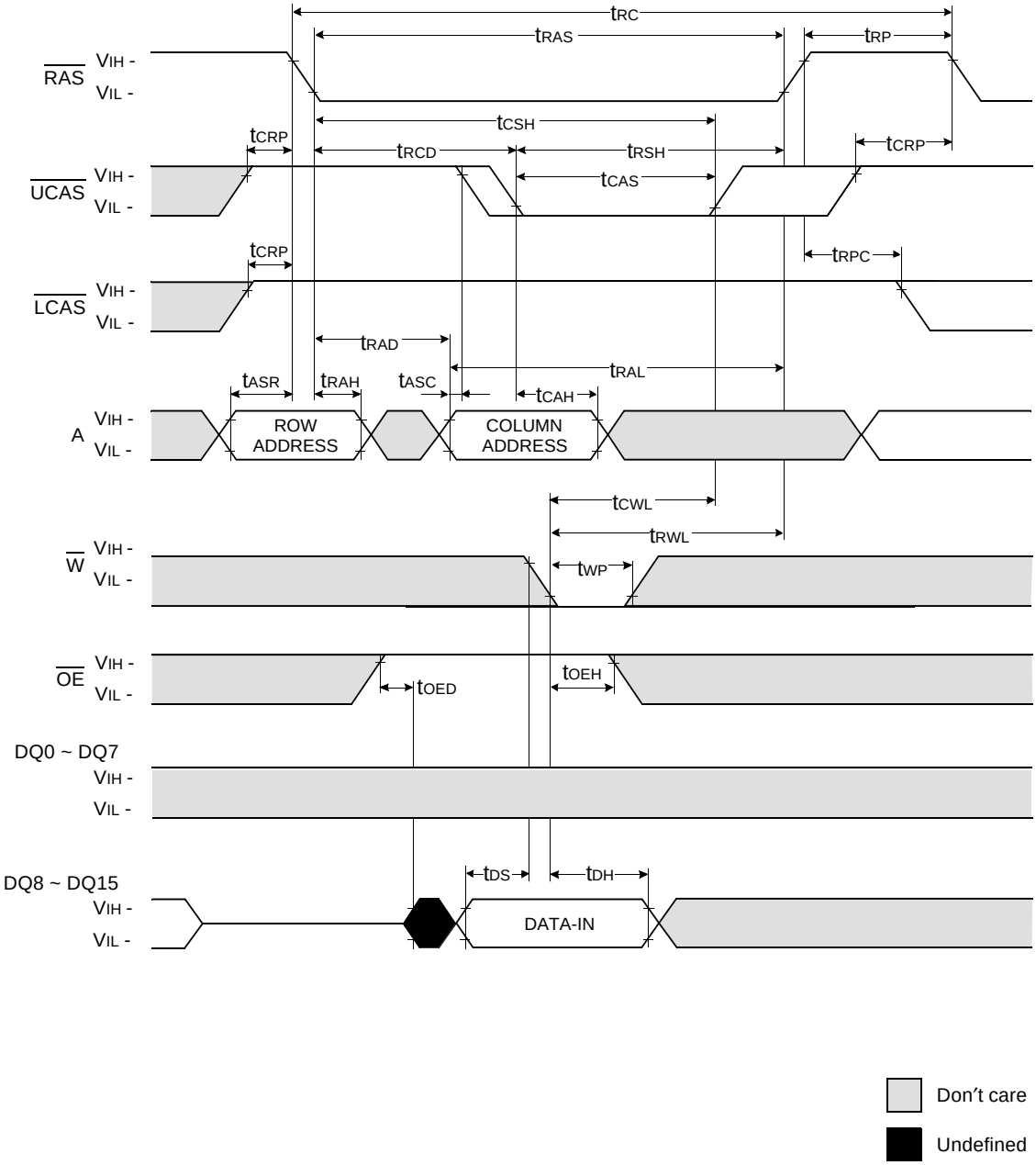
NOTE : DOUT = OPEN



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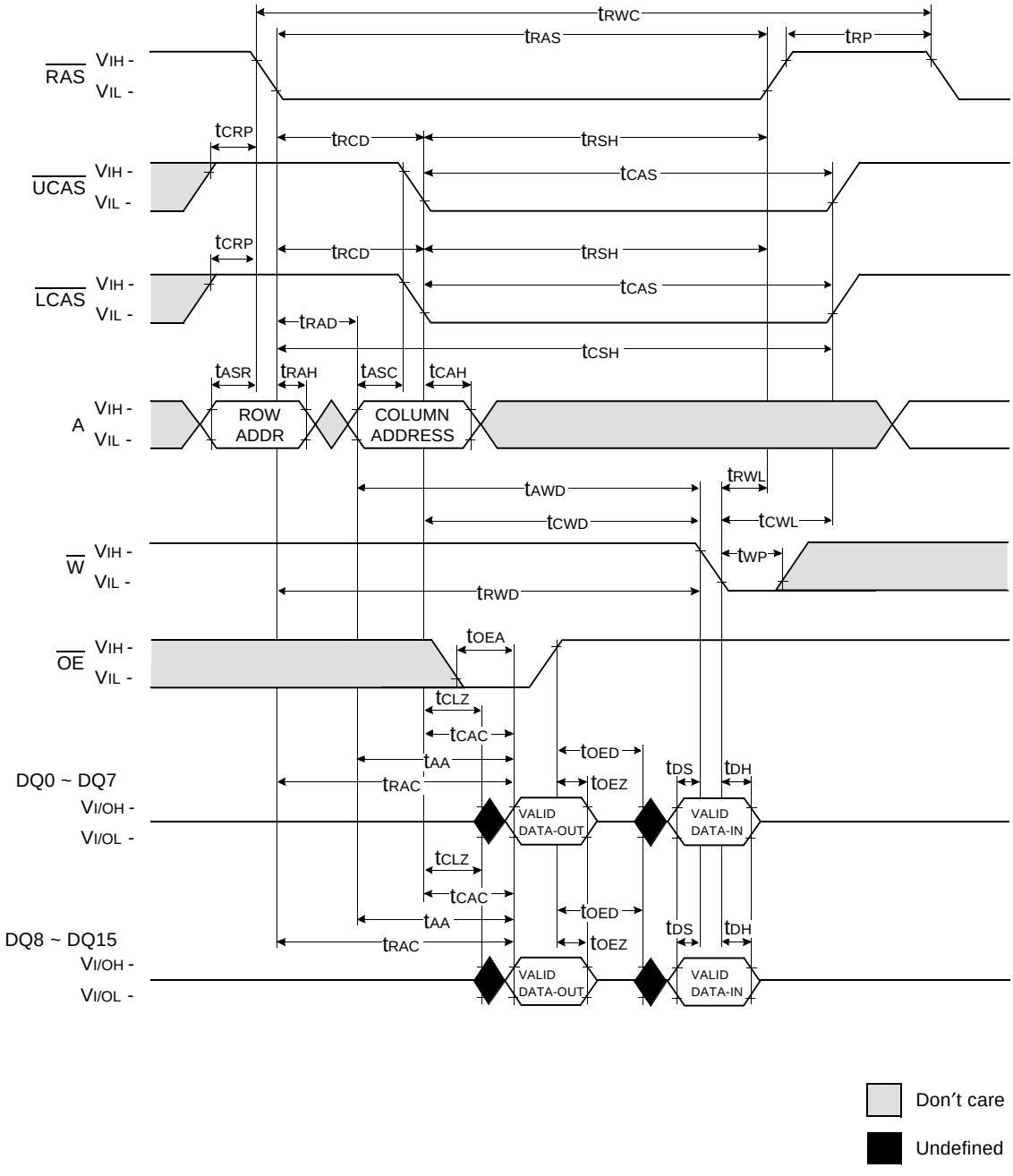
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



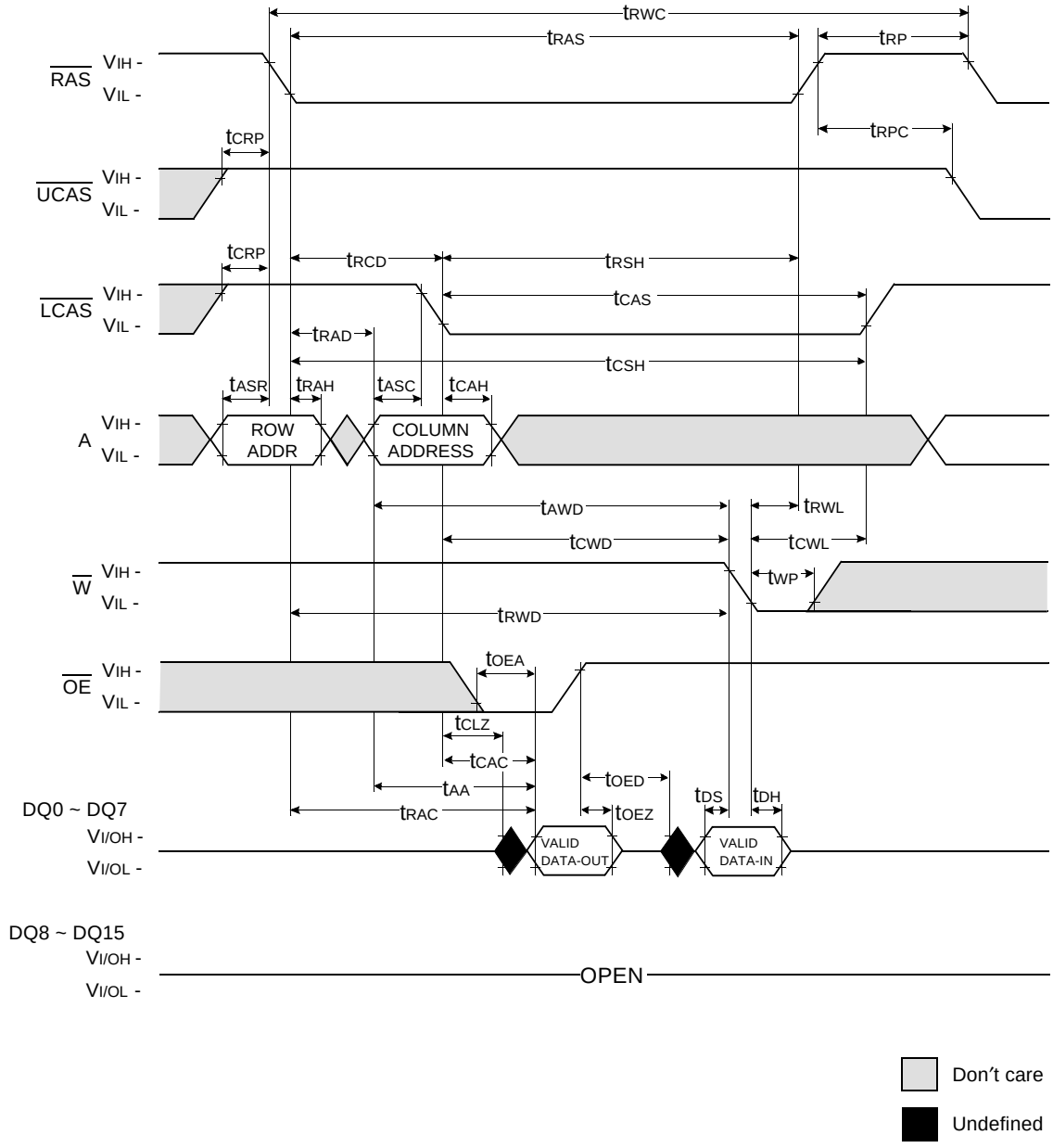
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WORD READ - MODIFY - WRITE CYCLE



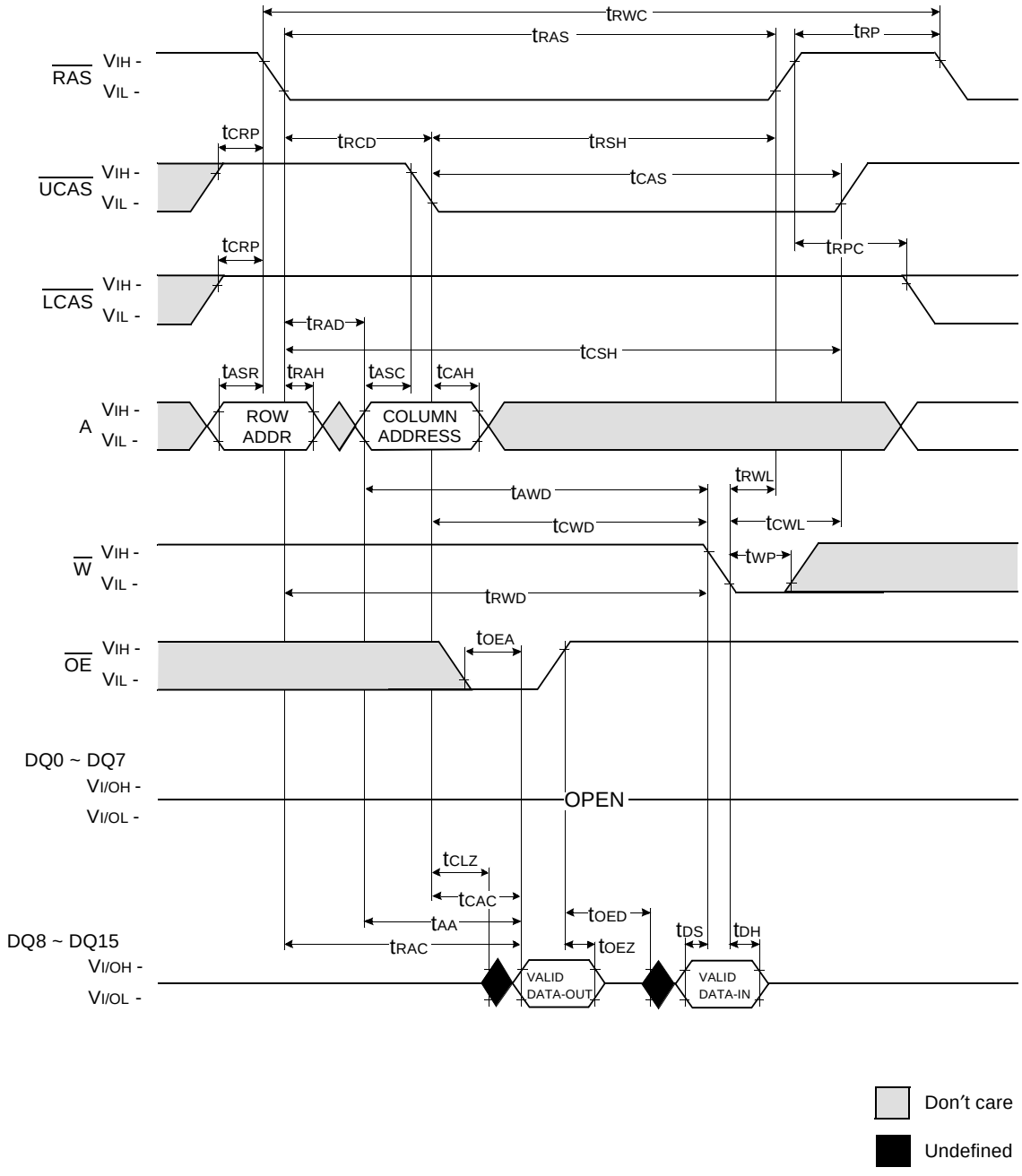
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LOWER-BYTE READ - MODIFY - WRITE CYCLE



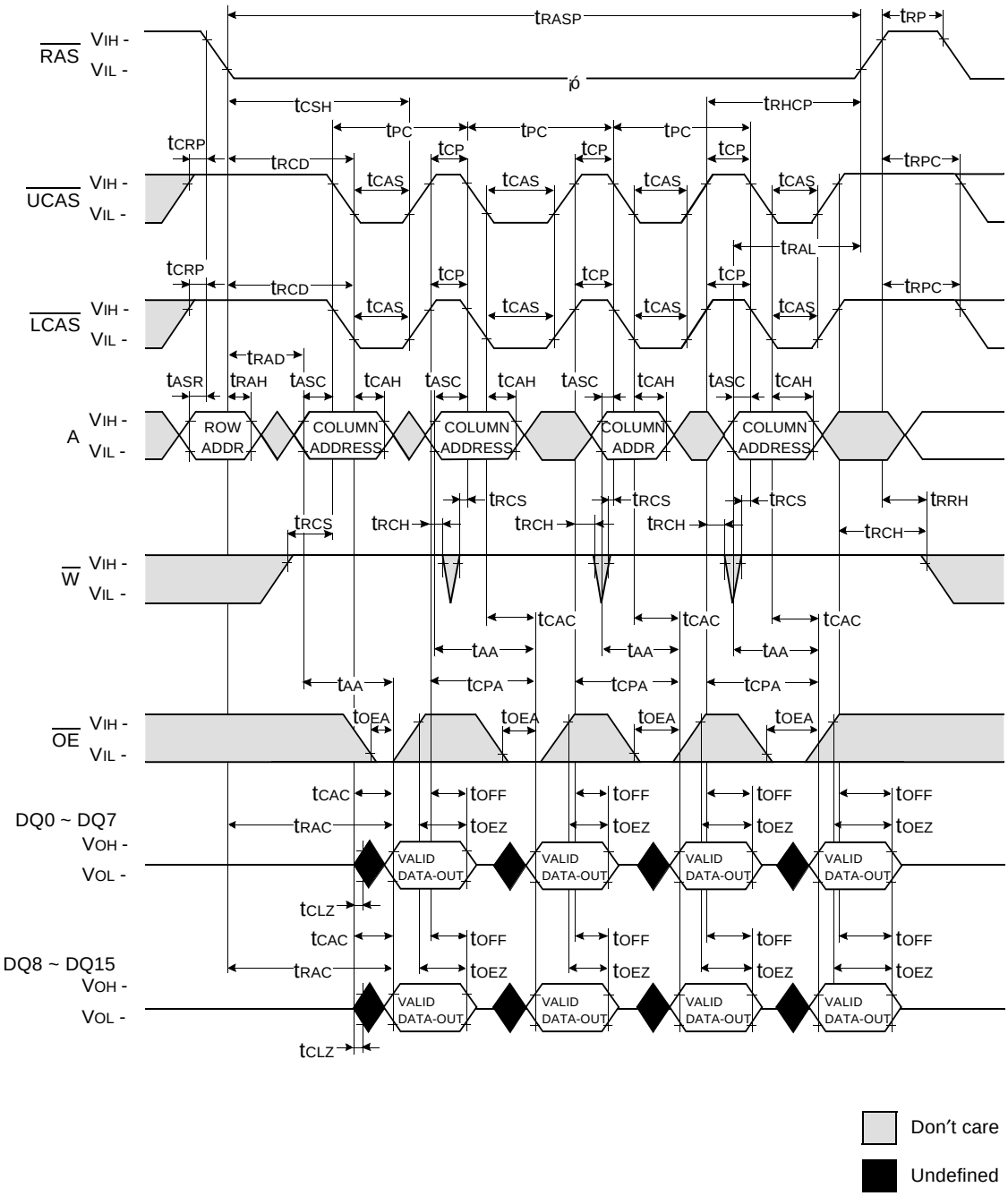
www.BDTIC.com/SAMSUNG

UPPER-BYTE READ - MODIFY - WRITE CYCLE



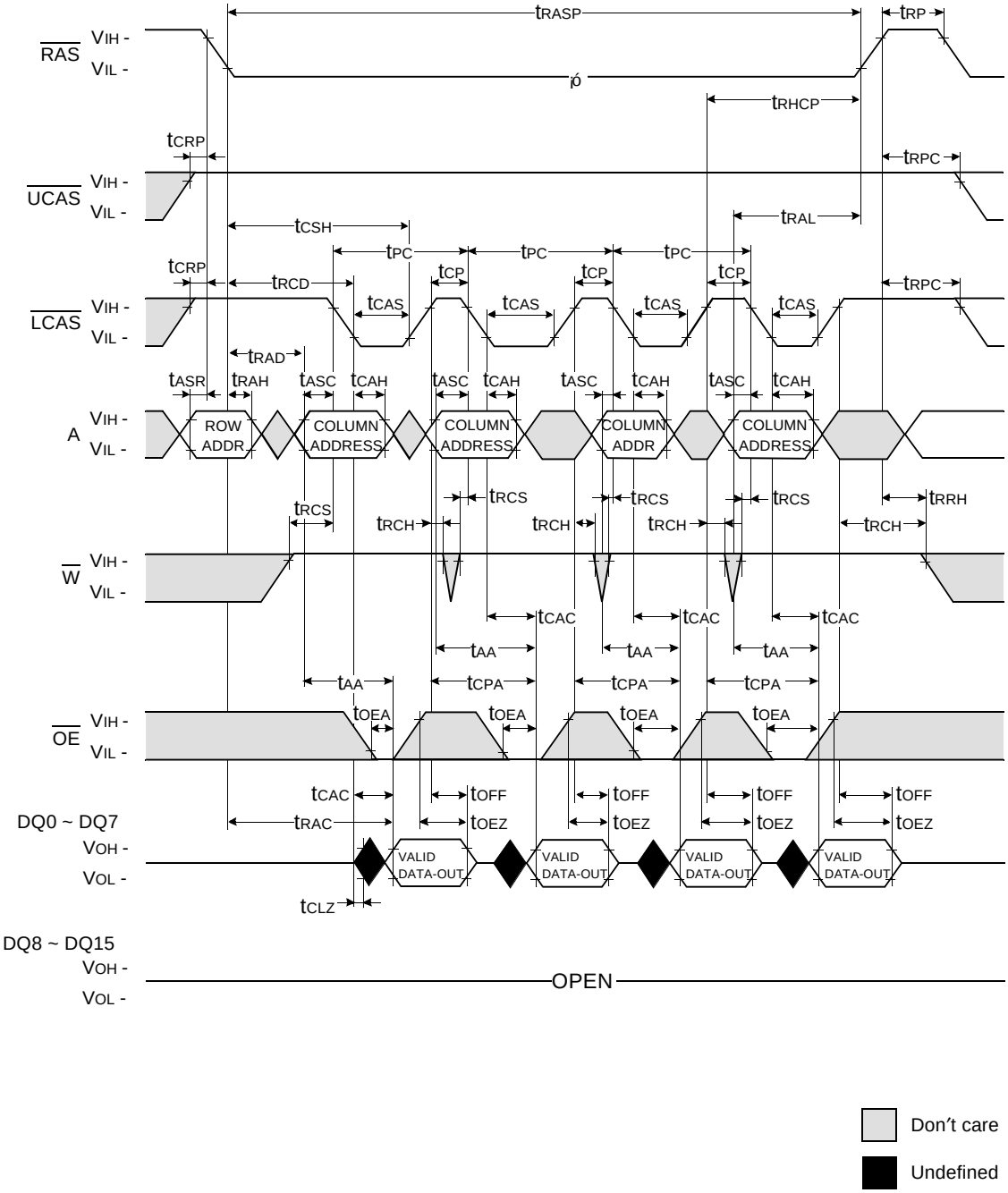
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FAST PAGE MODE WORD READ CYCLE



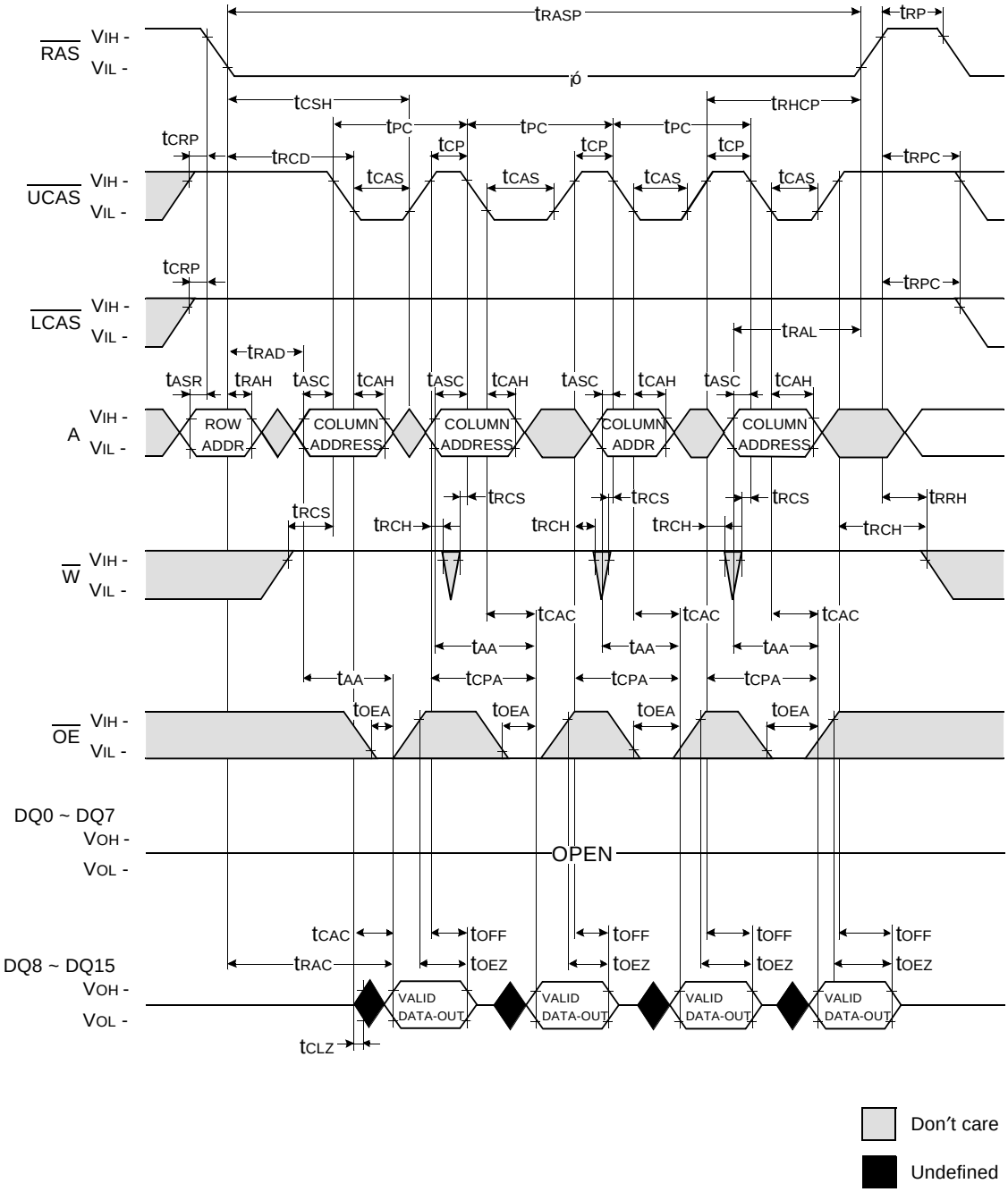
www.BDTIC.com/SAMSUNG

FAST PAGE MODE LOWER BYTE READ CYCLE



www.BDTIC.com/SAMSUNG

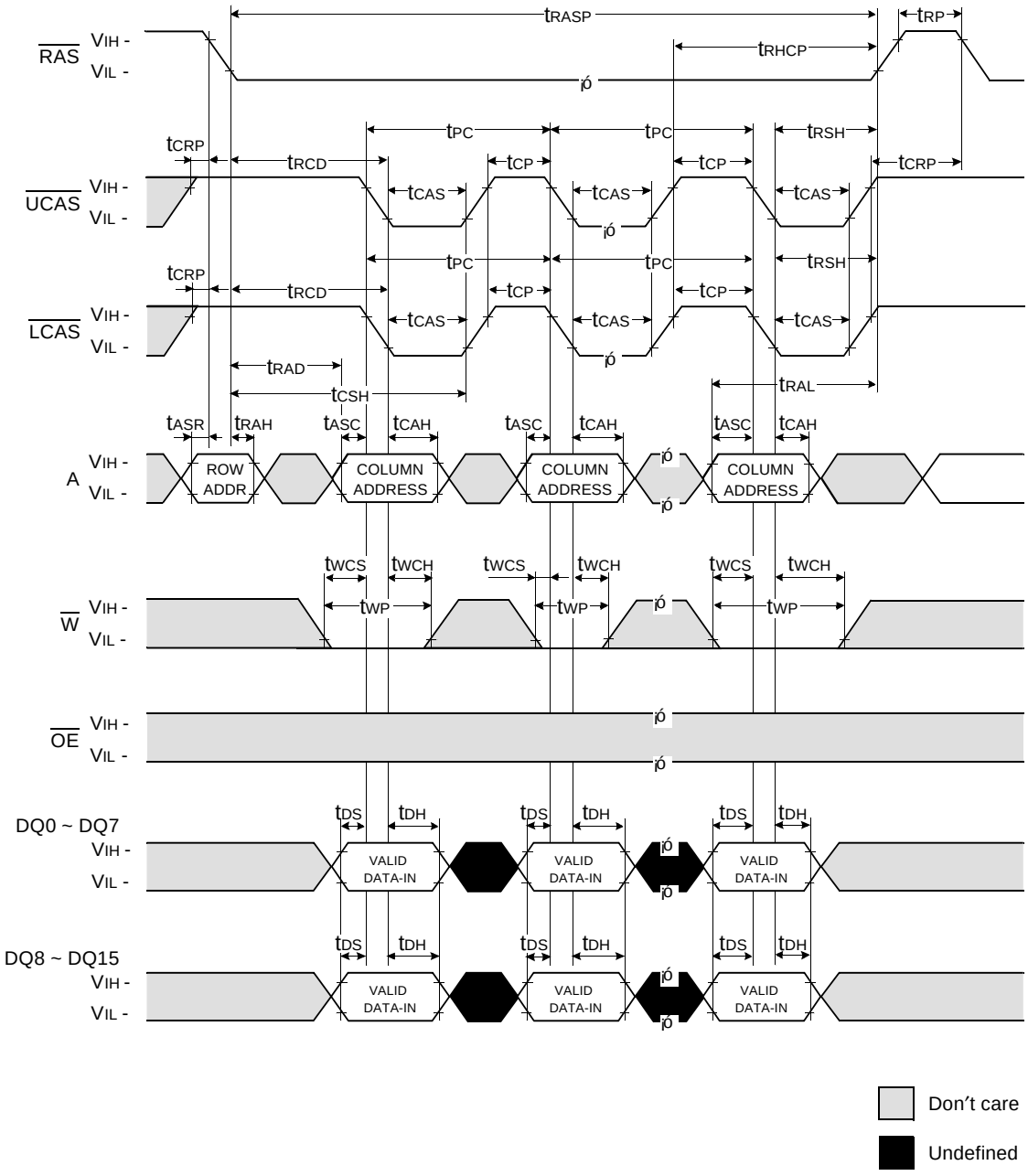
FAST PAGE MODE UPPER BYTE READ CYCLE



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FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

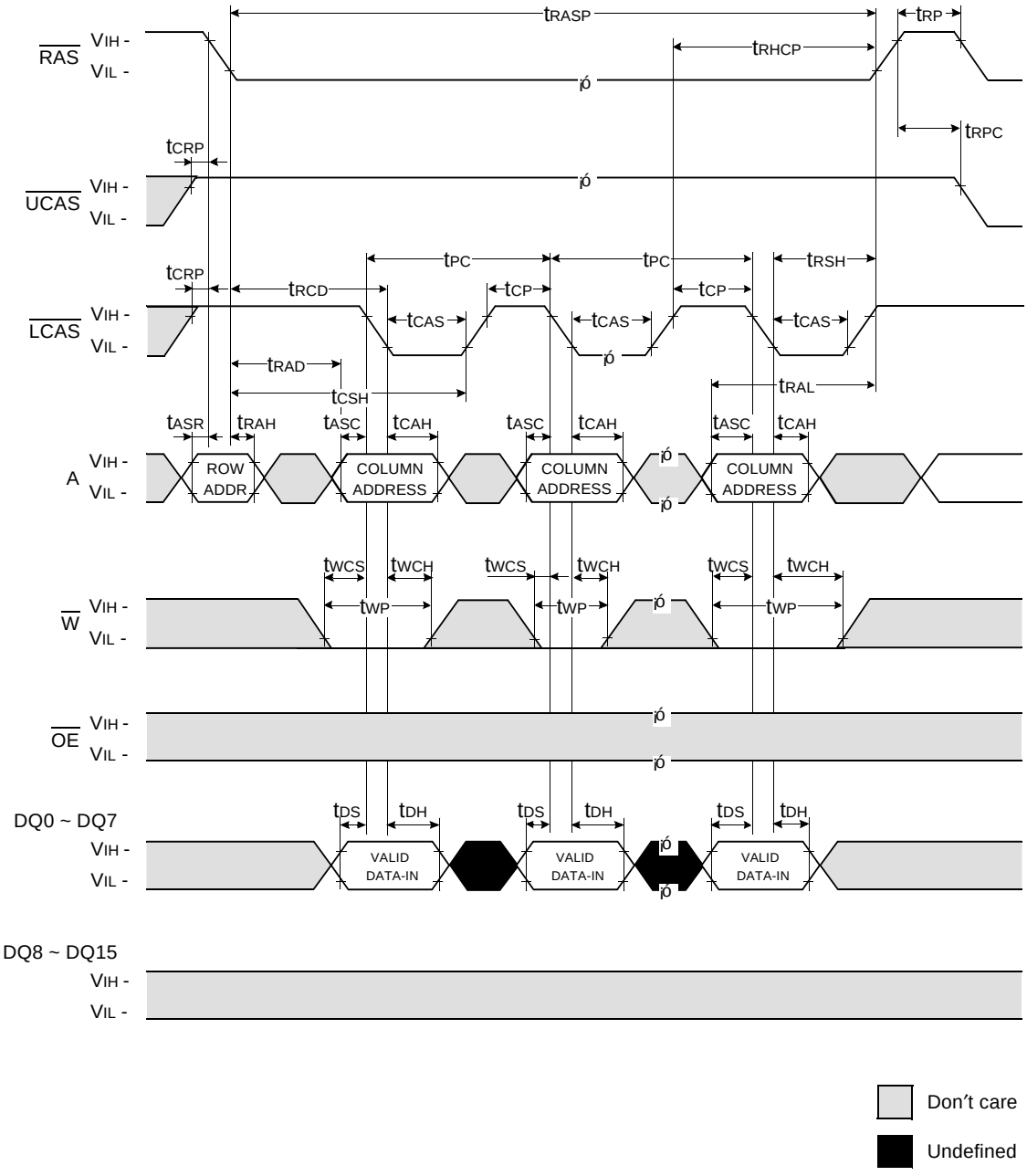
NOTE : DOUT = OPEN



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FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

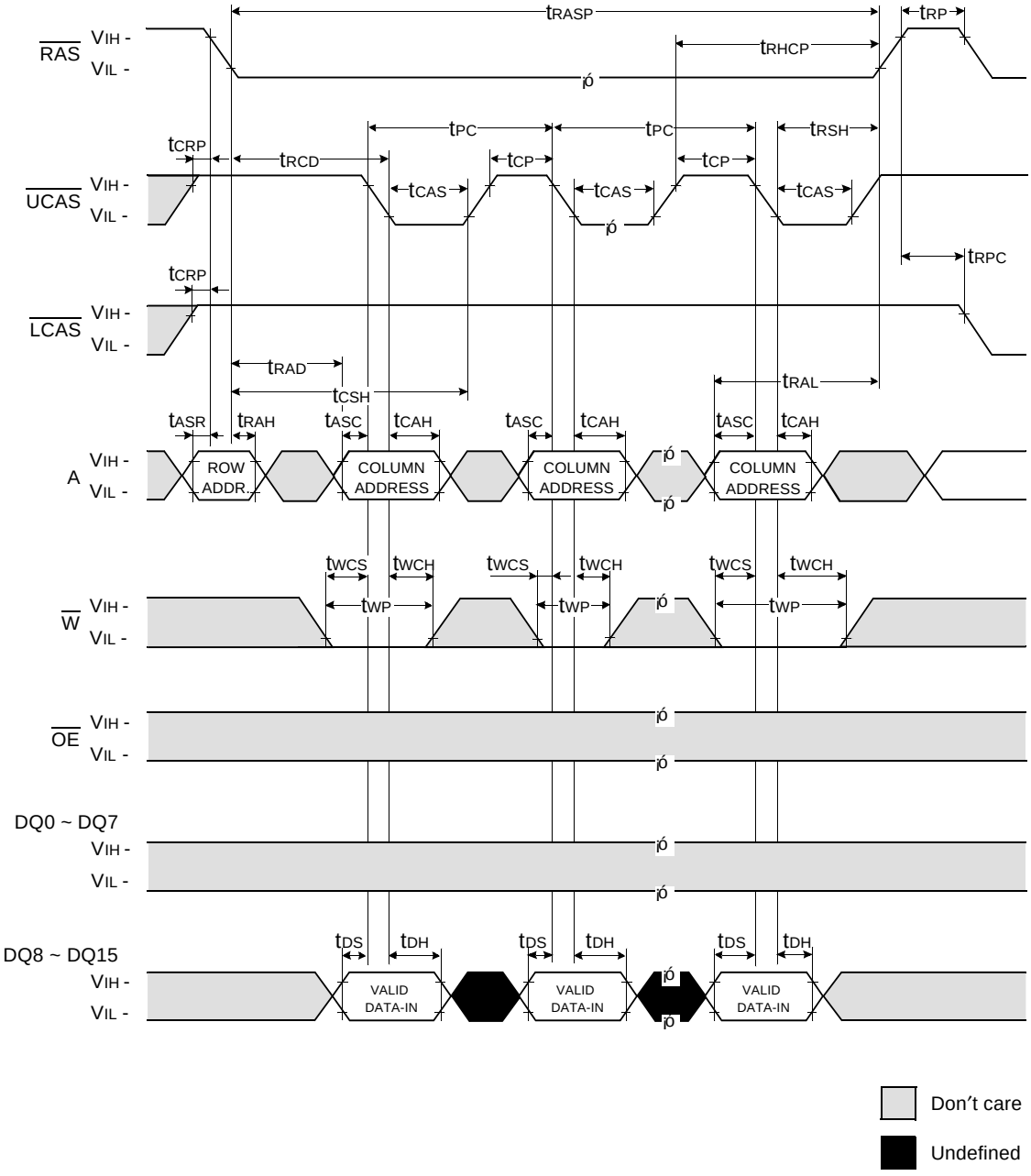
NOTE : DOUT = OPEN



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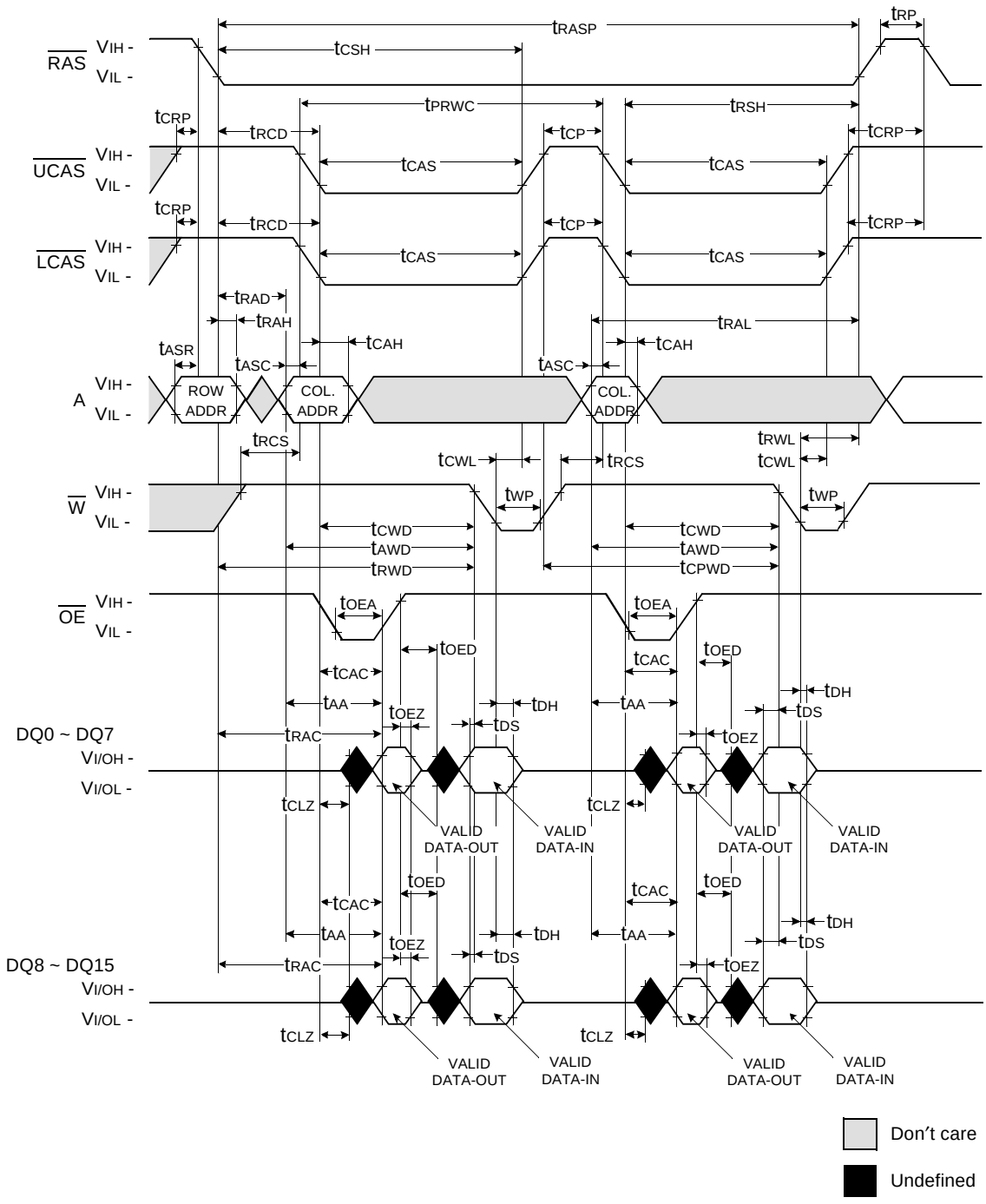
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



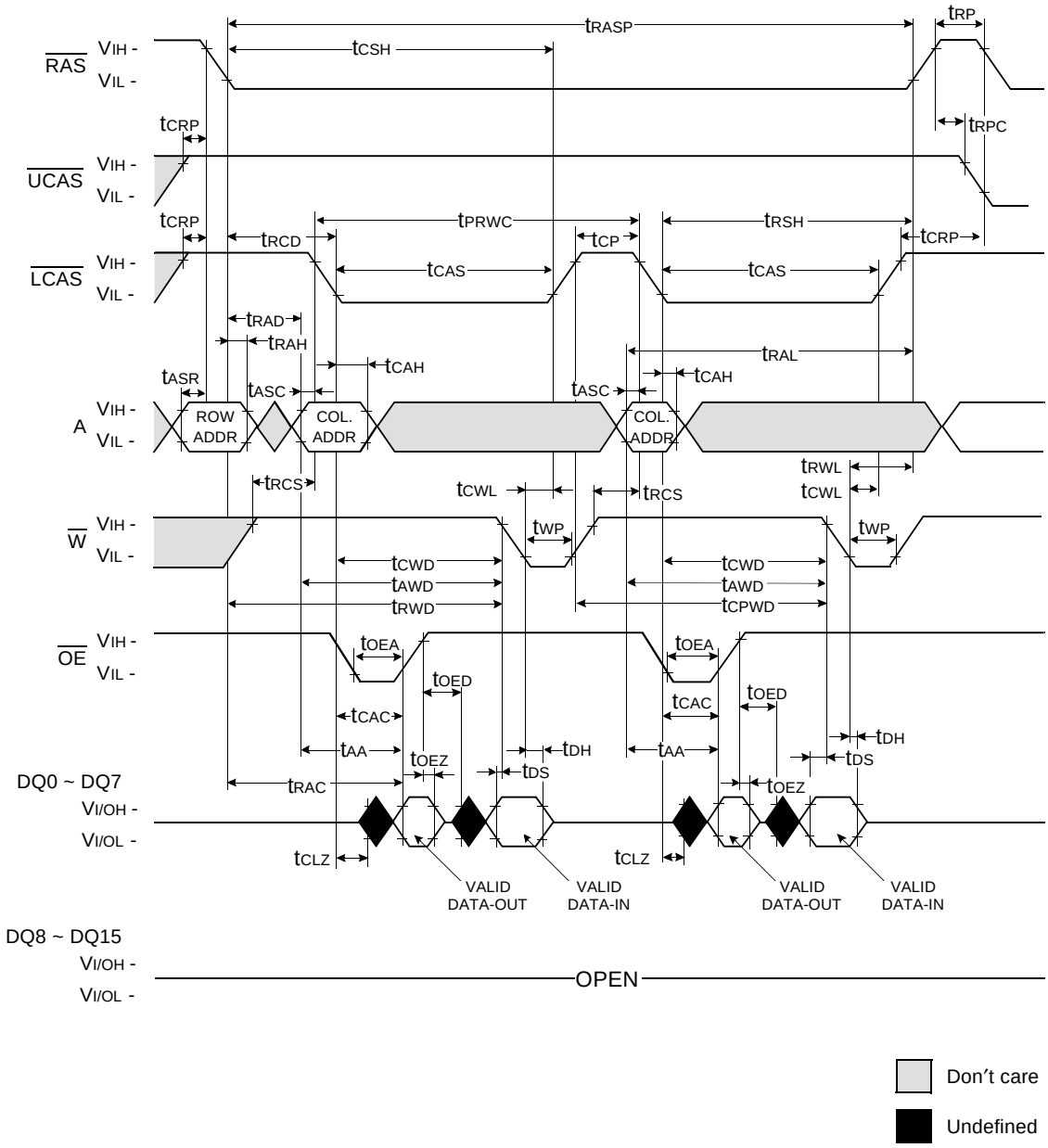
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FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



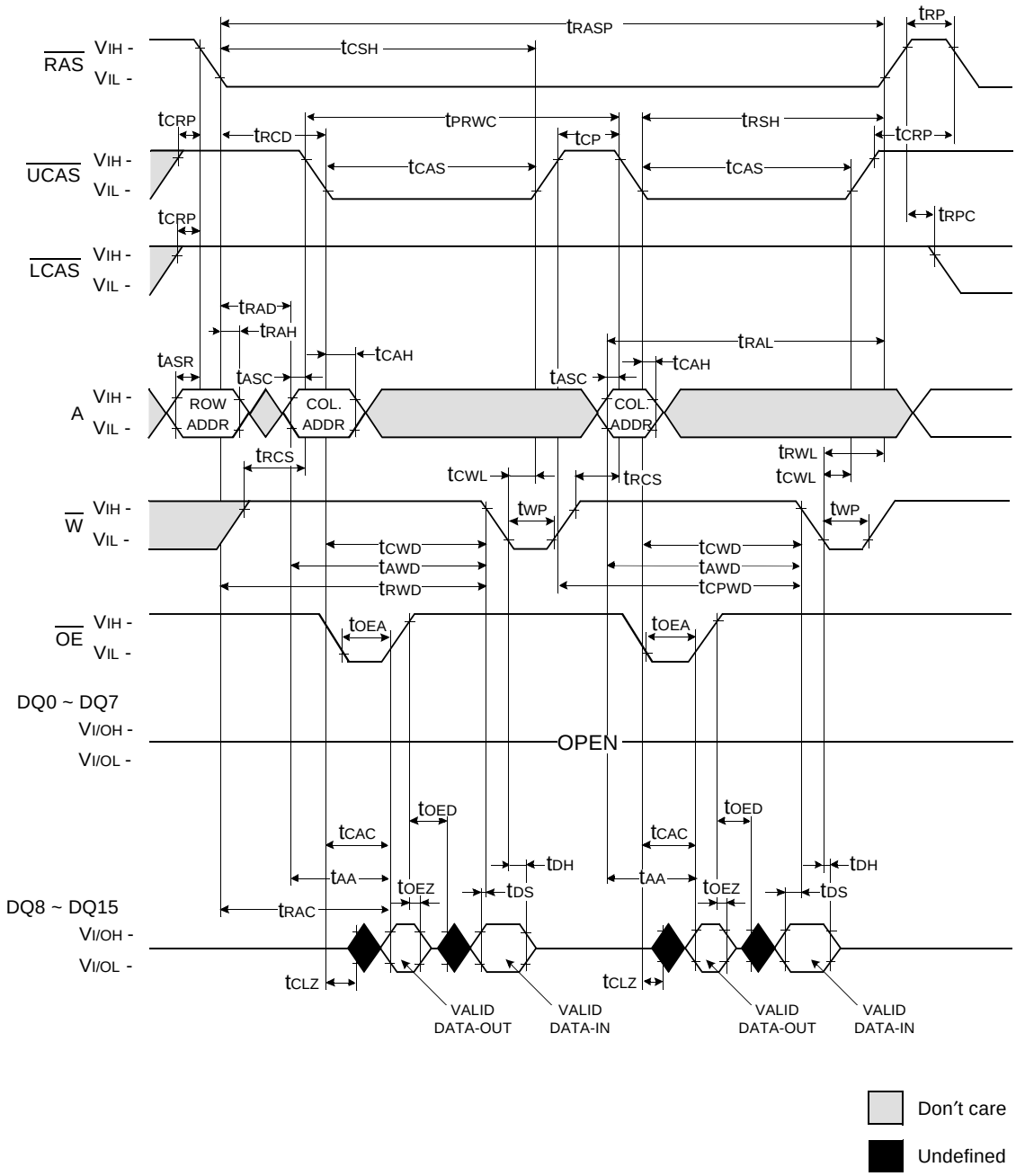
www.BDTIC.com/SAMSUNG

FAST PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE



www.BDTIC.com/SAMSUNG

FAST PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE

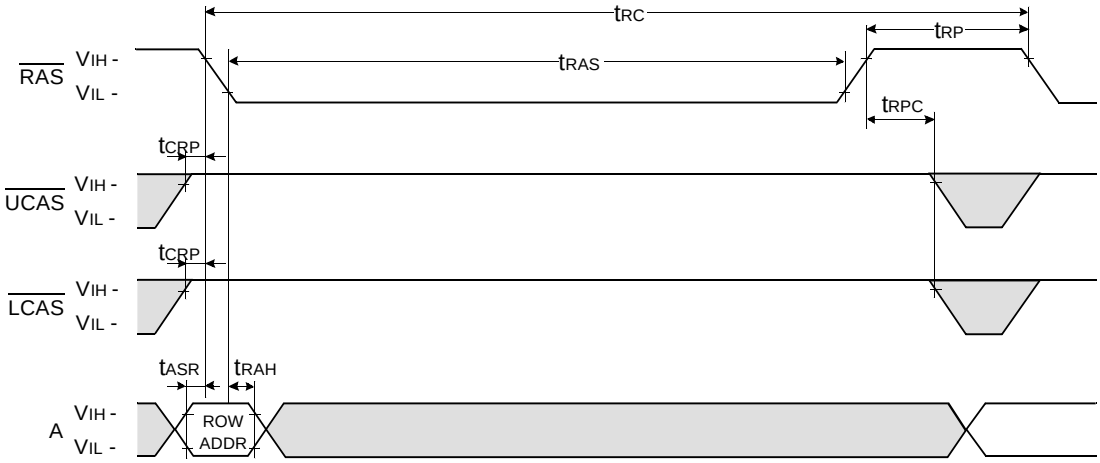


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$\overline{RAS}$ - ONLY REFRESH CYCLE

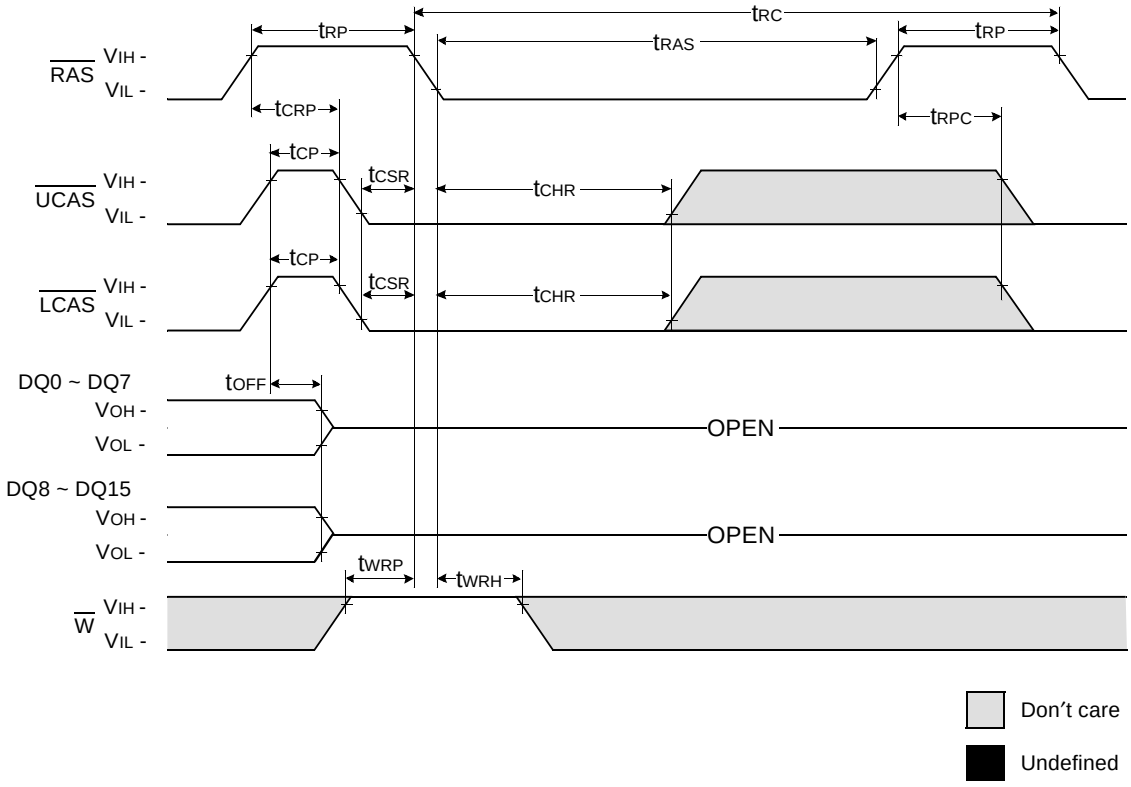
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



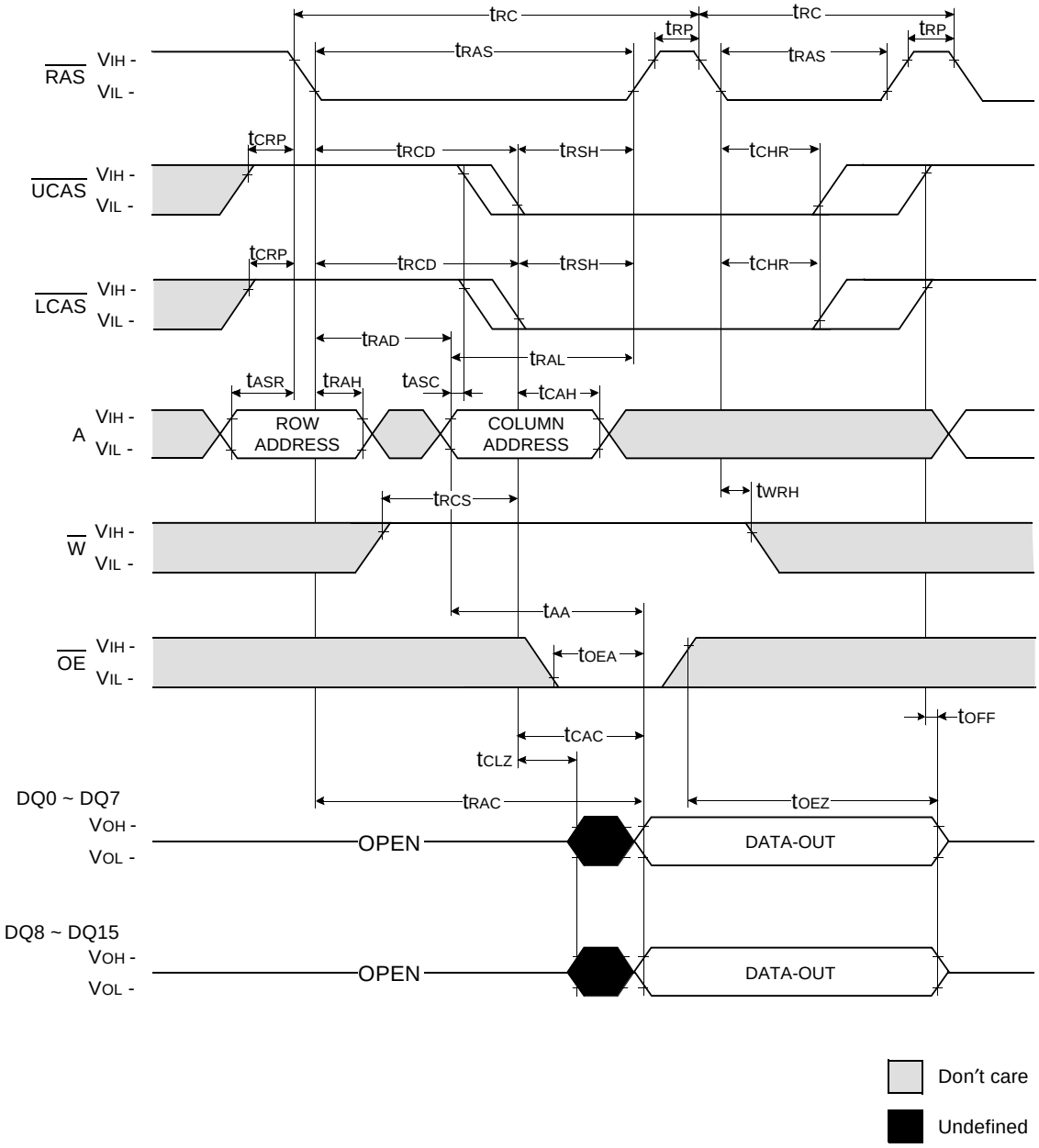
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



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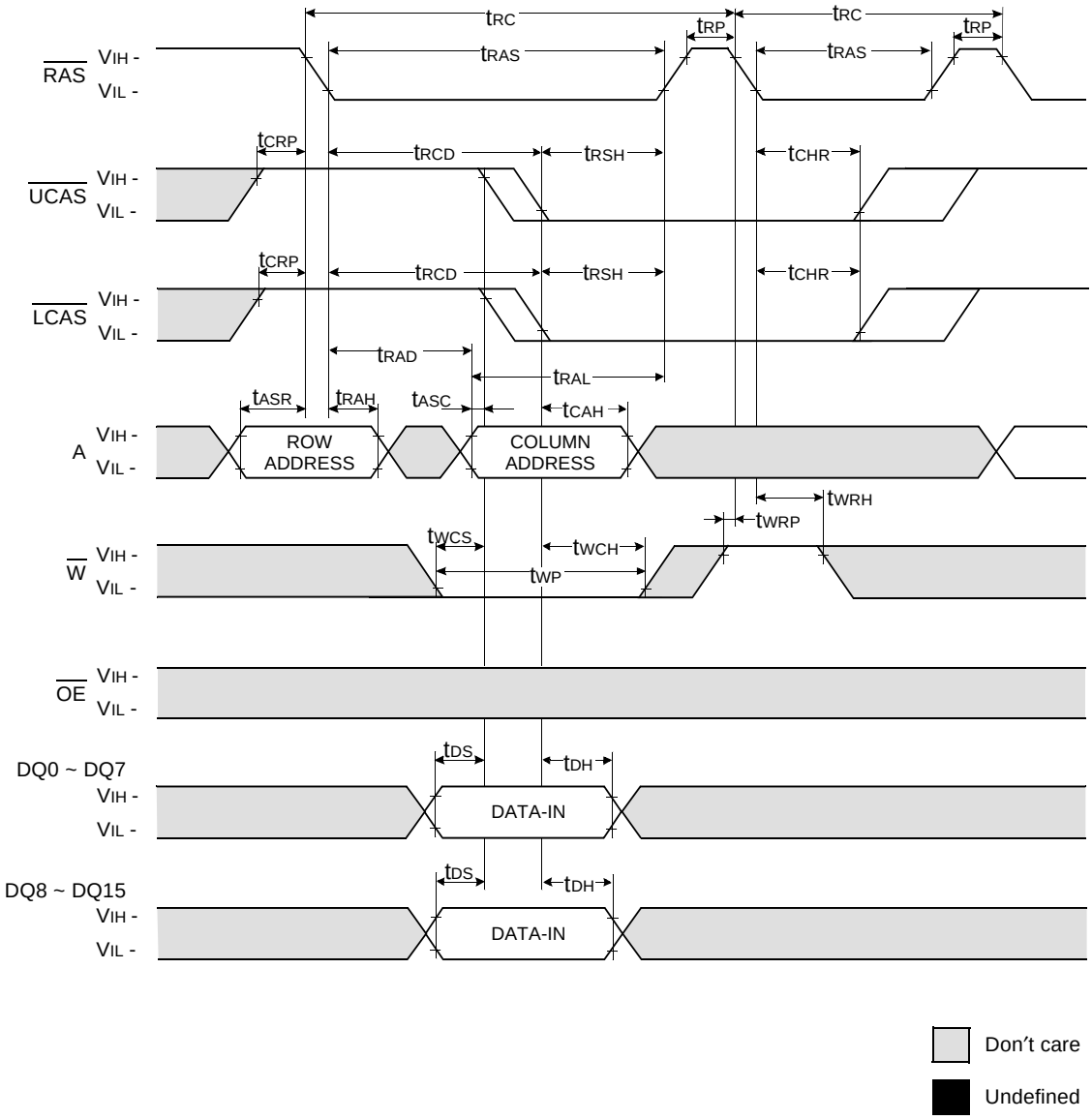
HIDDEN REFRESH CYCLE (READ)



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HIDDEN REFRESH CYCLE (WRITE)

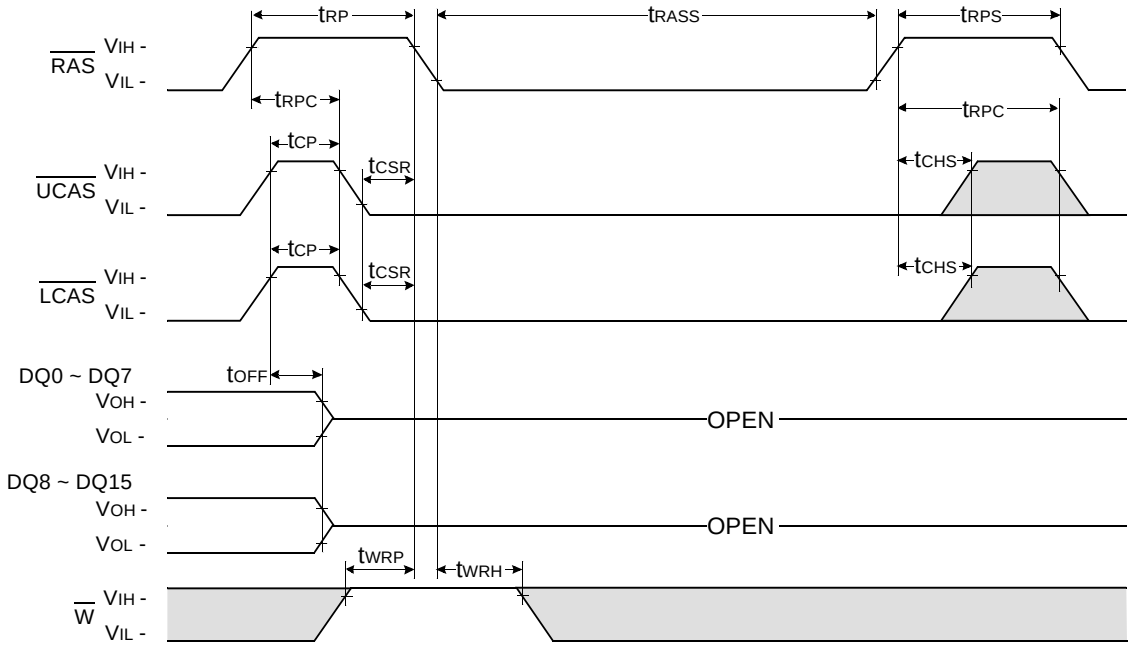
NOTE : DOUT = OPEN



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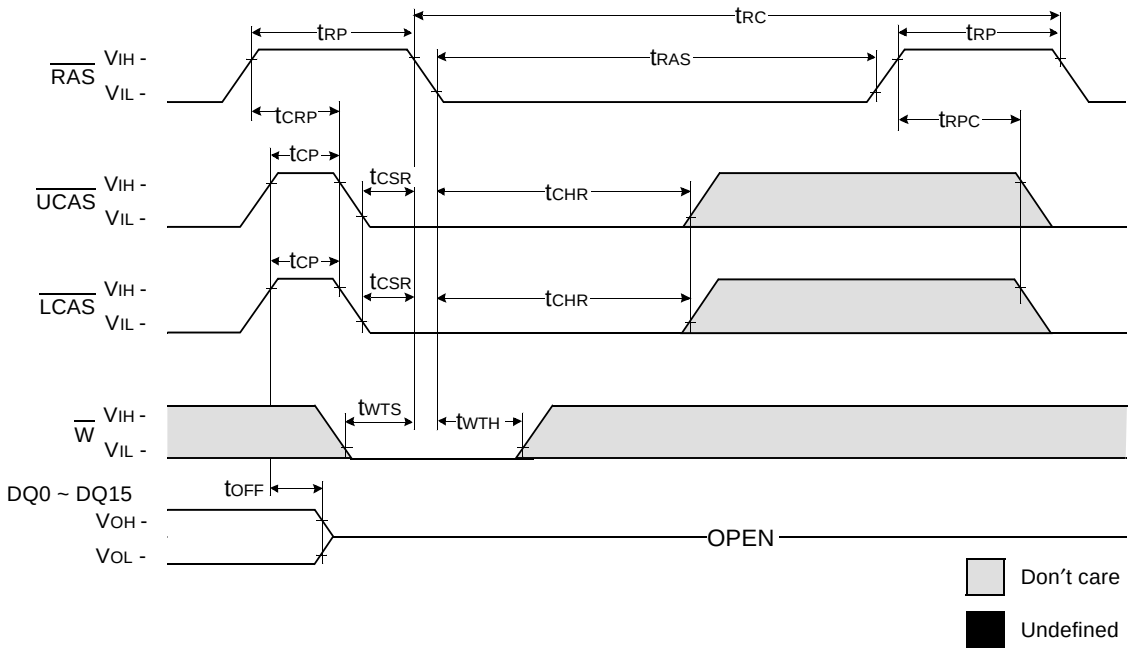
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

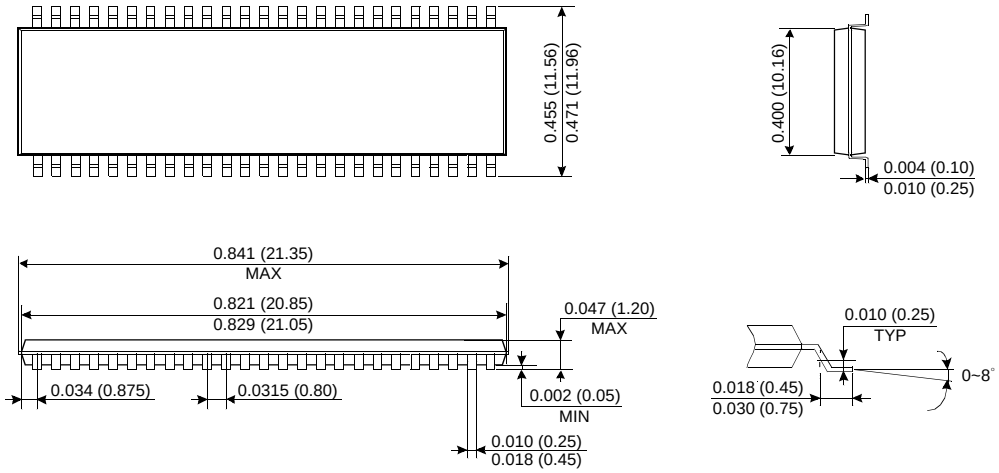


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PACKAGE DIMENSION

50 TSOP(II) 400mil

Units : Inches (millimeters)



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