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4Byte 8Mx32 SIMM

(4Mx16 base)

Revision 0.0

June 1999

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Revision History

Version 0.0 (June 1999)

• The 4th. generation of 64Mb DRAM components are applied for this module.

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M53230804CY0/CT0-C EDO Mode

8M x 32 DRAM SIMM Using 4Mx16, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M53230804CY0/CT0-C is a 8Mx32bits Dynamic RAM high density memory module. The Samsung M53230804CY0/CT0-C consists of four CMOS 4Mx16bits DRAMs in TSOP packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M53230804CY0/CT0-C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-C50	50ns	13ns	84ns	20ns
-C60	60ns	15ns	104ns	25ns

FEATURES

- Part Identification
  - M53230804CY0-C(4K cycles/64ms Ref, TSOP, Solder)
  - M53230804CT0-C(4K cycles/64ms Ref, TSOP, Gold)
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ & Hidden Refresh capability
- $\overline{RAS}$-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ18	39	$\overline{Vss}$
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	RAS1
10	Vcc	46	$\overline{NC}$
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{A9}$	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs
DQ0-7, DQ9-16 DQ18-25, DQ27-34	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

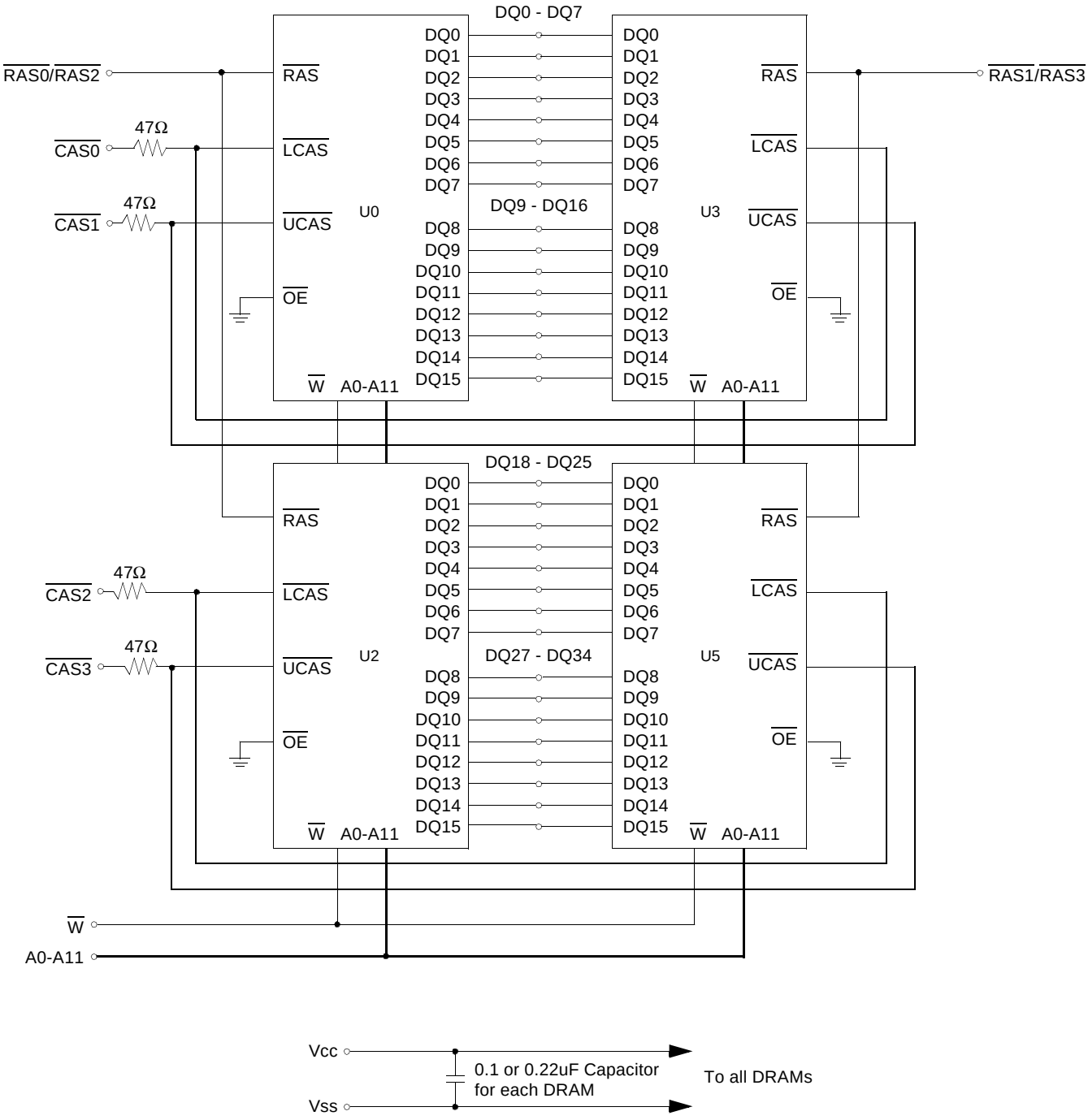
PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

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FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230804CY0/CT0		Unit
		Min	Max	
I_{CC1}	-50 -60	- -	244 224	mA mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-50 -60	- -	244 224	mA mA
I_{CC4}	-50 -60	- -	224 204	mA mA
I_{CC5}	Don't care	-	4	mA
I_{CC6}	-50 -60	- -	244 224	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} :Hyper Page Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

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CAPACITANCE (T_A = 25°C, V_{CC}=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W}$]	C_{IN2}	-	38	pF
Input capacitance[$\overline{RAS0}$/$\overline{RAS2}$, $\overline{RAS1}$/$\overline{RAS3}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.6/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,10
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,10
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		45		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	4
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	37	20	45	ns	9
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	0		0		ns	9
Data hold time	t_{DH}	8		10		ns	9
Refresh period	t_{REF}		64		64	ms	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3

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AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.6/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Hyper page mode cycle time	t_{HPC}	20		25		ns	11
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are Vih/Vil. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.

5. Assumes that tRCD≥tRCD(max).

6. This parameter defines the time at which the output achieves the open circuit and is not referenced for VOH or VOL.

7. tWCS is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either tRCH or tRRH must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

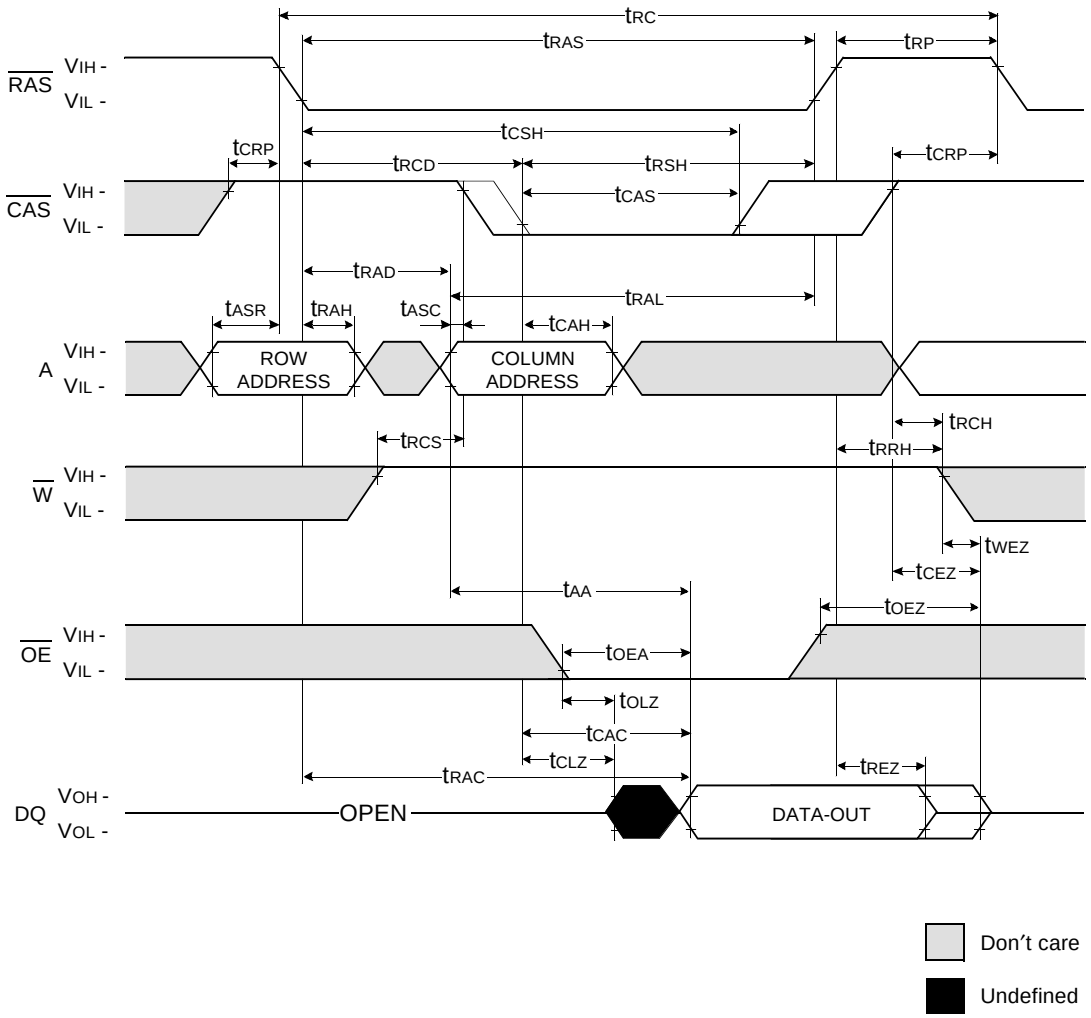
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit access time is controlled by tAA.

11. tASC≥6ns, Assume tT=2.0ns.

12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

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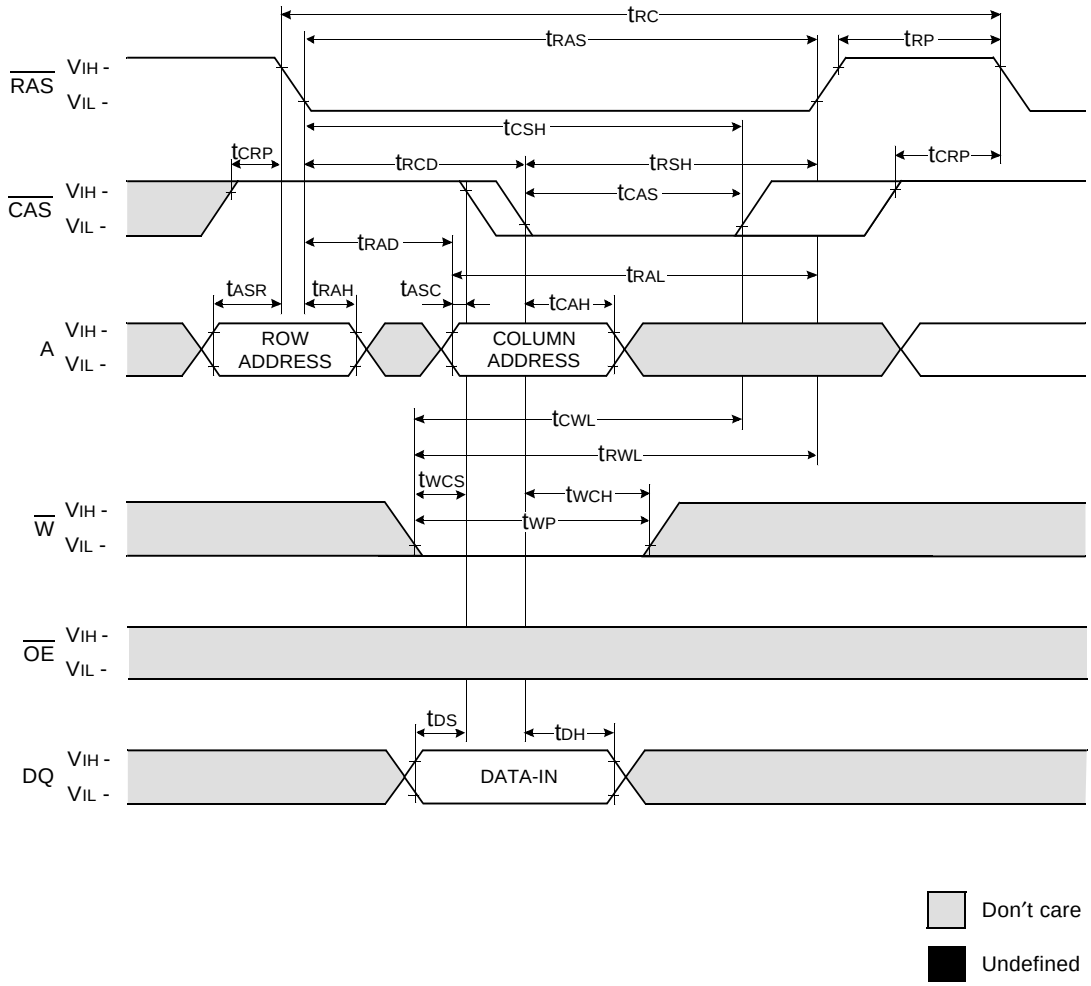
READ CYCLE



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WRITE CYCLE (EARLY WRITE)

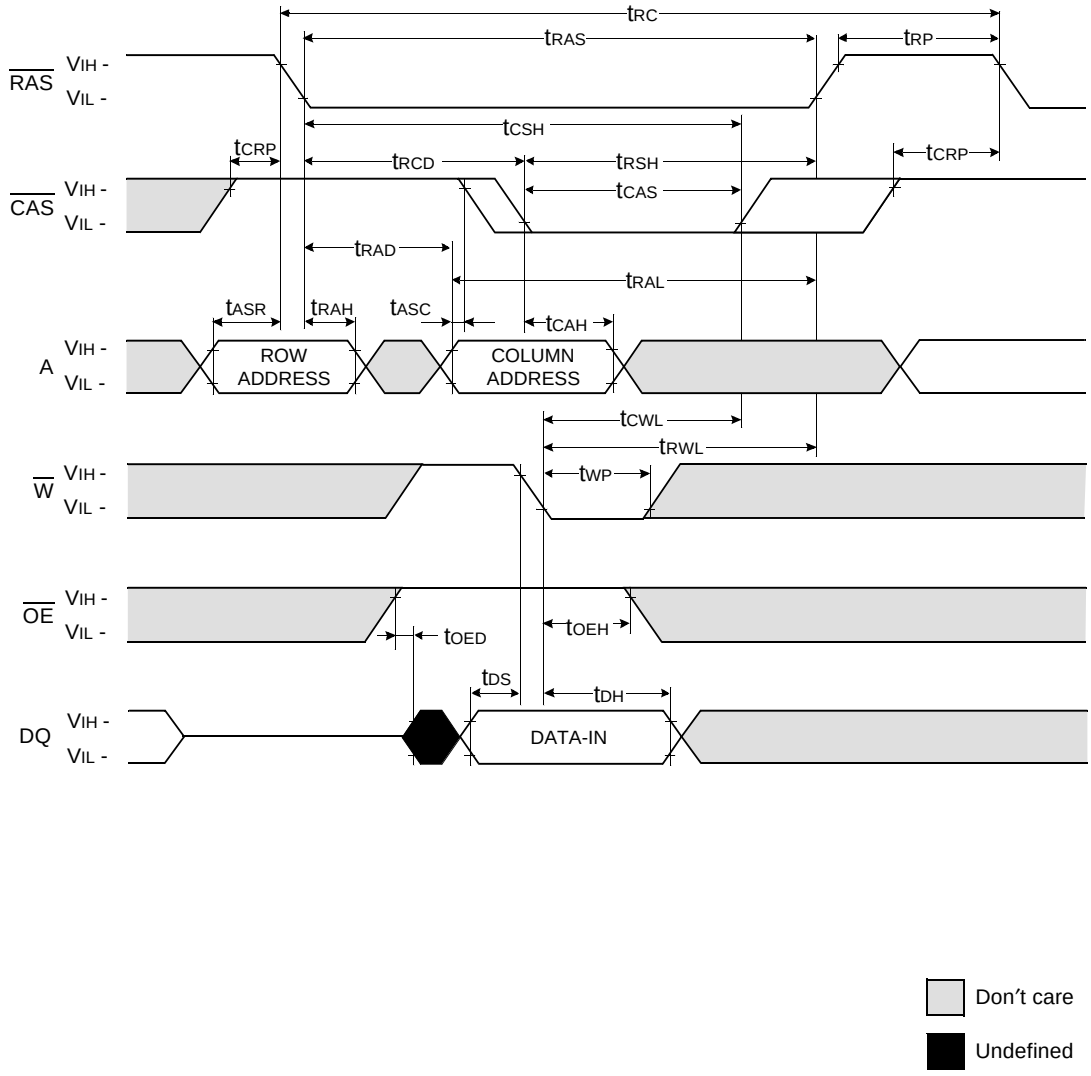
NOTE : DOUT = OPEN



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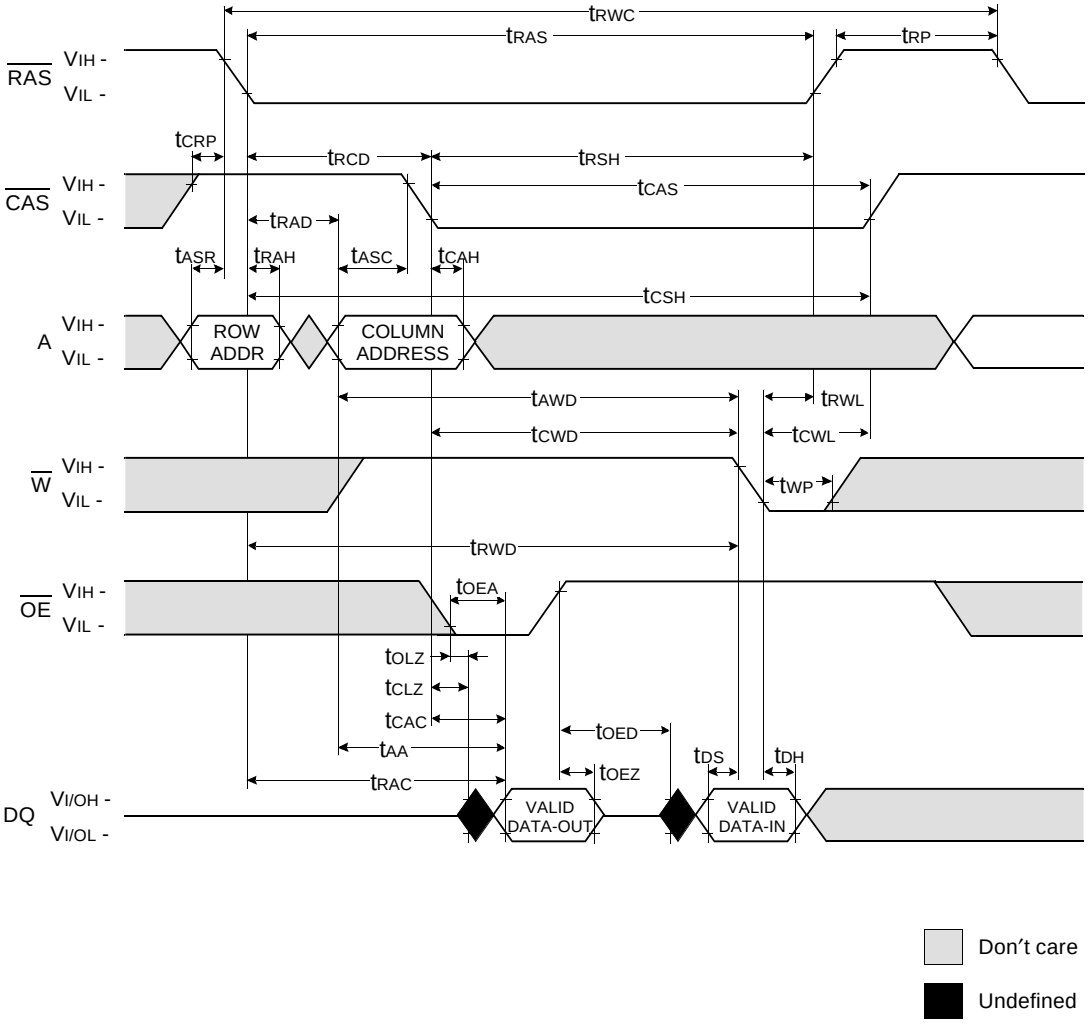
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



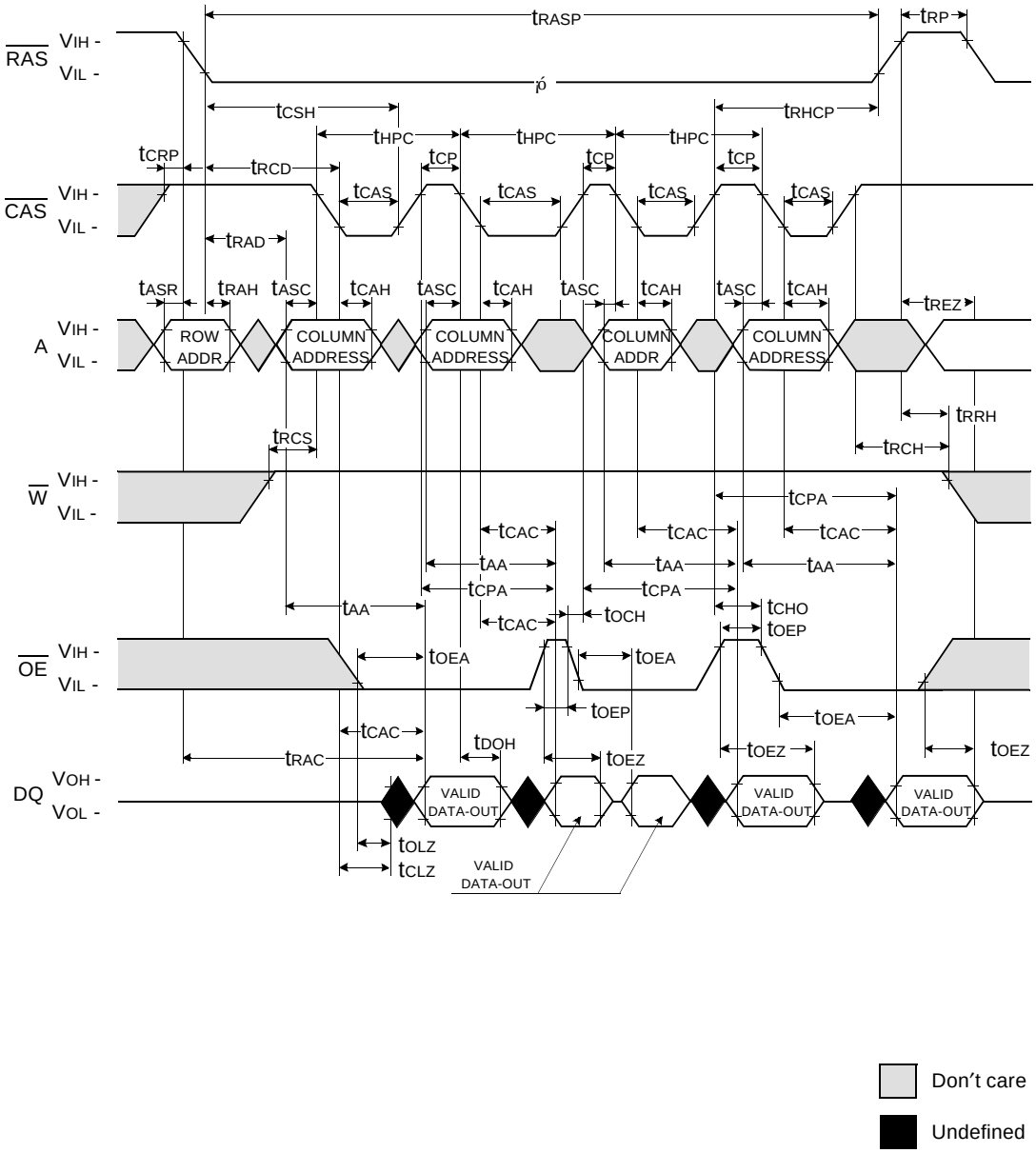
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READ - MODIFY - WRITE CYCLE



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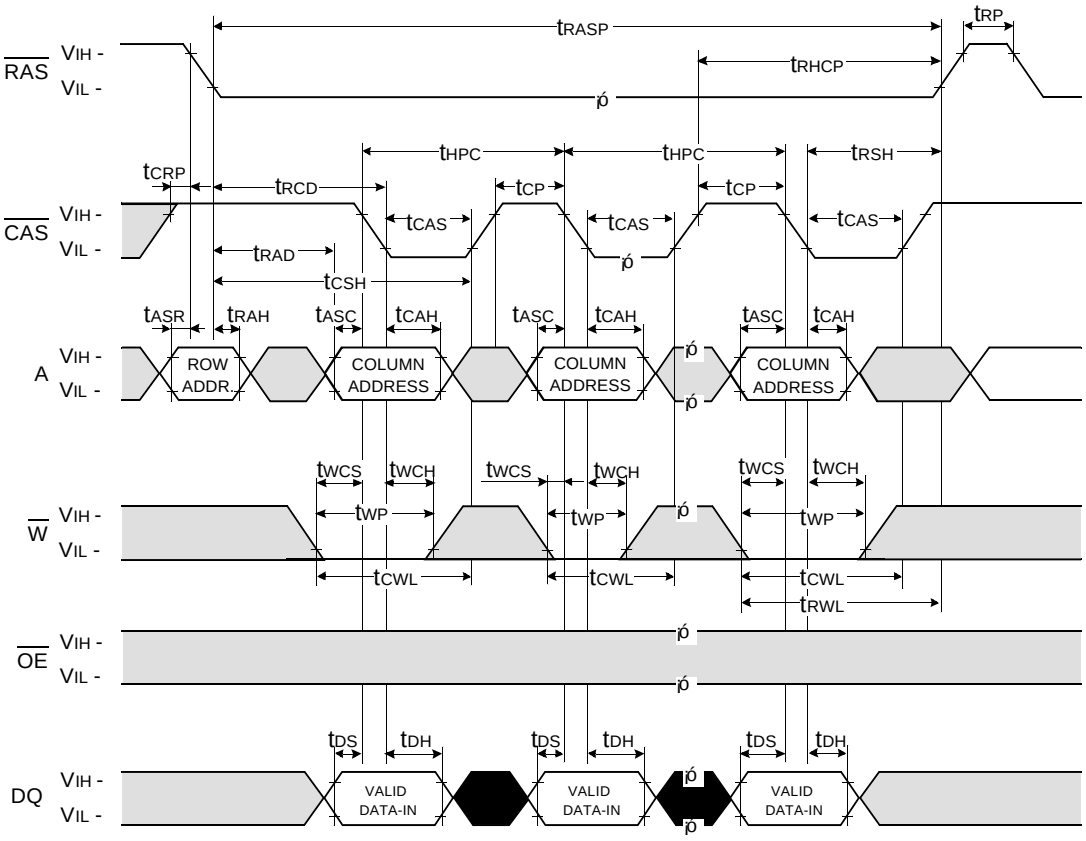
HYPER PAGE READ CYCLE



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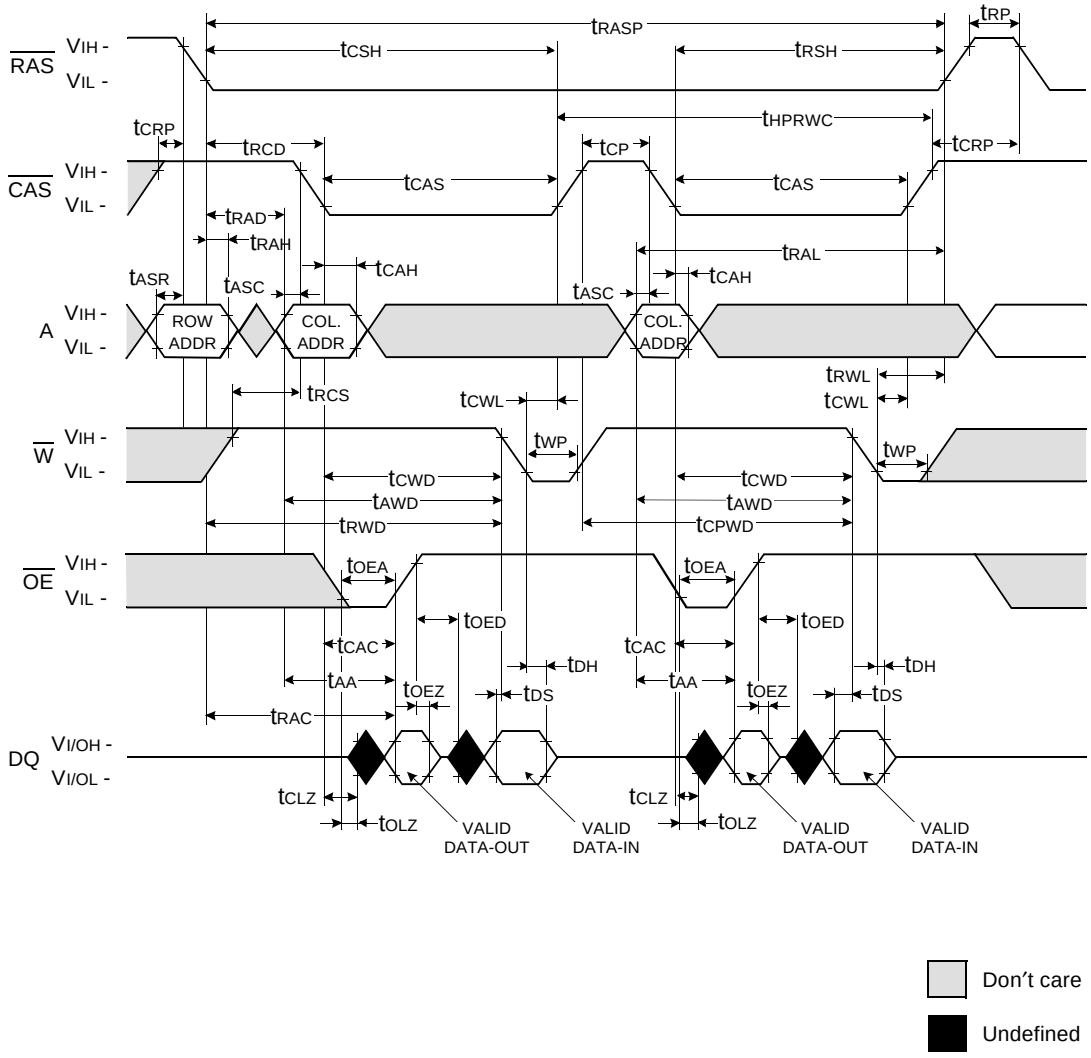
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



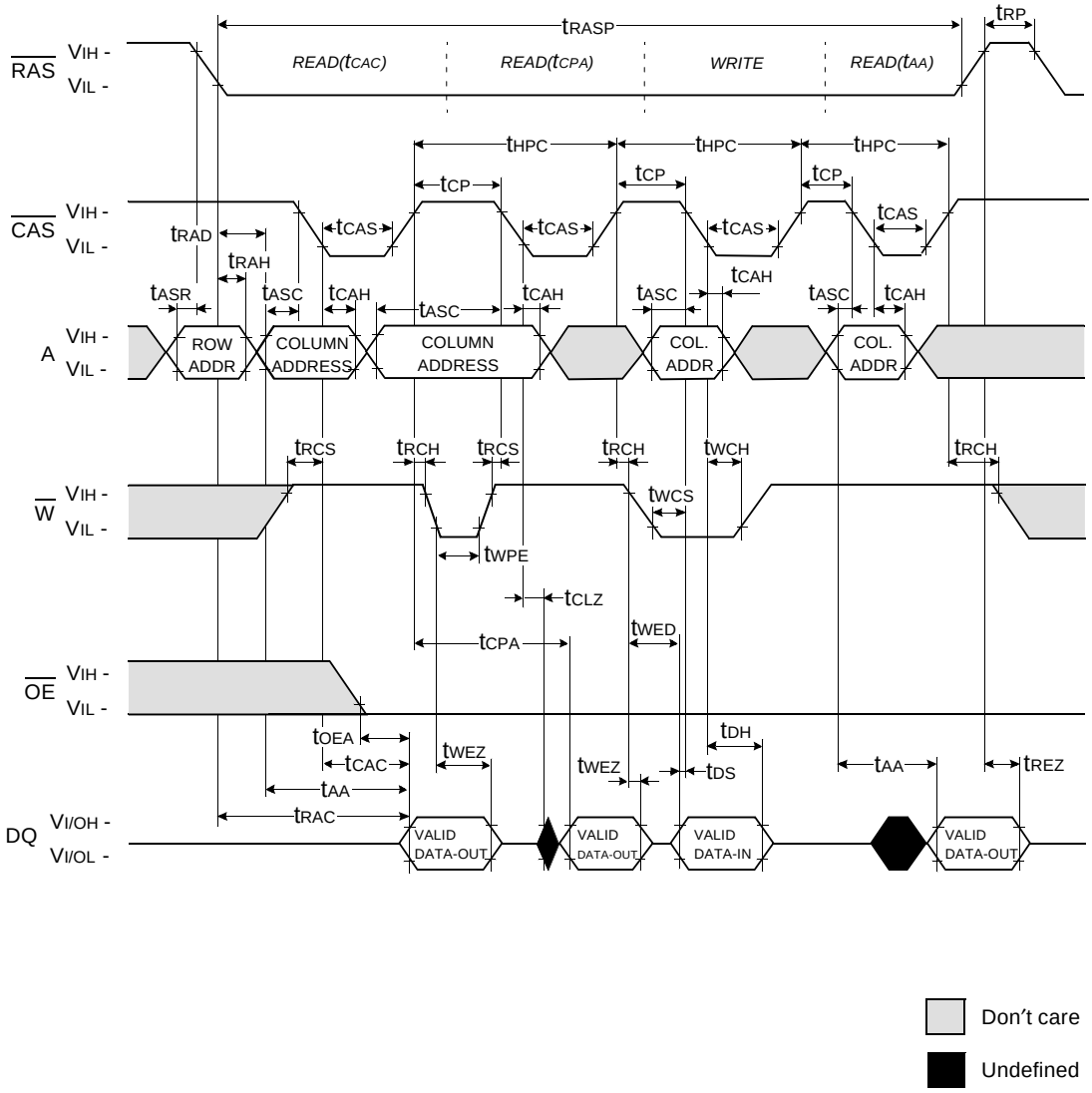
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HYPER PAGE READ-MODIFY-WRITE CYCLE



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HYPER PAGE READ AND WRITE MIXED CYCLE

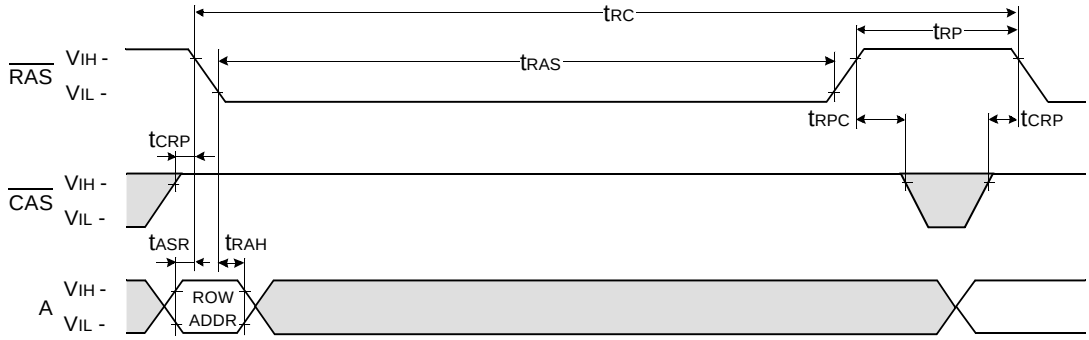


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$\overline{RAS}$ - ONLY REFRESH CYCLE*

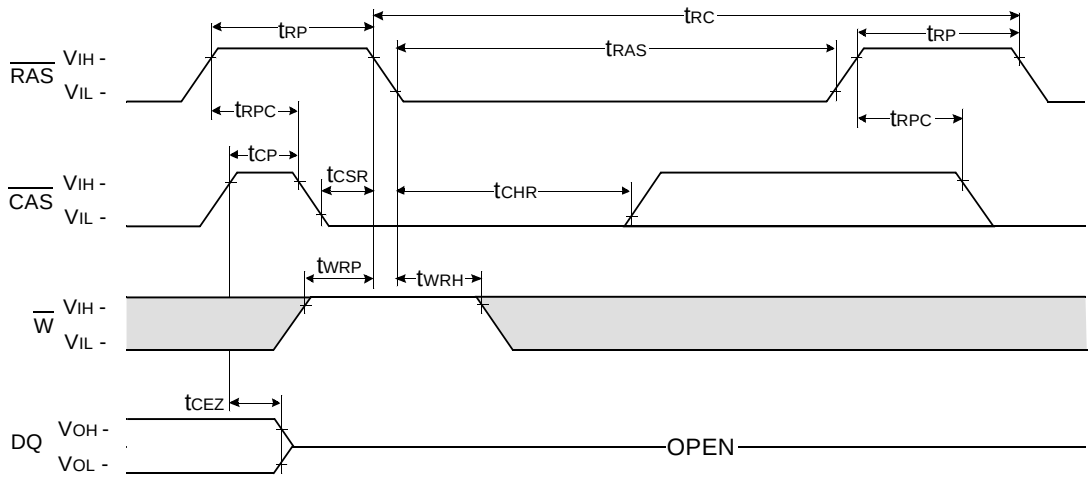
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



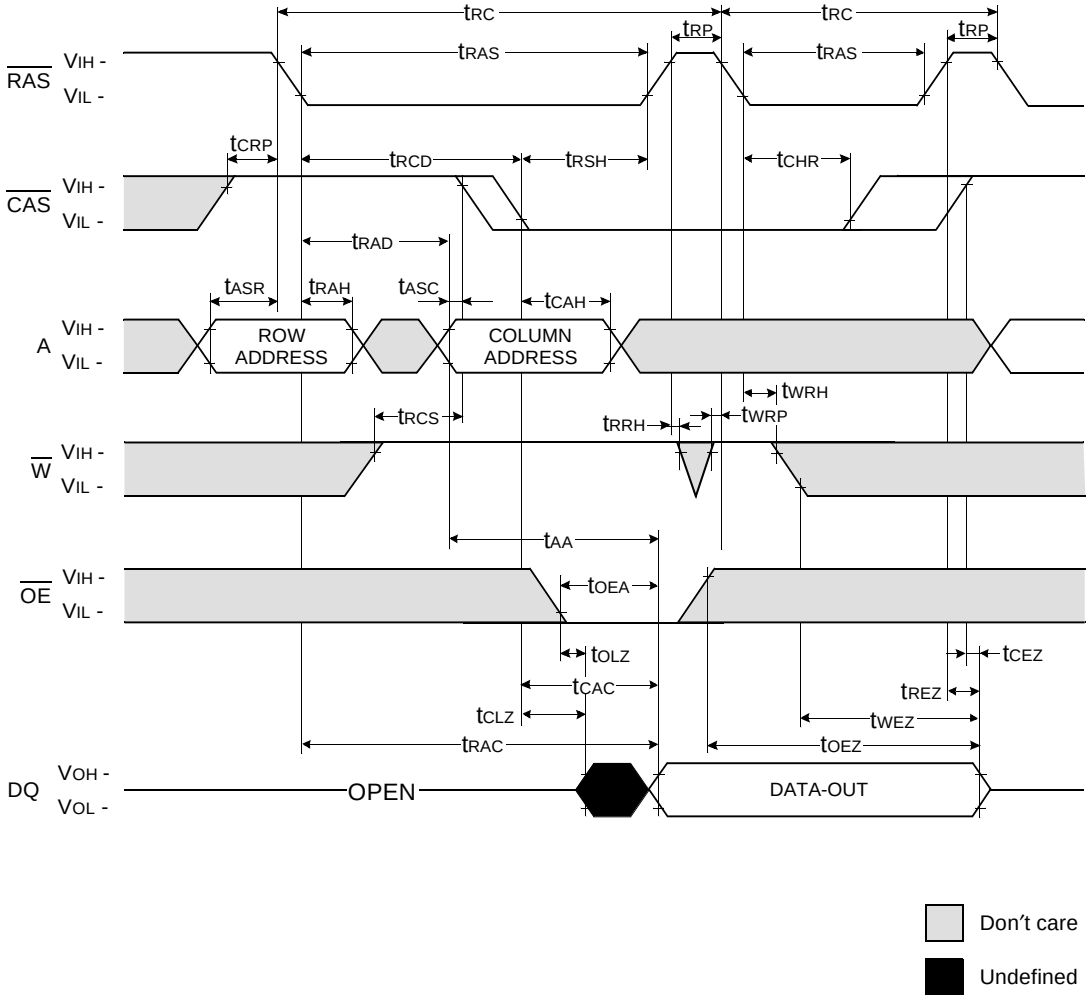
Don't care

Undefined

* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

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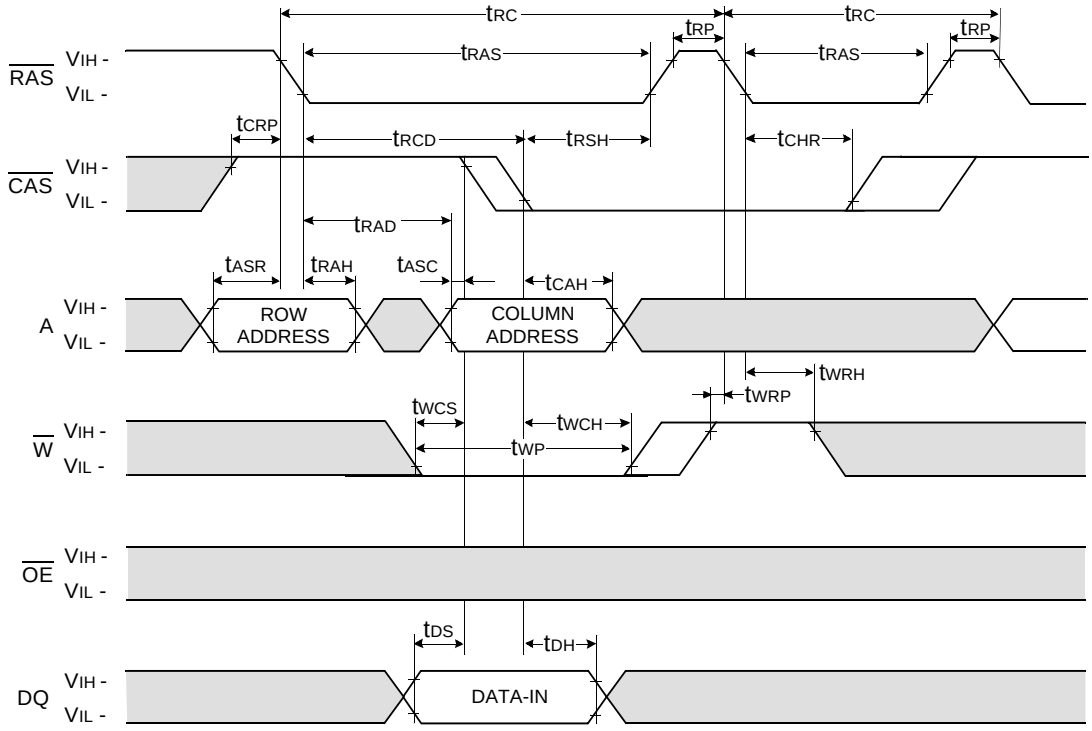
HIDDEN REFRESH CYCLE (READ)



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HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

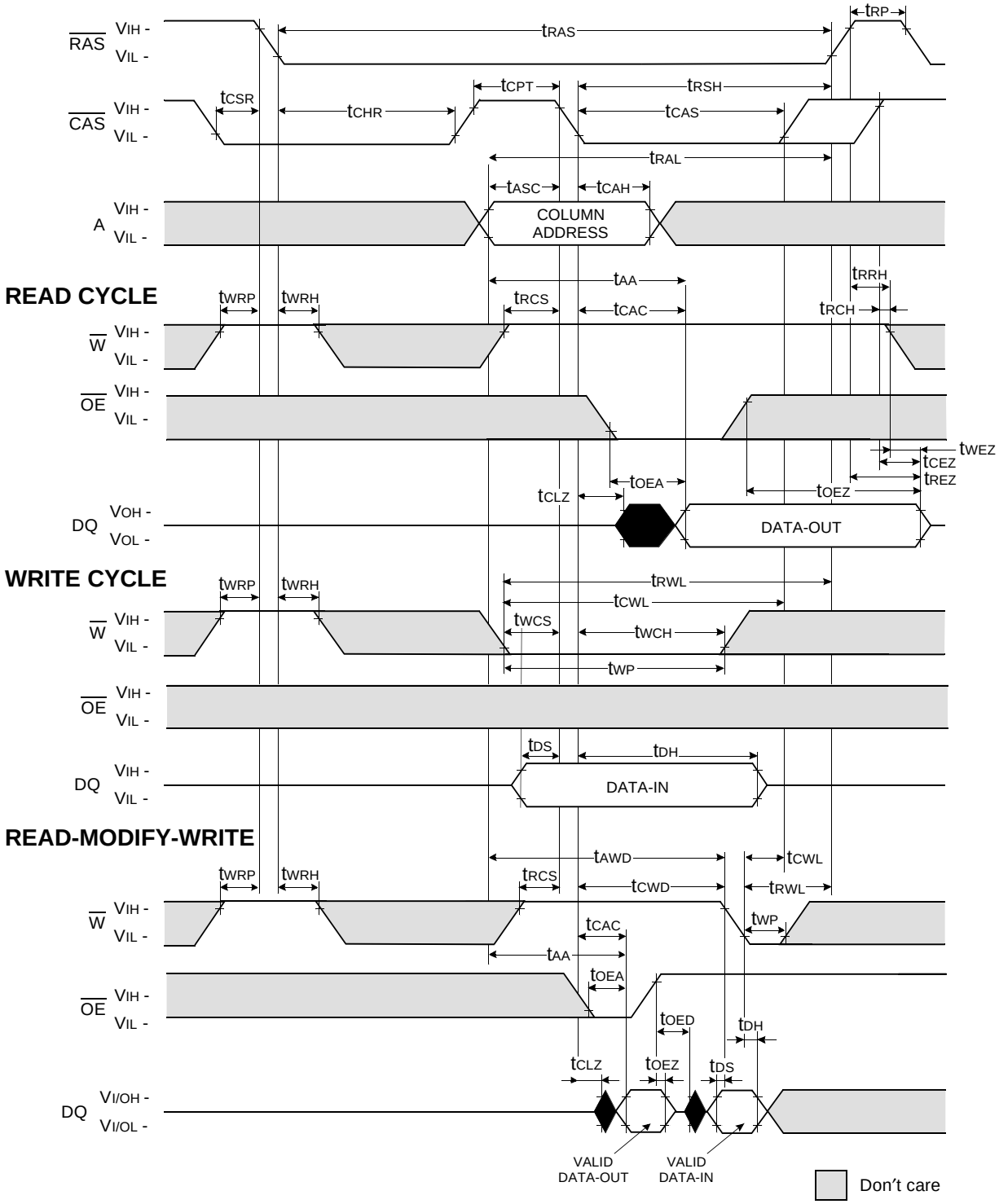


Don't care

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CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

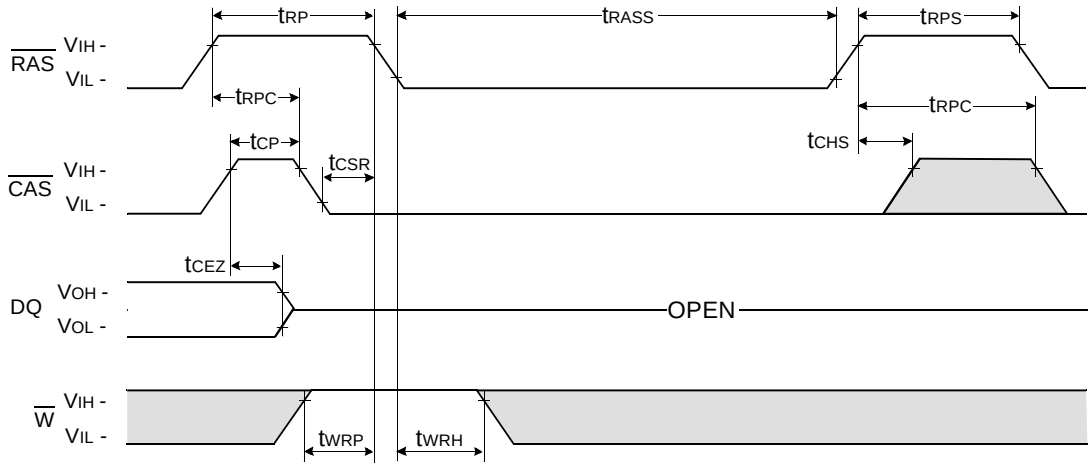


NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

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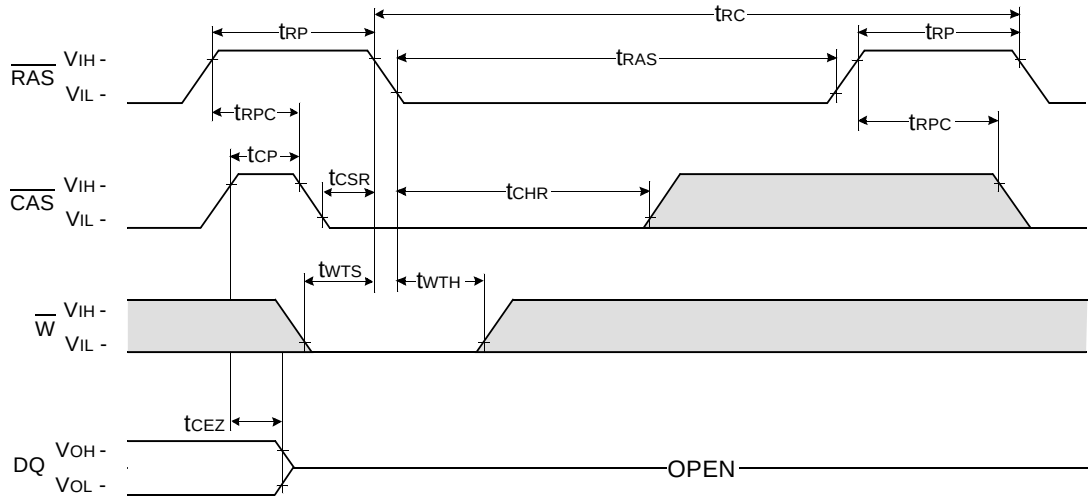
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



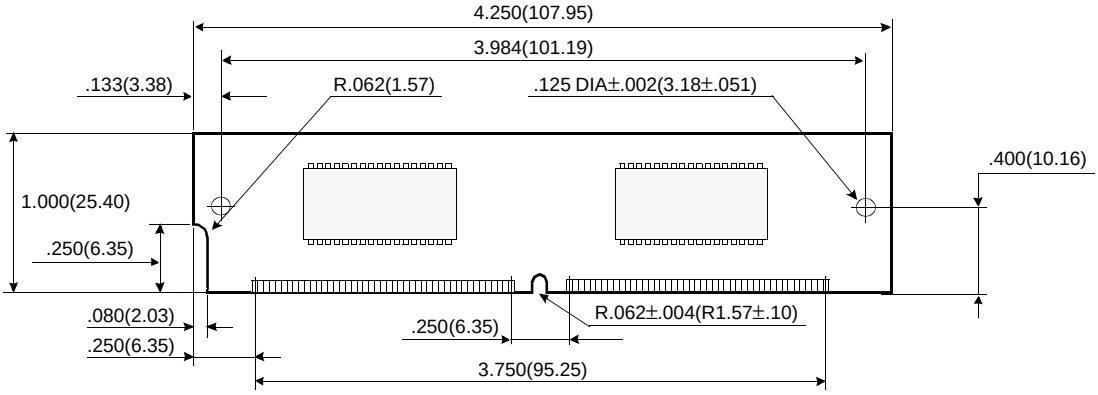
Don't care

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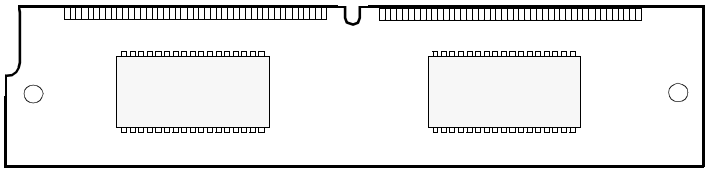
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PACKAGE DIMENSIONS

Units : Inches (millimeters)

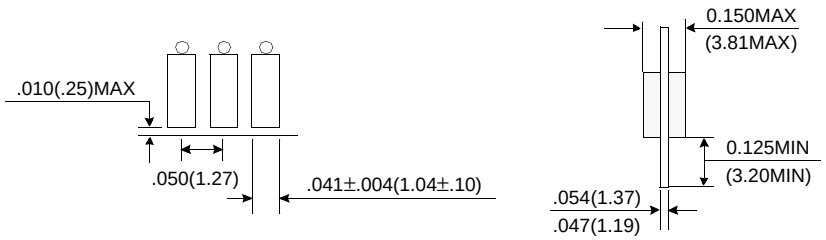


(Front view)



(Back view)

Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 4Mx16 DRAM, TSOPII
DRAM Part No. : M53230804CY0/CT0 -- K4E641611C (400 mil)