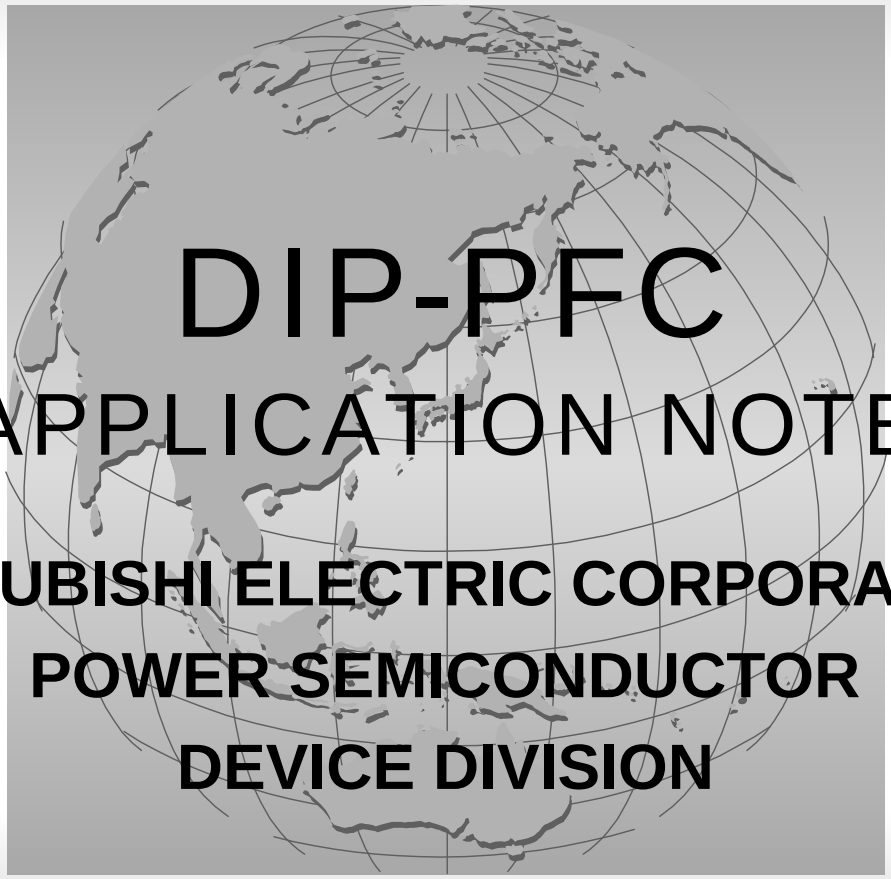
Application Note	Prep.		Rev.				
	Apr.						

TENTATIVE



DIP-PFC
APPLICATION NOTE

MITSUBISHI ELECTRIC CORPORATION
POWER SEMICONDUCTOR
DEVICE DIVISION

Table of Contents

CHAPTER 1 PRODUCT OUTLINES

1.1 Applications and Features

DIP-PFC (Dual-In-line-Package Power-Factor-Correction) is an IPM used for the power factor correction of AC-DC-AC inverter systems such as inverter air-conditioners, general-purpose inverters, etc. It is a highly integrated power module manufactured by the means of transfer mold technology, and featured with the following advantages:

(1) Compact Structure

DIP-PFC realizes a very compact active converter structure by Integrating a conventional AC/DC converter, and high speed switching elements IGBT in one package, which contributes to a perfect system solution of with small size, simplification, high reliability and low cost.

(2) Transfer Mold Package

DIP-PFC is manufactured by using the transfer mold technology, which realizes smaller size, lower cost and improved productivity. Furthermore, By mounting a DIP-PFC on the same control board with DIP-IPM, minimum wiring and share of one heat sink can be easily realized.

(3) Lower Power Loss

DIP-PFC employs the low loss IGBT and Diode chips. The total power loss is reduced by about 10% comparing to traditional products, which contributes to an improved system efficiency.

(4) Excellent Performance

By combined utilization with the application specific control IC, the output voltage can be controlled in a wider range, and the high order current harmonic problem can be completely cleared which leads to a high power factor over 99%.

(5) Abundant Protective Functions

DIP-PFC and the control IC are designed with various protective functions for the prevention of module destruction against steep variation of load and various abnormal operations, which improves the reliability of the total system.

1.2 Products Line-up

Table 1 DIP-PFC family

	Input Voltage Rating (Vi)	Input Current rating (Ii)	Typical Switching Frequency (f_{PWM})	Isolation Grade Viso
PS51277-A	90～264V	15Arms	20kHz	AC1500Vrms (Sinusoidal 1min)
PS51259-A	90～264V	20Arms	20kHz	

1.3 Structure and Functions

1.3.1 Module Structure

Fig.1(a) and (b) show the DIP-PFC package photograph and its cross-section diagram, respectively.

In order to avoid erroneous installation with DIP-IPM, some pins are specially treated, such as lead cut and with wider width.

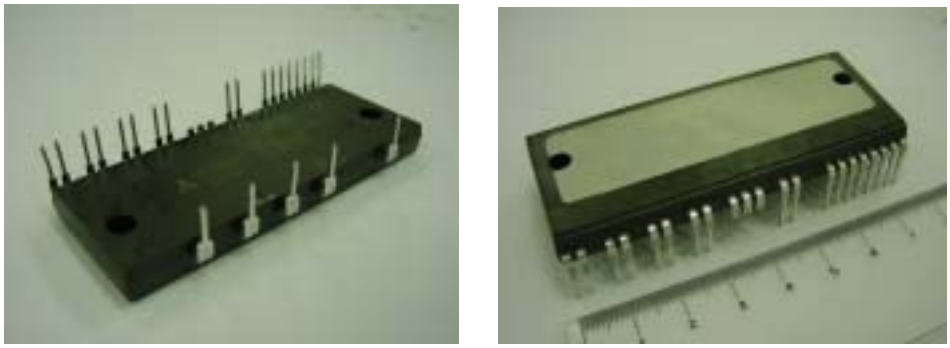


Fig.1(a) DIP-PFC photograph

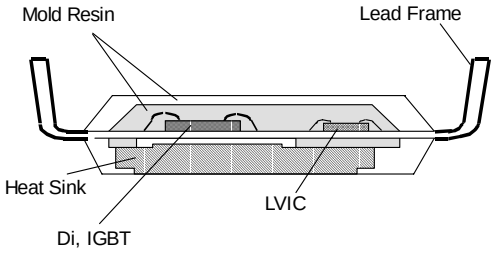


Fig.1 (b) Cross-Section diagram of DIP-PFC

1.3.2 Internal Circuitry Topology

Fig.2 shows the internal circuitry of DIP-PFC, which consists of a full-wave diode rectifier bridge and two IGBT elements parallel connected to the negative-side of the diode bridge, and an LVIC for drive of the IGBTs.

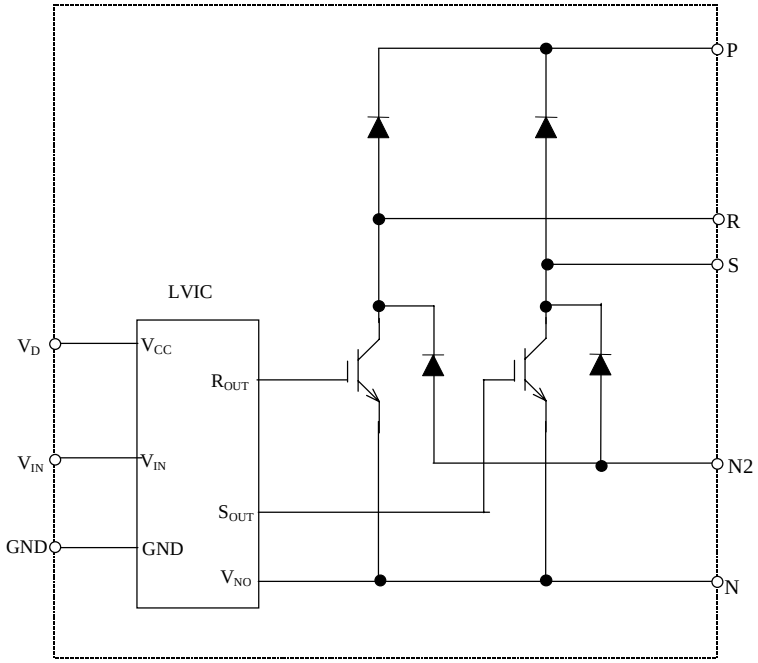


Fig.2 DIP-PFC circuitry diagram

1.3.3 Built-in Functions

(a) AC/DC conversion: Converting commercial single phase AC input into DC output.

(b) IGBT drive and protection: The built-in LVIC provides the functions of IGBT gate drive and control supply under voltage (UV) protection.
PFC operation becomes unstable and easy to cause malfunction if control supply is below a certain level. It is necessary to block IGBT operation immediately if UV happens.

(Note): LVIC inside the DIP-PFC only provides the function of IGBT gate drive and UV protection, the DIP-PFC control circuitry and OV/OC protective functions are not built-in. Therefore, a set utilization of the control IC with the DIP-PFC is necessary.

CHAPTER 2 ELECTRIC CHARACTERISTICS

2.1 Static Characteristics

Table 2 Typical static characteristics of DIP-PFC

Symbol	Parameters	Condition	Rating	
			PS51277-A	PS51259-A
I_{CES}	Collector-emitter shut-down current	V_{CE}=600V, Tj=25℃	1.0mA(max.)	1.0mA(max.)
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D=15V, V_{CIN}=5V,Tj=25℃ (Note1)	2.0V(Typ.)	1.8V(Typ.)
V_F	Diode Forward voltage drop	Tj=25℃, V_{CIN}=5V (Note 2)	1.6V(Typ.)	2.1V(Typ.)
I_{rr}	Diode Recovery current	Vcc=300V,VD=15V, Tj=25℃ (Note 3)	13A(Typ.)	13A(Typ.)

Note1：PS51277-A@Ic=30A、PS51259-A@Ic=50A

Note 2：PS51277-A@-Ic＝30A、PS51259-A@-Ic＝50A

Note 3：PS51277-A@Ic=20A、PS51259-A@Ic=30A

2.2 Switching Characteristics

Table 3 Typical switching characteristics of DIP-PFC

Symbol	Parameter	Condition	Rating	
			PS51277-A	PS51259-A
ton	Switching time	V_{CC}=300V, V_D=15V Tj=125℃, V_{IN}=0⇔5V, Inductive Load (Note 4)	0.23us(Typ.)	0.29us(Typ.)
toff			0.43us(Typ.)	0.46us(Typ.)
tc(on)			0.14us(Typ.)	0.15us(Typ.)
tc(off)			0.23us(Typ.)	0.17us(Typ.)

Note 4：PS51277-A@Ic=20A、PS51259-A@Ic=30A

2.3 Recommended Operation Conditions

Item	Symbol	Condition	Value			Unit
			min.	typ.	max.	
AC input voltage	V_{CC}	Between S-R terminals	90	–	264	V_{rms}
Control Supply	V_D	Between V_D－GND terminals	13.5	15.0	16.5	V
PWM Carrier Frequency	f_{PWM}	Tc≦100°C, Tj≦125°C	–	20	–	kHz
Input on voltage	$V_{IN(ON)}$	Between V_{IN}－GND terminals	4.0～V_D			V
Input off voltage	$V_{IN(OFF)}$		0～1.0			V

2.4 Waveforms of Input Current/Voltage and Current Harmonic

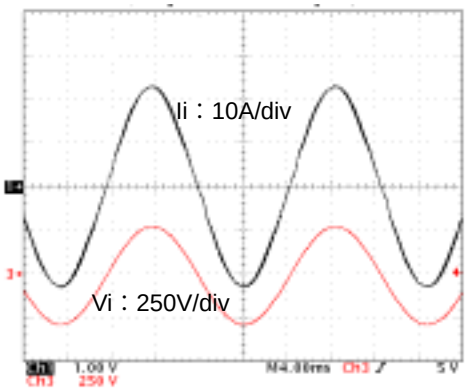


Fig.3 Input current/voltage wave of PS51259-A

Condition: Vi=200V, Ii=15.732A, Vo=275.6V, P.F=99.9%

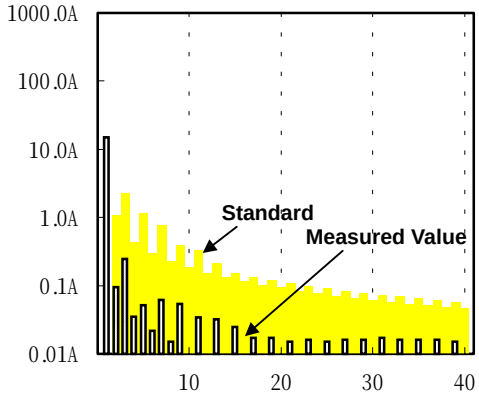


Fig. 4 Current harmonic of PS51259-A

Condition: Vi=200Vrms, 60Hz, Vo=370V, fsw=20kHz

CHAPTER 3 PACKAGE

3.1 Package Outline Drawing

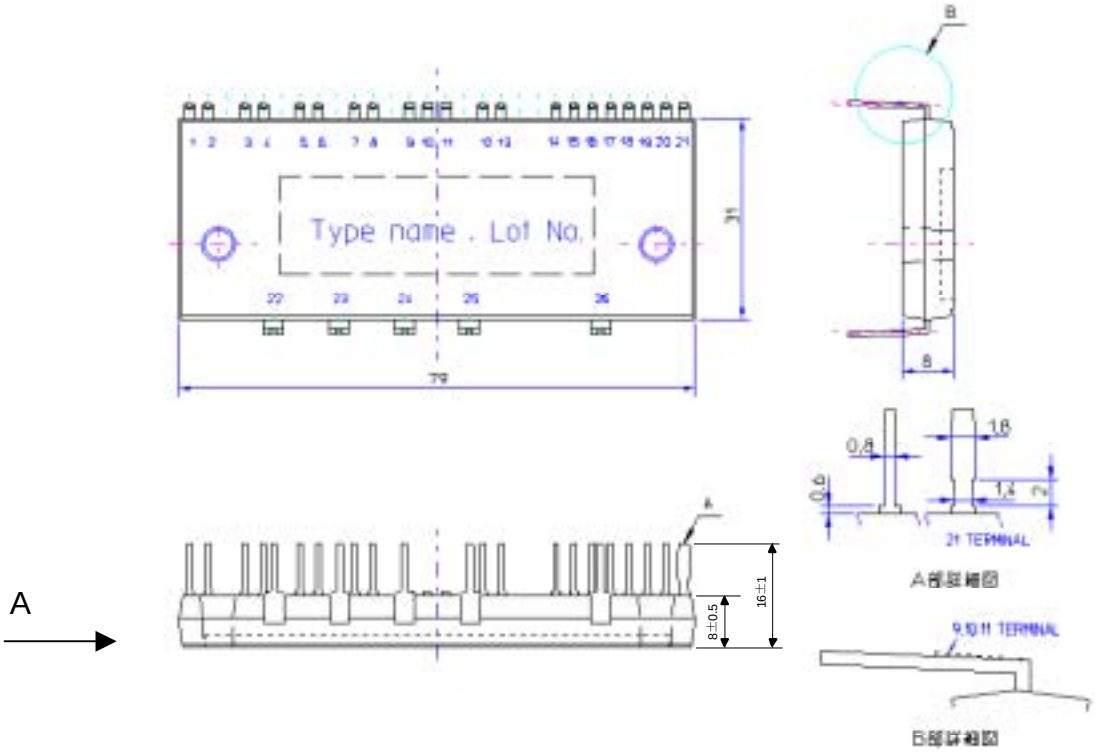


Fig. 5 Package Outlines

3.2 Laser Marking

Fig. 6 shows the laser marking range of DIP-PFC. Mitsubishi mark, type name(area A), lot number(area B) are marked in an area of 42.5×8mm, positioned 38mm far away from the right edge of the package.

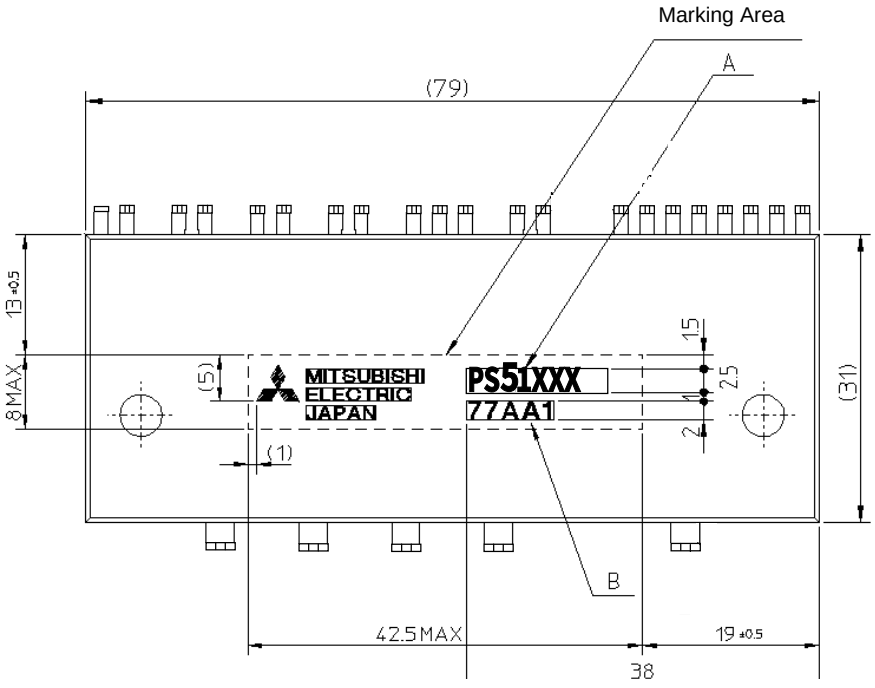


Fig. 6 Laser marking

3.3 Description of Input/Output Terminal

Table 4 Description of input/output terminal

No.	symbol	Terminal Name	Content
1 2	N2	Output Terminal of PFC	・Connected with the minus side of the converter. ・A shunt resistor is inserted between N2 and N terminals to detect DC bus current.
14	GND	GND of Control Supply	・This is the GND of DIP-PFC. ・In order to avoid the GND potential variation due to IGBT switching, please add a fast clamp diode between this GND and the N terminal.
15	VD	Control Supply (+)	・The positive terminal of the 15V supply of LVIC. ・Please add a noise filter with good temperature and frequency characteristics near the terminal to prevent DIP-PFC malfunction from noise intereference. ・Please ensure the voltage ripple within the specifications. ・Please add a Zenner diode(24V/1W) between the control supply terminals to protect LVIC from surge destruction if the surge voltage is large.
16	V_{IN}	Control Input	・Input terminal of LVIC. Please connect it to the output terminal of the control IC. If the signal is affected by noise, please add a noise filter with good temperature and frequency characteristics near the input terminal.
17	GND	GND	・The input signal GND, connected to the control supply GND inside.
22	P	Output Terminal of PFC	・Connected with the positive side of internal converter. ・Connect to the positive polarity of inverter input terminal. ・An electrolytic condenser should be mounted as closely as possible to the P&N terminals so as to suppress surge voltage. In addition, a film condenser with good frequency characteristics is also necessary.
23	S	AC Input Terminal	・Connect to commercial AC supply via ACL.
24	R	AC Input Terminal	・Connect to commercial AC supply via ACL.
25 26	N	IGBT Emitter	・In order to measure the bus line current, please insert a shunt resistor between N and N2 terminals. ・The two IGBTs' terminals are connected inside DIP-PFC.

Note: No. 3～13,18～21pins are dummy pins, therefore, should not be connected to PCB pattern

3.4 Function Description

Table 5 Function description

Item	Symbol	Content
Normal Operation	—	・The input drive logic is high-active. ・IGBT turns on if the input signal voltage level is higher than $V_{th(on),}$ and IGBT turns off if the signal level is lower than $V_{th(off),}$
Control Supply Under Voltage	UV	・The LVIC monitors the control supply voltage. If there is an under voltage happens within a certain period of time, IGBT gate will be interrupted immediately, and the control input will be suspended. ・The UV state is defined to be the period from the time the control supply drops below the UV trip level to it rises again to the UV reset level. ・The control input will be released in the next pulse soon after the control supply rises over the UV reset level.

3.5 Installation Guidelines

Fastening a module to a heat sink with excessive uneven stress might cause devices to be damaged or degraded because over stress will apply to the internal silicon chips. An example of recommended fastening order is shown in Figure 7. Approximately, set the temporary fastening torque to be 20～30 % of the maximum rating.

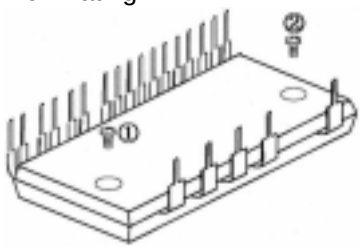
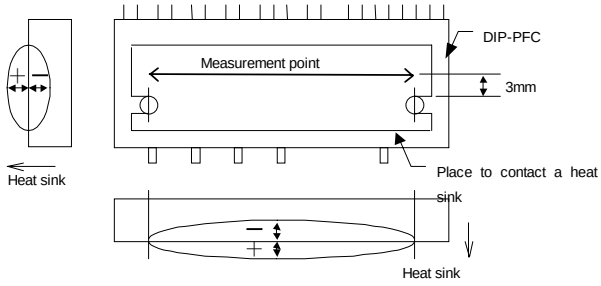


Fig. 7 Recommended Fastening Order of Mounting Screws

Table 6. Mounting Torque and Heat Sink Flatness Specifications

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw : M4	Reccomended 1.18N･m	0.98	1.18	1.47	N･m
		Reccomended 12 kg･cm	10	12	15	kg･cm
DIP-PFC flatness	−		−50	—	+100	um
Heat sink flatness			−50	—	+100	um



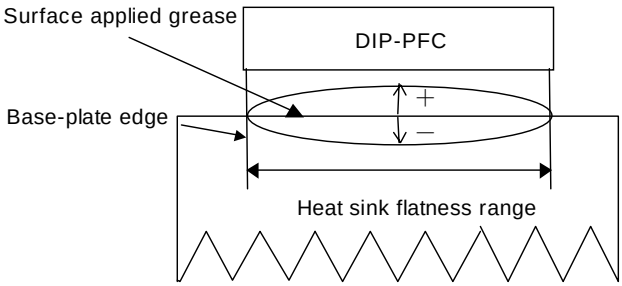


Fig. 8 Flatness measurement point of heat sink.

Tightening torque test

Tightening torque test is to investigate the maximum allowable tightening torque under which DIP-PFC package will not broke or voltage endurance; inserting a 100um thickness gauge between DIP-PFC and Heat-sink, tightening DIP-IPM gradually to the heat-sink with 0.098N･m (1kg･cm) unit from 1.18Nm (12kg･cm).

Tightening torque is confirmed to be more than 0.98N･m (10kg･cm), even in the worst condition.

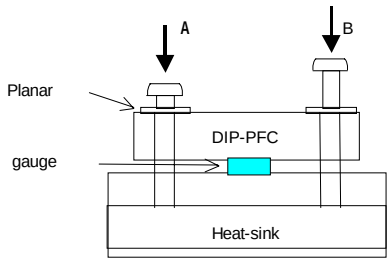


Fig.9 Tightening torque test

Heat sink flatness is prescribed as shown in Figure 8. For most effective heat-radiation it is necessary to enlarge as much as possible, the contact area between the module and the heat sink to minimize the contact thermal resistance. According to the heat sink flatness (surface warp/concavity and convexity) on the module installation surface (refer to Figure 9). Also, the surface finishing-treatment should be less than 12um.

Evenly apply 100um～200um grease with good thermal-conductivity over the contact surface between a module and a heat sink. It is also helpful for preventing the contact surface from corrosion . Further more, use grease with stable quality within the operating temperature range and have long endurance. Use a torque wrench to fasten up to the specified torque. Exceeding the maximum torque limitation might cause

the modules to be damaged or degraded as the above mentioned fastening with uneven stress. Please pay attention not to remain any ash on the contact surface of the module and the heat sink.

3.6 Temperature measurement of DIP-PFC Case and Heat Sink

The heat sink should be such designed to have enough thermal dissipation capability that the case temperature and IGBT junction temperature of DIP-PFC would not exceed the maximum ratings even at the worst condition. If the DIP-PFC operates at a temperature over the specification, it will possibly lead to a thermal destruction.

Therefore, please select the heat sink on the basis of a careful thermal calculation. In addition, it is also necessary to confirm the effect by a prototype evaluation.

Please measure the case temperature at the position as shown in Fig. 10.

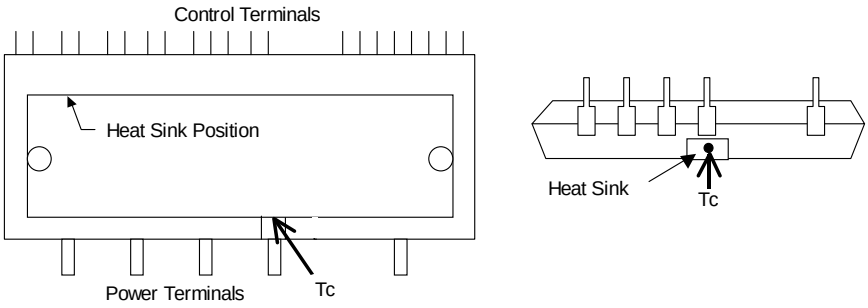


Fig. 10 Case temperature measurement point

CHAPTER 4 SYSTEM APPLICATIONS

4.1 System Connections

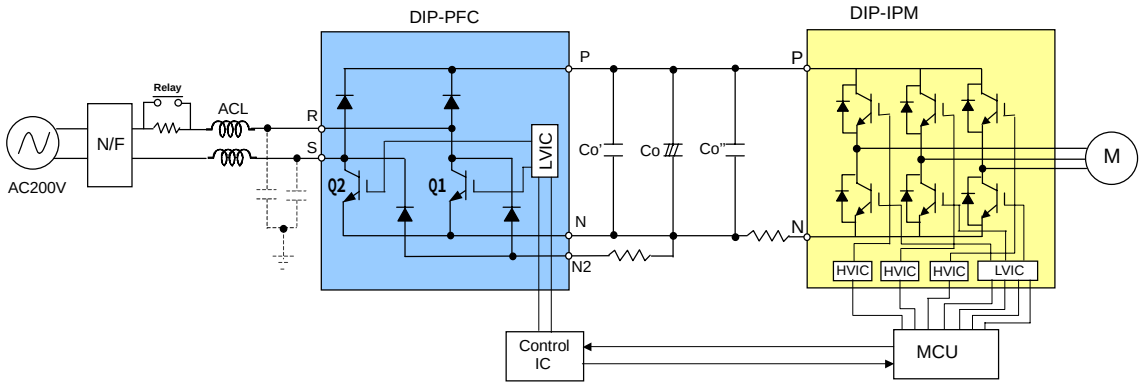


Fig. 11 System connection block diagram

Note:

2. To operate DIP－PFC properly and make full use of its excellent performance, it is necessary that the DIP-PFC should be used together with its control IC and DIP-IPM.
3. It is necessary to operate DIP-PFC, the control IC, DIP-IPM and MCU on the same GND stage. This GND is usually set to the DIP-PFC N terminal.
4. A large charge current of the electrolytic condenser will flow on the DIP-PFC when applying AC supply, which might cause destruction. Therefore, An Inrush current prevention circuit shown in Fig. 10 is necessary. Open the relay when condenser Co is initially charged, and close it after the charge is over.
5. Large surge voltage is easily produced between P&N terminals when switching large current at a high frequency. The countermeasure to the surge is to shorten the DC-link bus wiring between DIP-PFC and the DIP-IPM as possible as you can. Also, the capacitance of the electrolytic condenser should be large enough to absorb the surge voltage generated both by DIP-PFC and DIP-IPM. In addition, it is necessary to mount a condenser with good high frequency characteristics, such as polypropylene film condenser closely to the P and N terminals of DIP-PFC.
6. In case of mounting the DIP-PFC on the same heat sink as that of DIP-IPM, please make sure that the mounting height and grease thickness of the two modules are the same, so as to minimize the contacting thermal resistance of both modules.
7. Recommendation: ACL:1mH,
   Co: Electrolytic condenser (sutibale for high frequency) ,1000～2000uF/450VDC,
   Co': Polypropylene film Condenser (suitable for high frequency) , 0.22uF／630VDC

＊ Concerning DIP-IPM, please refer to its application note DPH-0352-B.

4.2 Recommended system Composition

PFC	Control IC	IPM	Remark
PS51277-A	M81012FP*	PS21865, PS21245-E	
PS51259-A	M63914FP	PS21867, PS21246-E	

(*) Under Development

4.3 DIP-PFC Wiring Guidelines

Because DIP-PFC switches large current at a very high speed, considerable large surge voltage is generated easily between P and N terminals. Please pay attention to the following items:

- The area of P-Co-N shown in Fig. 12 should be as small as possible because the rectangle shaped switching current flows on this route. In addition, please add a bypass condenser Co' with good frequency response such as a polypropylene film condenser closely to the P and N terminals.
- The two IGBT emitters are connected to the VNO terminal of LVIC inside the DIP-PFC. If the internal wiring inductance shown as L1 and L2 in Fig. 13 is too large, large surge voltage will be generated by di/dt. Especially, the lower the temperature, the faster the switching speed, therefore the larger the di/dt. This surge voltage applies to the VNO and N terminals, which is possible to destruct LVIC.
- In order to suppress the surge voltage, the external wiring method shown in Fig. 13 is recommended. To reduce the parasitic wiring inductance, the wiring of the external terminals of $N_{(N-1)}$ and $N_{(N-2)}$ should be made as short as possible.
- Please mount a fast clamp diode (EG01Y@Sanken) between N and control GND terminals to prevent control GND potential variation from the minus voltage of N terminal.

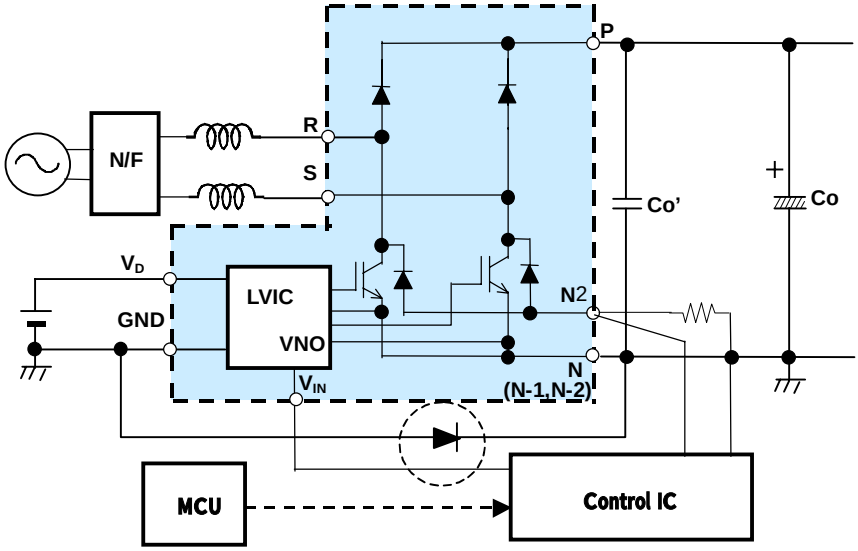


Fig. 12 DIP-PFC Interface

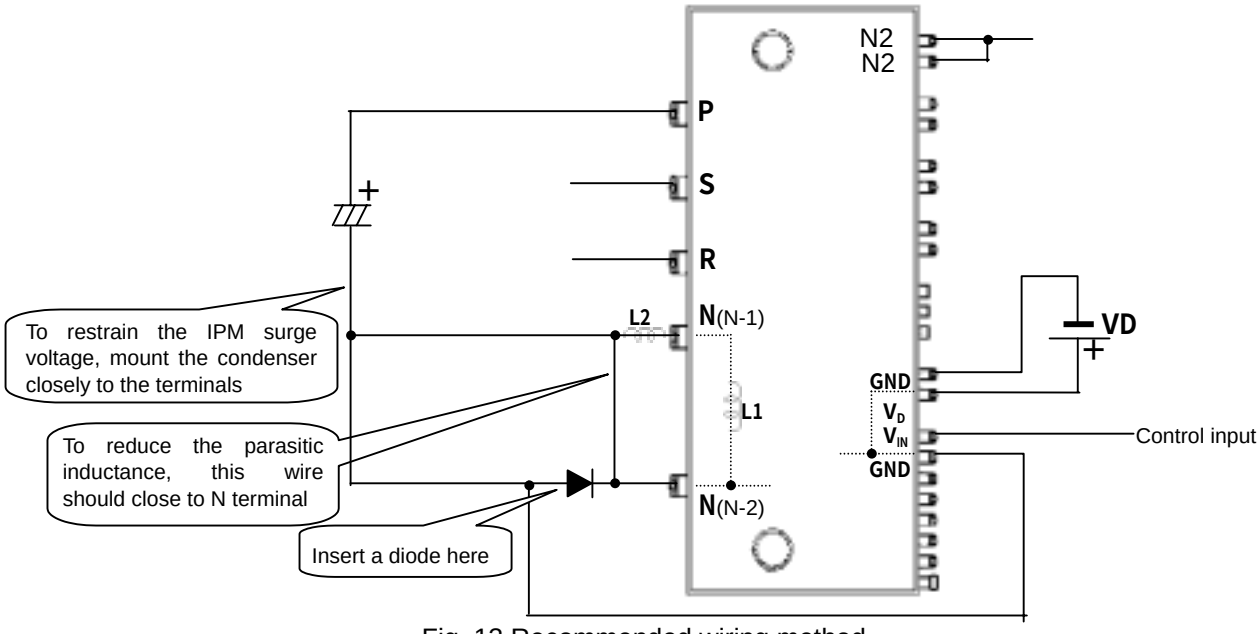


Fig. 13 Recommended wiring method

4.4 DIP-PFC Operation Sequence

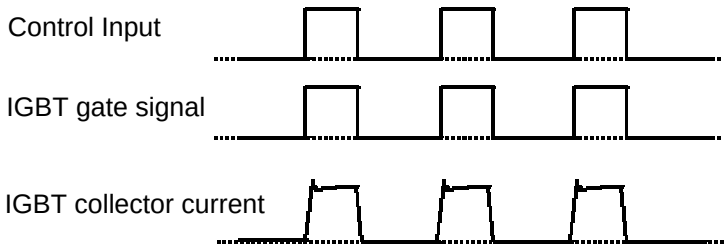
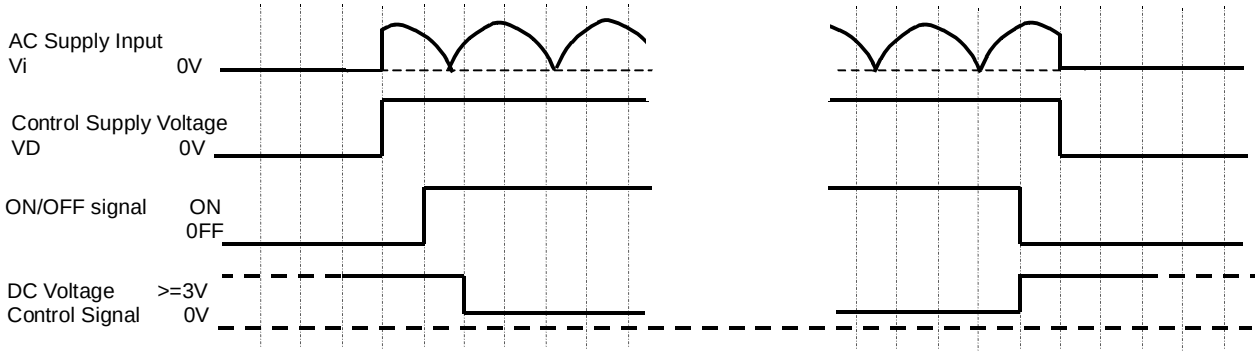


Fig. 14 DIP-PFC operating sequence

4.5 Start-up and Stop Operation Sequence of AC Supply, Control Supply and Control Signal

Please follow the sequence shown in Fig. 15 to start-up and stop PFC so as to avoid malfunction or abnormal destruction due to noise or other disturbance at start-up and stop operation.

The DC voltage control signal Vctrl should be activated after the ON/OFF switch is turned on.



(a) Start-up sequence (b) Stop sequence

Fig. 15 Start-up and stop operation sequence

There are possibility that the LVIC output will not be ON when the VD is in rising state from 0V even the ON/OFF signal is set to ON level.

This phenomenon is understood that the initial state of the internal protective circuit is not stable (Hi or Lo) at the control voltage rising period. In this case, please turn off the ON/OFF signal to reset the IC. In addition, even if the IC output can set to ON state, the IGBT gate might be blocked due to abnormal input such as noise.

To avoid such problem, please set the ON/OFF signal after the VD has completely established.

4.6 Noise Withstand Capability

The noise withstand capability of DIP-PFC is carried out under the following conditions, from which over ± 2.0kV withstand capability has been confirmed. However, noise withstand capability greatly depends on the test conditions, such as the wiring patterns of control substrate, parts layout, and motor type etc., therefore the actual system test should be performed. Fig. 16 shows the evaluation system.

(1) Common noise test condition:

Vi=200V, V_D=15V, Ta=-20～80℃, Line noise pulse width tw=1μs/T=16ms, Amplitude=±2kV
Continuous pulse input with pulse width 15μs/T=50μs to DIP-PFC input terminals.

(2) Thunder surge test condition:

Vi=200V, V_D=15V, Ta=25℃, Thunder surge pulse width tw=1.2μs/T=50μs, Amplitude=±7kV
Continuous pulse input with pulse width 15μs/T=50μs to DIP-PFC input terminals.

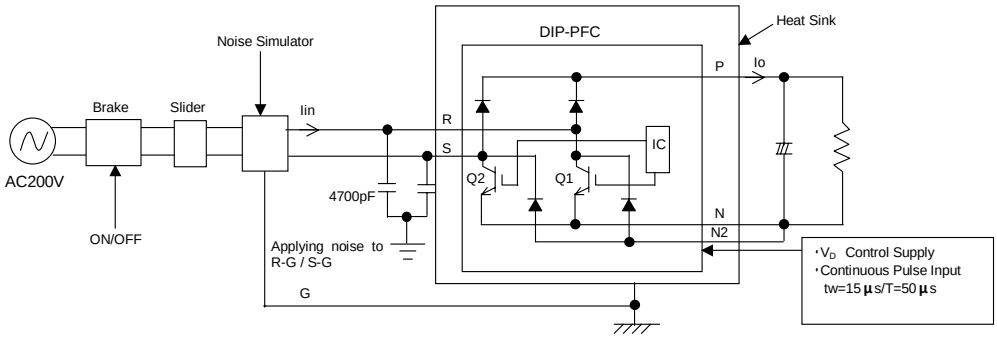


Fig. 16 Common noise evaluation circuit

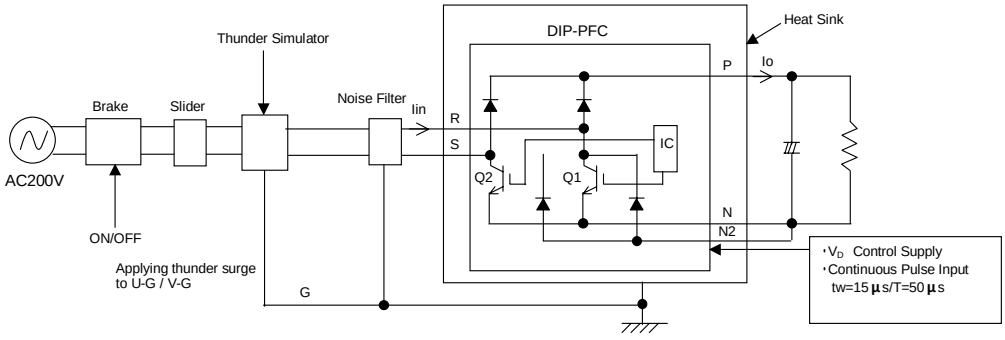
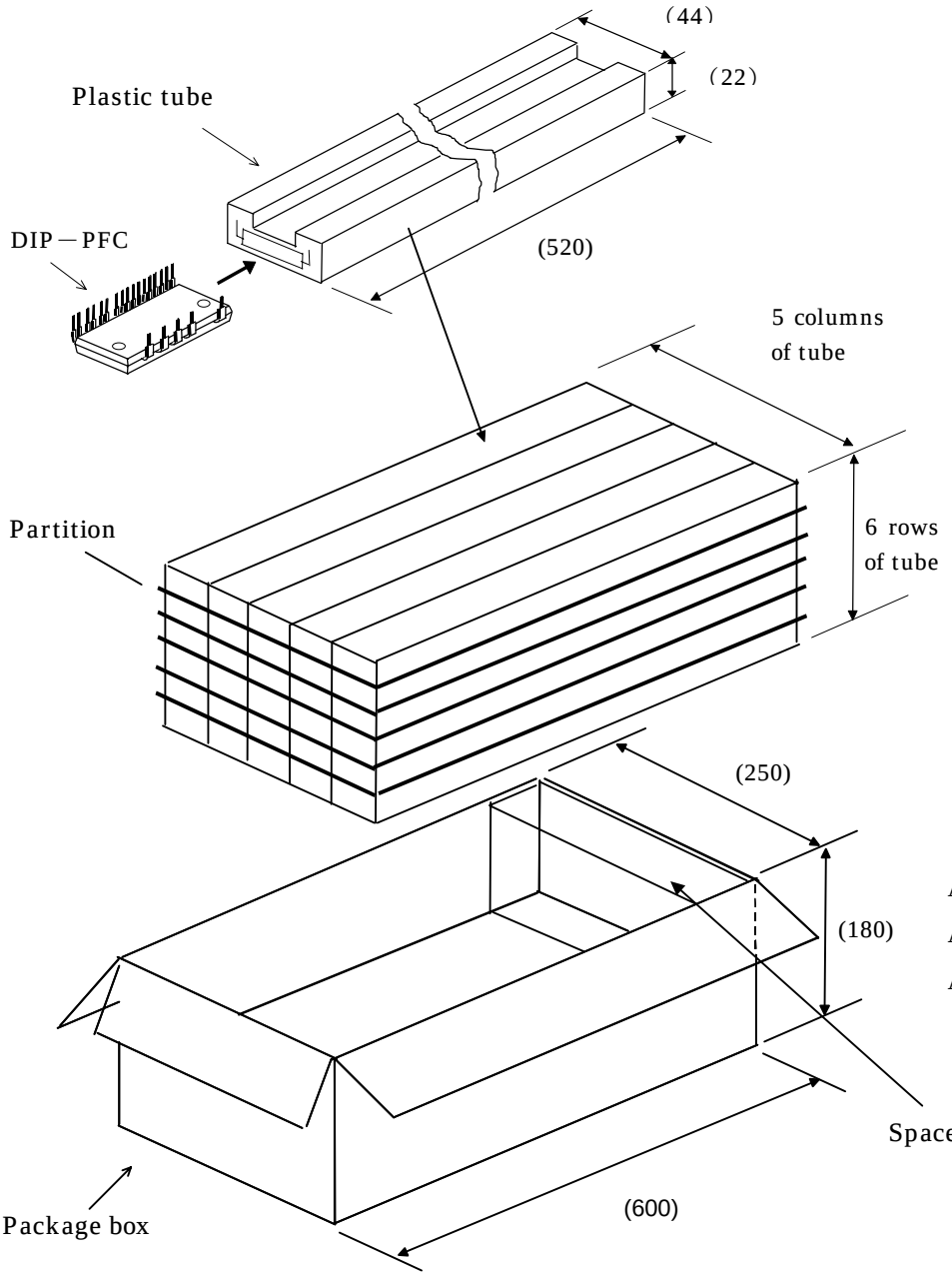


Fig. 17 Thunder surge evalution circuit

CHAPTER 5 ADDITIONAL GUIDELINES

5.1 Packaging Specifications



Per tube

6 pieces of DIP-PFC per tube

Per package box (Max.)

Total number of tubes is 30.
(5 columns×6 rows)

Total number of DIP-PFC is 180.
(30 tubes×6 pieces)

Weight

Approximately 54g ／Per DIP－PFC

Approximately 420g／Per tube

Approximately 14kg ／Per package

The above weights are ones when the maximum number of DIP-PFC is packaged.

Fig. 18 DIP-IPM Packaging Specification

5.2 Handling Precautions

Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend room temperature and humidity in the ranges 5～35℃ and 45～75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Disposal	・The epoxy resin and the case materials are made of approved products in the UL standard 94-V0, still they are incombustible.
Static electricity	・Exclusive ICs of MOS gate structure are used for the DIP-PFC power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1) Notice of breakdown by static electricity Excessively high voltage (over the Max. rated input terminal voltage) resulting from the static electricity of human bodies and packaging materials, might cause the modules to be damaged if applied on the control terminals. For countermeasures against static breakdown, it is important to control the static electricity as much as possible and when it exists, discharge it as soon as possible. ＊Do not use containers which are easy to be electro-staticly charged during transportation. ＊Be sure to short the control terminals with carbon cloth, etc. just before using the module. Also, do not touch between the terminals with bare hands. ＊During assembly (after removing the carbon cloth, etc.), earth machines used and human bodies. We suggest putting a conductive mat on the surface of the operating table and the surrounding floor. ＊When the terminals on the printed circuit board with mounted modules are open, the modules might be damaged by static electricity on the printed circuit board. ＊When using a soldering iron, earth its tip. (2) Notice when the control terminals are open ＊When the control terminals are open, do not apply voltage between the collector and emitter. ＊Short the terminals before taking a module off.

Appendix

Specific Control IC for DIP-PFC

TENTATIVE

A.1 M81012FP (*Under Development*)

A.1.1 Introduction

M81012FP is an integrated circuit specially developed for the control of DIP-PFC. It is designed in a standard 24-pin SSOP outline as shown in Fig. 19.

A.1.2 Feature

- Automatically synchronizing to the AC input supply, and generating referenced sinusoidal current waveform (50/60Hz);
- Voltage over-shot restraint function in light load (OV1)
- Soft start function
- Built-in protective function
  - −Over Voltage protection (OV2)
  - −Over Current protection (OC) by using external shunt resistor

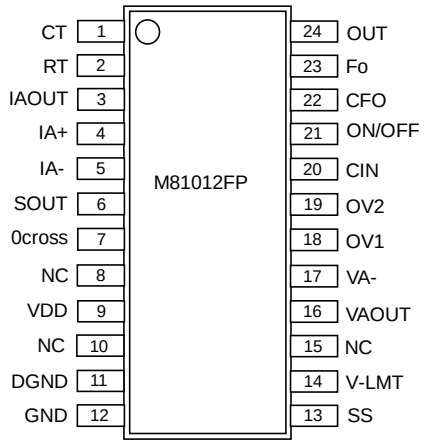


Fig.19 Pin Arrangement of M81012FP

A.1.3 Pin Arrangement and Description

No.	Symbol	Content
1	CT	The oscillator frequency is determined by the potential of middle point of RC, the frequency can be set in the range of 10kHz～50kHz
2	RT	
3	IAOUT	Current error amplifier output
4	IA+	Current error amplifier input, referenced current signal
5	IA-	Current error amplifier input, actual current signal
6	SOUT	Referenced standard sinusoidal current
7	0cross	Zero cross signal input, synchronized to AC voltage
8	NC	Null
9	VDD	Positive terminal of 5V power supply
10	NC	Null
11	DGND	GND terminal of IC, please make it short circuit to the GND (No.12 pin)
12	GND	GND of 5V power terminal
13	SS	Terminal for setting soft start time
14	V-LMT	Terminal for setting current limit in soft start operation
15	NC	Null
16	VAOUT	Voltage error amplifier output
17	VA-	Voltage error amplifier input, from DC output voltage signal
18	OV1	Voltage overshot restraint at light load, from DC output voltage signal
19	OV2	Over Voltage protection terminal, from DC output voltage signal
20	CIN	Over current protection terminal, input from shunt voltage signal
21	ON/OFF	Input terminal of ON/OFF signal for DIP-PFC start/stop control
22	CFO	Fault signal output pulse width setting terminal
23	Fo	Fault signal output terminal
24	OUT	PWM output for IGBT gate drive, connected to DIP-PFC Vin Terminal

A.1.4 Maximum Ratings (Ta=25℃)

No.	Item	Symbol	Rating	Unit	Note
1	Supply Voltage	V_{DD}	-0.3～+6.5	V	V_{DD} (Typ.)=5V
2	Input Operating Voltage	Vi	-0.3～V_{DD}+0.3	V	
3	Output Voltage	V_O	-0.3～V_{DD}+0.3	V	
4	OSC Frequency Capability	f_{OSC}	100	kHz	Typical value=20kHz
5	Fo Output Current	I_{FO}	+15	mA	
6	Operating Temperature	Topr	-20～80	℃	

A.1.5 Interface Circuit Example

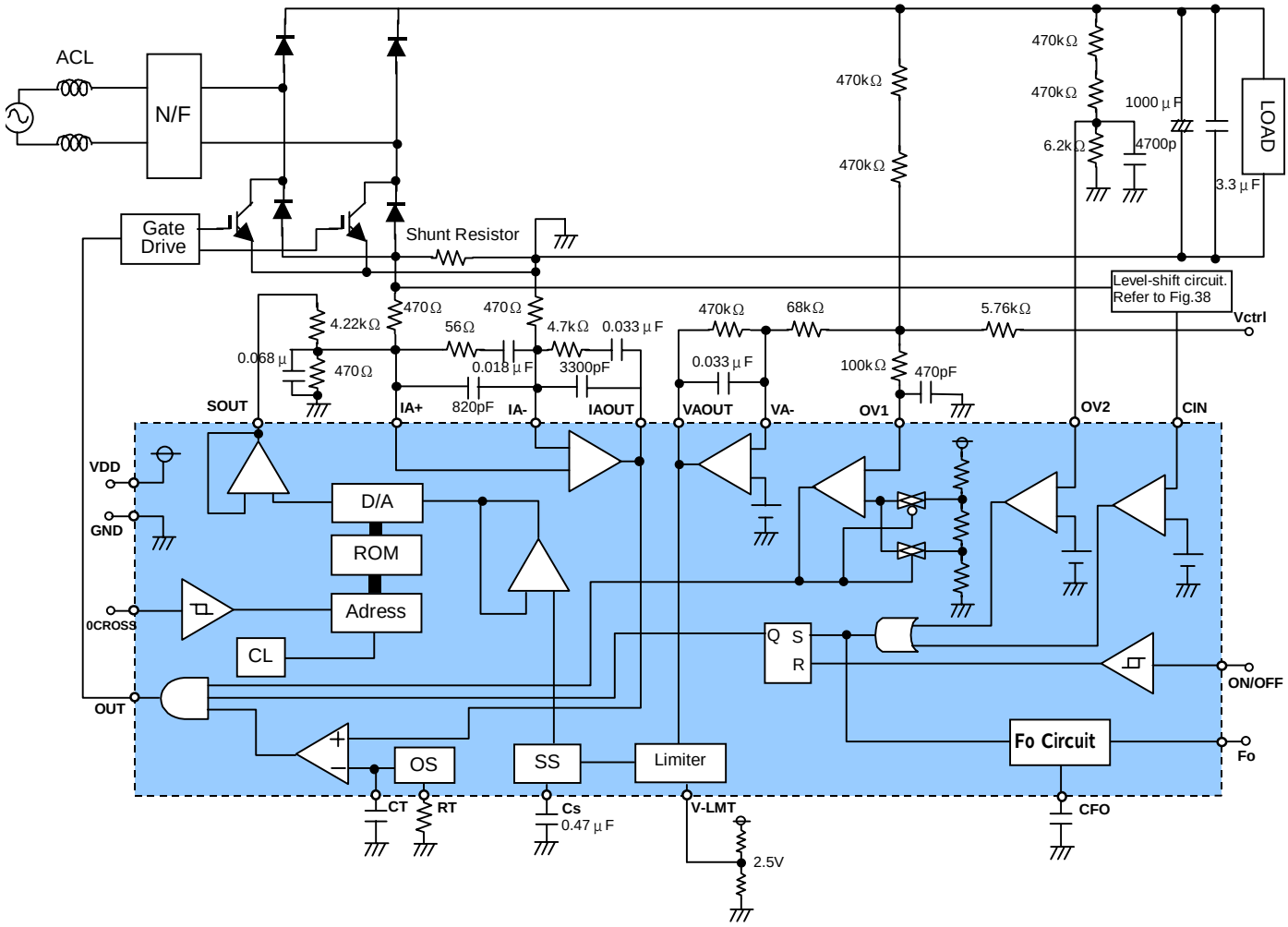


Fig. 20 Example of evaluation circuit using M81012FP

A.2 M63914FP

A.2.1 Introduction

M63914FP is a semiconductor integrated circuit specifically developed for the control of active filter. Fig. 19 shows its package outline of 36-pin SSOP.

A.2.2 Features

- Voltage overshot restraint function (OV1)
- Soft start function (SS1)
- Built-in protective functions
  - −Over voltage protection (OV2)
  - −OC/SC protection by using external shunt resistor
  - −Control voltage under voltage protection (UV)
  - −Over temperature (OT)

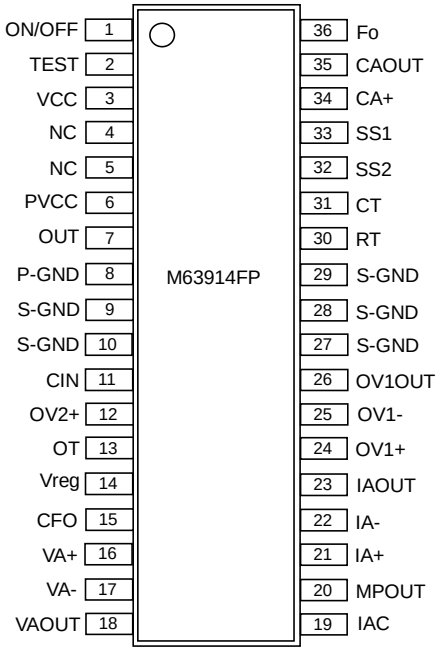


Fig. 21 Pin Arrangement of M63914FP

A.2.3 Terminal Arrangement and Description

No.	Symbol	Content
1	ON/OFF	Input terminal of DIP-PFC operation start signal
2	TEST	Test terminal, please shorten it to the GND in actual use
3	Vcc	15V control supply
4	NC	Null
5	NC	Null
6	PVcc	Power supply terminal for control output
7	OUT	PWM Output terminal for IGBT gate drive
8	P-GND	Shorten to GND
9	S-GND	Shorten to GND
10	S-GND	Shorten to GND
11	Cin	Over current protection terminal, input from shunt voltage signal
12	OV2	Over Voltage protection terminal, from DC output voltage signal
13	OT	Output terminal for over temperature
14	Vreg	IC internal regular supply
15	CFO	Fault signal output pulse setting terminal
16	VA+	Voltage error amplifier input, reference voltage
17	VA-	Voltage error amplifier input, from DC output voltage signal
18	VAOUT	Voltage error amplifier output, connected to the multiplier input
19	Iac	Multiplier input, actual current signal
20	MPOUT	Multiplier output, connected with IA+ terminal
21	IA+	Current error amplifier input, Referenced sinusoidal current signal
22	IA-	Current error amplifier input, Actual current signal
23	IAOUT	Current error amplifier output
24	OV1+	Voltage error amplifier input, form DC output voltage
25	OV1-	Voltage error amplifier input, form DC output voltage
26	OV1OUT	Voltage error amplifier output, used for voltage overshot control
27	S-GND	Connect to GND

28	S-GND	Connect to GND
29	S-GND	Connect to GND
30	RT	The oscillator frequency is determined by the potential of middle point of RC, the frequency can be set in the range of 10kHz～50kHz
31	CT	
32	SS2	Referenced voltage generating terminal
33	SS1	Used for soft start time setting (0.1μF for about 1sec)
34	CA+	Buffer for control signal input
35	CAOUT	Buffer for control signal output
36	Fo	Fault output terminal

A.2.4 Maximum Ratings (Ta=25℃)

No.	Item	Symbol	Rating	Unit	Note
1	Supply Voltage 1	V_{DD}	-0.2～+20	V	V_{DD} (Typ.)=15V
2	Supply Voltage 2	PV_{DD}	-0.2～V_{DD}+0.2	V	
3	Output Voltage	V_{OUT}	-0.2～V_{DD}+0.2	V	
4	Output Current	I_{OUT}	±1	A	
5	OSC Frequency Capability	f_{OSC}	50	kHz	Typical value=20kHz
6	Fo Output Current	I_{FO}	+15	mA	
7	Operating Temperature	Topr	-20～80	℃	

A.2.5 Interface Circuit Example

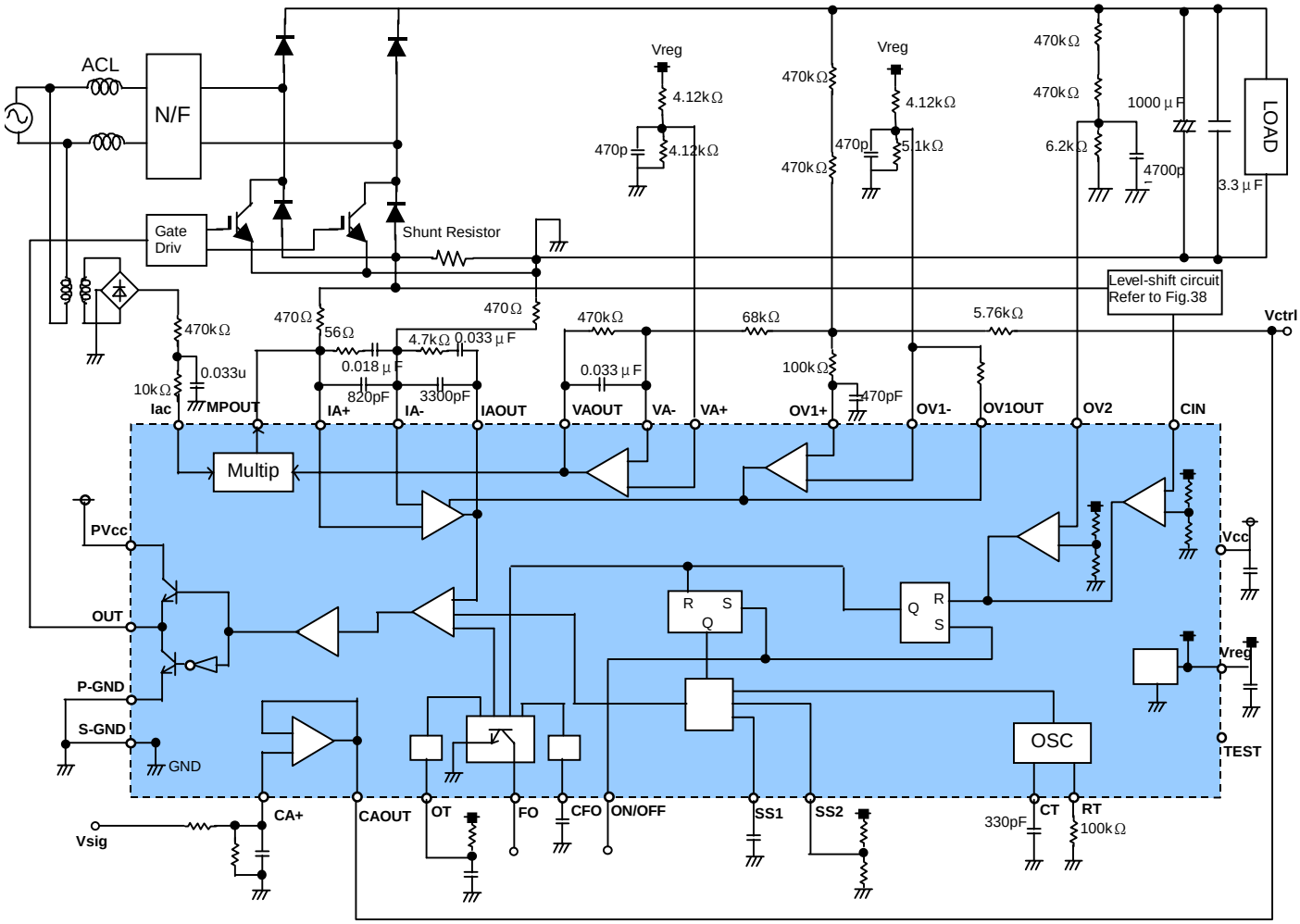


Fig. 22 Example of evaluation circuit using M63914FP

A.3 Protective Function (M81012FP, M63914FP)

(1) Voltage Overshot Control Function (OV1)

Generally, the output voltage of a boost type active filter will rise greatly at a light load. OV1 is designed to restrain the overshot of the output voltage. When the voltage exceeds the defined value by about 20V, IGBT gate input will be blocked so that the further voltage rise can be restrained.

OV1 protection can be released automatically if the output voltage drops below the OV1 trip level.

(2) Over Voltage Protection (OV2)

IGBT gate input will be interrupted if the DC bus voltage exceeds the OV2 trip level. This can prevent the over voltage applying to the DC smoothing condenser and the load.

(3) Over Current / Short Circuit Protection (OC/SC)

The DC bus current is detected by using an external shunt resistor. If the current exceeds the SC trip level, IGBT gate input will be blocked to prevent DIP-PFC from over current destruction.

(4) Soft Start Function (SS)

This function is used to start the PFC softly so as to restrain the over current at start-up.

A.4 Fault Output Condition and Its Timing(M81012FP, M63914FP)

The control IC will assert an Fo signal when the following abnormal state is detected

- Over Voltage

Fault signal will output if the output voltage exceeds the OV2 trip level, and at the same time, IGBT operation will be stopped. Over voltage protection cannot be released automatically. To activate the DIP-PFC from an OV2 protection, please reset the ON/OFF signal once again.

- Over Current

Fault signal will output if the bus current exceeds the OC/SC trip level, and at the same time, IGBT operation will be stopped. Over current protection cannot be released automatically. To activate the DIP-PFC from a OC/SC protection, please reset the ON/OFF signal once again.

Note : For UV protection, IGBT gate will be interrupted when control voltage drops below the UV trip level, and the protection will be released automatically if the control voltage recovers to the UV reset level. Because UV protection is realized by the LVIC instead of the control IC in M81012FP, Fo signal will not be asserted by the control IC. However, Fo will be asserted by M63914FP.

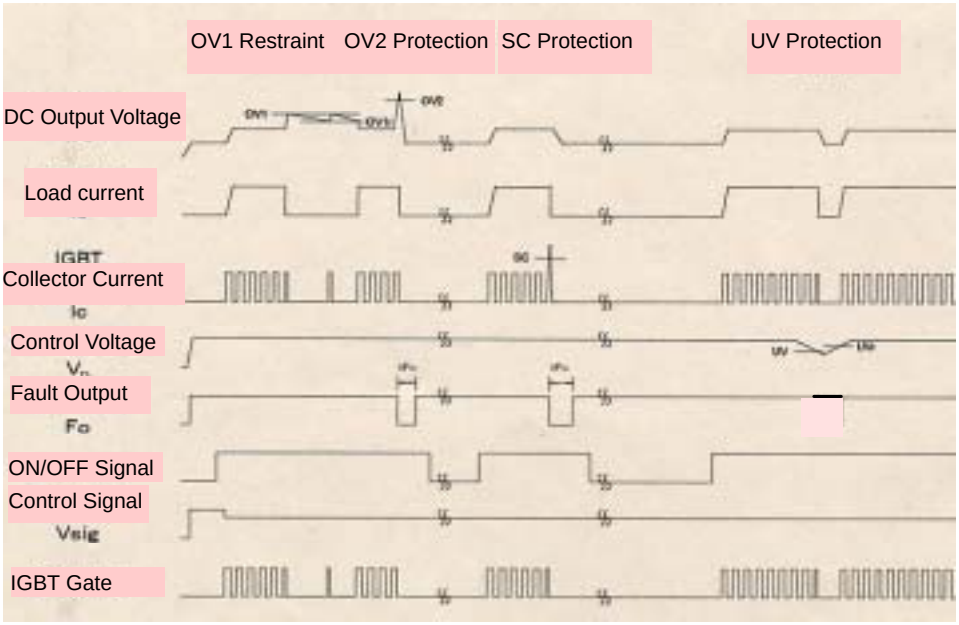


Fig.23 Fault output timing chart.

A.5 Example of Interface Circuit Design

(1) PFC ON/OFF Circuit (M81012FP, M63914FP)

The start-up and stop operation of DIP-PFC is controlled by the ON/OFF command usually from a MCU. The ON/OFF control is high active. Fig. 24 shows an interface circuit. It consists of two transistors for level shift. Also, a hard interruption circuit is realized synchronously to the Fo signal coming from DIP-IPM. It is necessary to consider the parameter dispersion of the total resistors in designing the circuit.

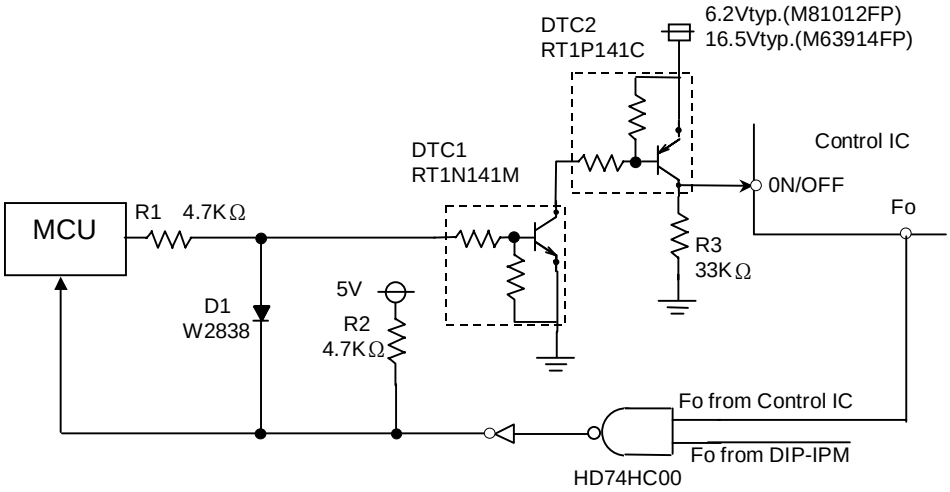


Fig. 24 ON/OFF circuit

・PFC ON

The internal circuit of ON／OFF terminal connecting to a comparator, therefore, current cannot flow into this terminal. Hence, the collector current of DTC2 can only flow on the resistor R3. Please control the DTC2 base current so that the voltage drop of R3 is within the IC on threshold range of 2.4～2.6V.

・PFC OFF

To stop PFC, the base of DTC1 should be set to low by the MCU. In addition, If the Fo output of DIP-IPM becomes low, the base of DTC1 will also become low due to clamp of the diode D1. Therefore, DTC1 as well as DTC2 will be turned off, and PFC will be stopped.

(2) Carrier Frequency Setting Circuit (M81012FP, M63914FP)

The carrier frequency of the IC can be arbitrary set by using the external resistor Rt and the condenser Ct. To make the PFC work most effectively, it is recommended that the carrier frequency to be set to 20～25kHz.

Carrier frequency can be determined as follows:

$$Ict = Vrt / Rt$$

Where Ict is the current flows on the condenser, and Vrt the reference voltage of internal oscillator.

The ON and OFF time can be calculate by using the upper and lower threshold value Vosch, Voscℓ of the oscillator,

$$Ton = Toff = (Vosch - Vosc\ell) \times Ct / Ict$$

Therefore, the carrier frequency can be got from

$$f_{PWM} = 1/(Ton + Toff)$$

As for MP81012FP, Vrt=1.73V, Vosch=3.0V, Voscℓ=1.7V.

Suppose RT=100kΩ, CT=330PF, then

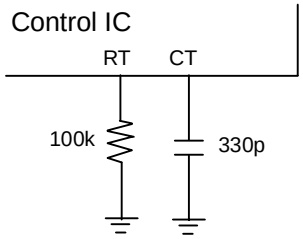


Fig. 25 Carrier frequency setting circuit

Ton=Toff= (3.0－1.7) ×330P／ (1.73／100k) =24.8 (μsec)

f_{PWM}=1/ (Ton＋Toff) =20.16kHz

(3) Soft Start Setting Circuit (M81012FP, M63914FP)

The DC voltage will be overshot easily if starting-up the PFC at the condition of a very low bus voltage. To restrain the peak value of voltage overshot, the control IC provide the soft start function, which starts the PFC slowly so that the voltage rises softly to the demand value.

The soft start time is determined by the condenser connected to the SS terminal as shown in Fig.26. The relationship between the soft start time and the capacitance is as follows:

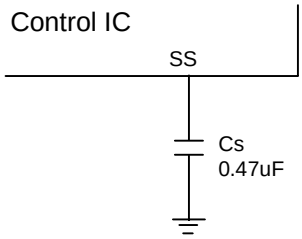


Fig. 26 Soft start setting circuit

Ts=3.25×10^5×Cs (s)　for M81012FP

Ts=1.83×10^5×Cs (s)　for M63914FP

For you reference, from the internal circuit constant, the voltage overshot becomes zero if the DC voltage control signal varies from 5V (PFC off) to 1.14V (300V) within 500ms. In actual use, the capacitance should be determined by according to the allowable maximum overshot and available mounting space for the condenser of the application system.

(4) Current Limitation Setting Circuit (M81012FP)

The control IC provide the current limitation function for soft start operation. The demanded current level can be set by the reference voltage of the V-LMT terminal, as shown in Fig. 27

Limited current (A) ＝$V_{(V\text{-}LMT)}$×20 (A/V)

Note 1: The control IC might not make response if the V-LMT voltage is under 1.0V.

Note 2: If the referenced voltage is obtained by using resistor division, please pay attention to the resistance dispersion and temperature characteristics of the resistors.

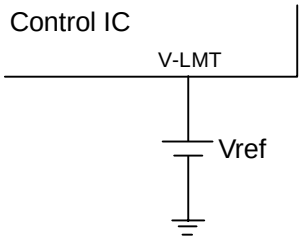


Fig. 27 Current limit setting circuit

(5) DC Voltage Control Circuit (M81012FP, M63914FP)

Because DIP-PFC is a boost type active converter, it is necessary to ensure the DC bus line voltage to be higher than the maximum peak value of the AC input voltage with a merging of about 30V. The DC output voltage is set by a microprocessor or a hardware circuit instead of the control IC. Figure 28 shows the relationship of DC output voltage versus the voltage command value. For reference, Vdc=300@Vctrl=1.04V. The maximum DC voltage should not be larger than the over voltage trip level..

The DC voltage setting circuit is shown in Fig. 29. The desired voltage is kept by the voltage feedback to the error amplifier in the control IC.

The DC voltage can be calculated as follows:

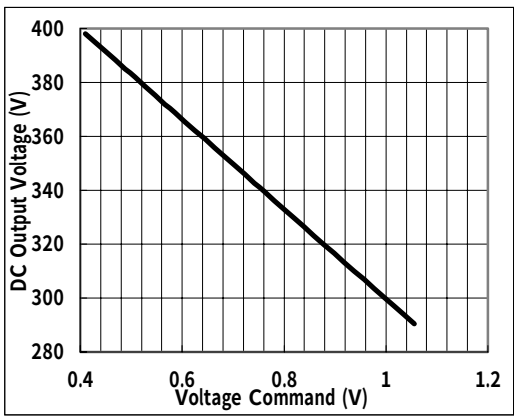


Fig. 28 DC voltage via command value

Vdc=Vctrl+ ((Vreg－Vctrl) * (R1+R2)) /R1

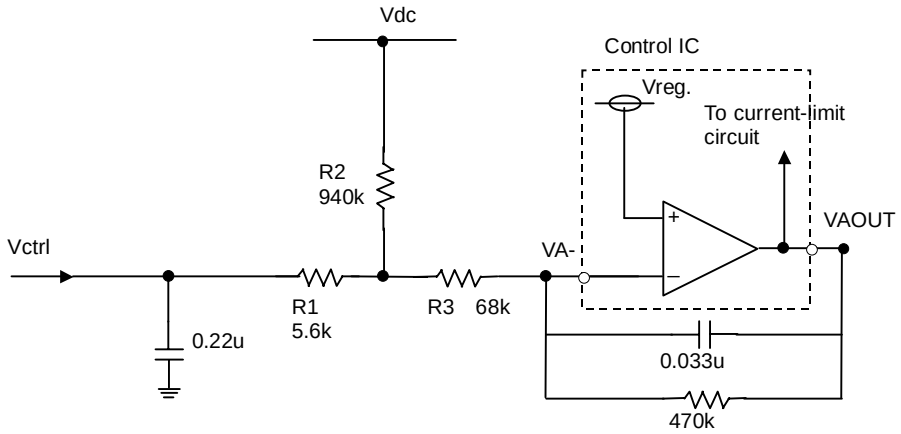


Fig. 29 DC output voltage setting circuit

(6) Zero Cross Capturing Circuit (M81012FP)

The control IC captures the zero cross point of AC input voltage, and generates the referenced sinusoidal current waveform with the internal digital/analog circuit. Figure 30 shows the zero cross capturing circuit. Opto-coupler is used to isolate the power side and the control side. The zero cross input to the control IC is pulse signal.

When a forward AC voltage is applied, PC1 turns on and current flows on the primary side. DTC1 also turns on because its base becomes low due to pull-down of R2. The 0cross input becomes high due to the R4.

On the other hand, when a reverse AC voltage is applied, the current is bypassed by diode D1, and the opto-coupler turns off. DTC1 also turns off, which leads to a low input to the 0cross terminal.

Therefore, it is understood that a high level zero cross signal corresponds to the positive waveform, and a low signal corresponds to a negative waveform of the AC input voltage.

The zero cross pulse signal might be not so precisely synchronized to the Ac input voltage because of the on/off threshold value of the opto-coupler and the inherent delay of the circuit. Please make compensation to the delay if necessary.

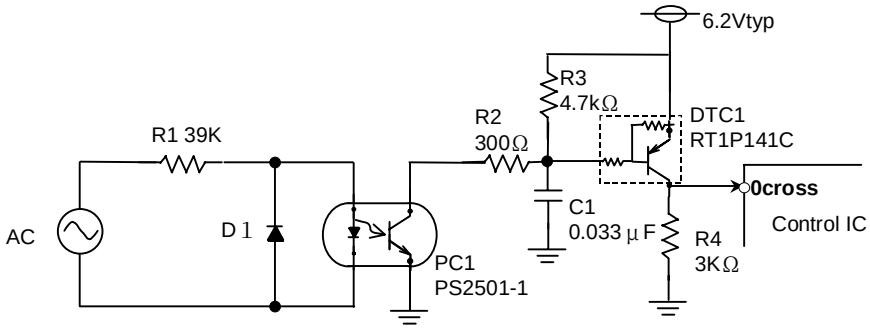


Fig. 30 Zero cross capturing circuit

(7) Referenced Sinusoidal Current Generating Circuit (M81012FP)

The control IC generates the referenced sinusoidal current waveform by the internal digital/analog circuit based on the detected zero cross signal and the demand current amplitude.

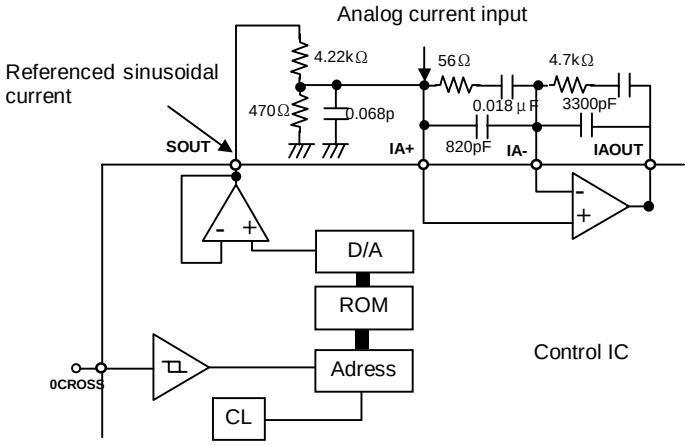


Fig. 31 Referenced sinusoidal current generating circuit

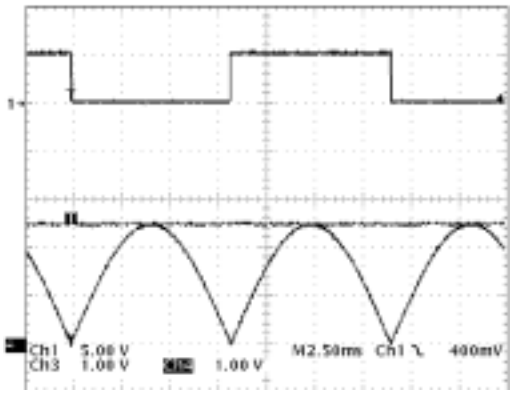


Fig. 32 Signal waveforms

Note: The PWM on pulse width becomes small when the AC input current phase is near 90 ° . The output of the voltage error amplifier comes to the peak values of the triangular carrier, as shown in Fig. 33. Therefore, IGBT on pulse is easily imposed by noise, which makes the output of SOUT unstable. If the output voltage of the error amplifier becomes smaller than the minimum value of the carrier, on pulse will not be generated and IGBT will not turns on.
A countermeasure to the problem is to connect a bypass film condenser to the SOUT terminal to filter the noise.

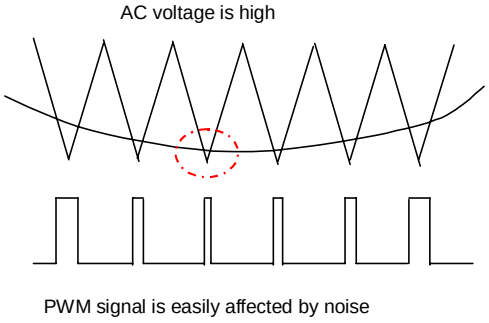


Fig. 33 Noise interference

For M63914FP, please input the AC current signal to Iac terminal (input of the multiplier) as shown in Fig. 22.

(8) Voltage Error Amplifier Interface Circuit (M81012FP, M63914FP)

The internal error amplifier compares the actual voltage Vdc and the demanded signal Vctrl, and regulate the PWM duty so as to keep the DC voltage to the demanded value. However, error might happens because of the dispersion of the circuit constants. Please make compensation if necessary.

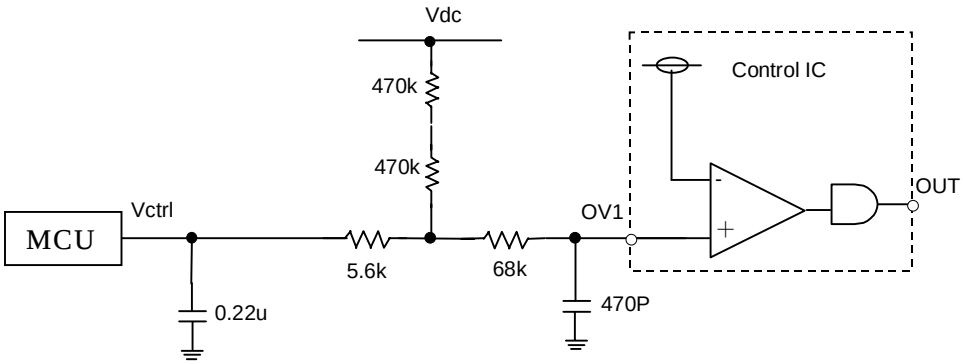


Fig. 34 Voltage error amplifier circuit

(9) Current Error Amplifier Interface Circuit (M81012FP, M63914FP)

The internal error amplifier compares the actual bus current with the referenced sinusoidal current, and regulates the PWM duty so as to make the actual current follow the referenced one. The output of the error amplifier is compared to the triangular carrier wave, and the result is then sent to DIP-PFC control input. If the wiring of this signal line is too long, noise maybe imposed on it, and result malfunction of DIP-PFC.

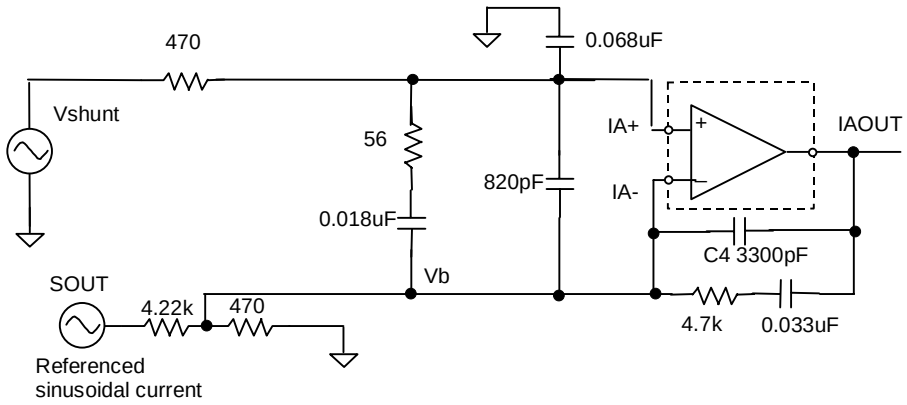


Fig. 35 Current error amplifier circuit

(10) Fault Output (Fo) Circuit (M81012FP, M63914FP)

The control outputs an Fo signal when there is a on over voltage or over current in the DIP-PFC. Since Fo terminal is open collector type, it is necessary to pull it up to 5V logic supply through a resistor of about 4.7 kΩ The electric characteristics of terminal is as follows:

Item	Code	Condition	Rating	Unit
Fo output voltage	$V_{FO(L)}$	$I_{FO(L)}$=10mA in operation	1.0max	V

Please ensure that $I_{FO(L)}$ will not exceed 10mA.

The operation of DIP-PFC will be interrupted by the circuit shown in Fig.24, however, to make the system fail-safe against noise, please also stop the PWM output of the microprocessor. In DIP-PFC/DIP-IPM system, although DIP-IPM can work with only a pure diode rectifier bridge, it is better to stop the total system by software in case there is Fo output either from DIP-PFC or DIP-IPM. In addition, a noise filter is recommended in the circuit. The time constant should be determined according to actual application condition.

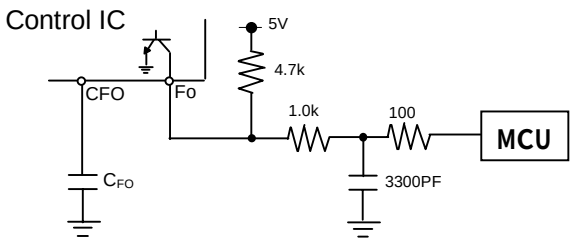


Fig. 36 Fo output circuit

The Fo output pulse width is determined by the condenser connected to the CFO terminal.
(Example: C_{FO}=22nF ⇒ t_{Fo}=1.8ms (typ.))

(11) Over Voltage detecting Circuit (M81012FP, M63914FP)

There are two over voltage control functions (OV1, OV2) in the control IC. OV1 is used for the restraint of voltage overshot in light load, it will not latch-up and can recover to normal state if the OV1 lock is released. OV2 is used for the protection DIP-PFC from over voltage destruction, it will stop the DIP-PFC and keep the latch-up state. The control IC outputs Fo only an OV2 failure is detected.

The over voltage detecting circuit of OV2 is shown in Fig.36. The DC bus voltage signal is obtained by the division of resistors, and is compared with the fixed reference voltage by the internal error amplifier. If the

DC voltage exceeds the setting value, the error amplifier will output a latch signal to the OV2 protection circuit to stop the DIP-PFC.

To prevent malfunction due to noise, a noise filter with a time constant of about 2 μs is recommended.

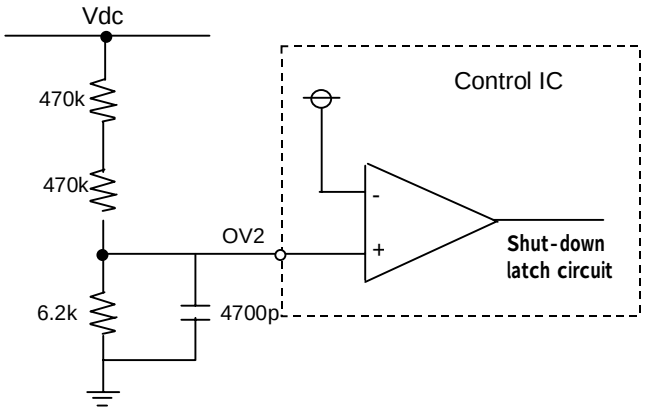


Fig. 37 Over voltage detecting circuit

(12) PFC Over Current Detecting Circuit (M81012FP, M63914FP)

The PFC DC bus line current is detected by using a shunt resistor. The detected current signal is transferred to the control IC with the circuit shown as Fig. 38

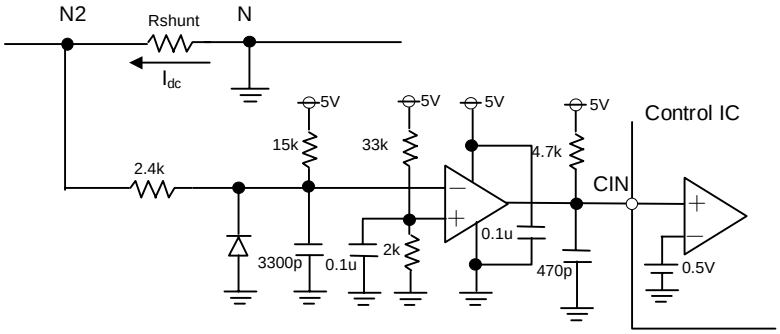


Fig. 38 Current detecting circuit

The maximum value of over current should be set below the 1.7 times of the IGBT current rating. In addition, please set the RC filter constant to 1.5～2.0 μsec so as to shut down PFC quickly in case of a over current.

Application Note	Prep.		Rev.				
	Apr.						

Notice for Safe Designs

- We are making every effort to improve the quality and reliability of our products. However, there are possibilities that semiconductor products be damaged or malfunctioned. Pay much attention to take safety into consideration and to adopt redundant, fireproof and malfunction-proof designs, so that the breakdown or malfunction of these products would not cause accidents including human life, fire, and social damages.

Notes When Using This Specification

- This specification is intended as reference materials when customers use semiconductor products of Mitsubishi Electric. Thus, we disclaim any warranty for exercise or use of our intellectual property rights and other proprietary rights regarding the product information described in this specification.
- We assume absolutely no liability in the event of any damage and any infringement of third party's rights arising from the use of product data, diagrams, tables, and application circuit examples described in this specification.
- All data including product data, diagrams, and tables described in this specification are correct as of the day it was issued, and they are subject to change without notice. Always verify the latest information of these products with Mitsubishi Electric and its agents before purchase.
- The products listed in this specification are not designed to be used with devices or systems, which would directly endanger human life. Should you intend to use these products for special purposes such as transportation equipment, medical instruments, aerospace machinery, nuclear-reactor controllers, fuel controllers, or submarine repeaters, please contact Mitsubishi Electric and its agents.
- Regarding transmission or reproduction of this specification, prior written approval of Mitsubishi Electric is required.
- Please contact Mitsubishi Electric and its agents if you have any questions about this specification.