Samsung S3C2412

Mobile computing oriented Application processor for PDA, Car navigation and general application

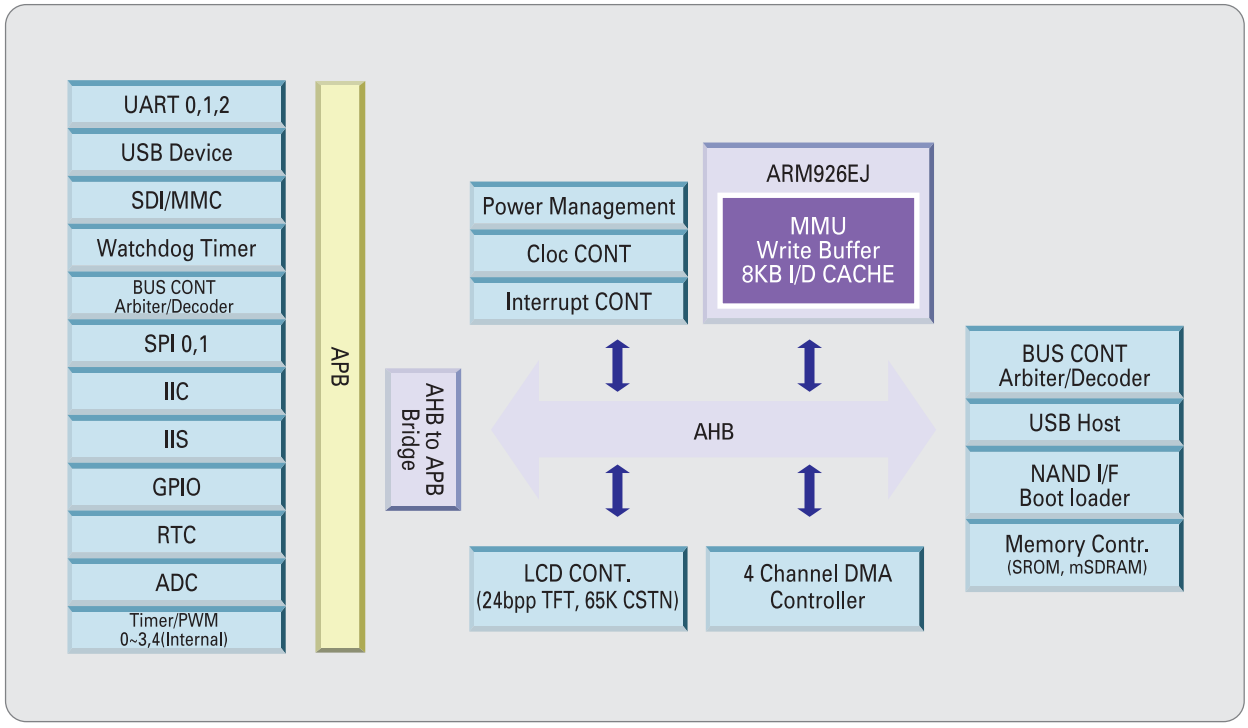
Product Brief

S3C2412 is a Derivative product of S3C2410A. S3C2412 is designed to provide hand-held devices and general applications with cost-effective, low-power, and high-performance micro-controller solution in small die size.
To reduce total system cost, the S3C2412 includes the following components separate 8KB Instruction and 8KB Data Cache, MMU to handle virtual memory management, LCD Controller (65K CSTN & TFT), NAND Flash Boot Loader, System Manager (chip select logic and SDRAM Controller), 3-ch UART, 4-ch DMA, 4-ch Timers with PWM, I/O Ports, RTC, 8-ch 10-bit ADC and Touch Screen Interface, IIC-BUS Interface, IIS-BUS Interface, USB Host, USB Device, SD Host & Multimedia Card Interface, 2-ch SPI and PLL for clock generation.

S3C2412 was developed using an ARM926EJ-S core, 0.13um CMOS standard cells and a memory complier. Its low-power, simple, elegant and fully static design is particularly suitable for cost- and power-sensitive applications. It adopts a new bus architecture called Advanced Microcontroller Bus Architecture (AMBA).

S3C2412 offers outstanding features with its CPU core, a 16/32-bit ARM926EJ-S RISC processor designed by Advanced RISC Machines, Ltd. The ARM926EJ-S implements MMU, AMBA BUS, and Harvard cache architecture with separate 8KB instruction and 8KB data caches, each with an 8-word line length.

Block Diagram



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Feature

ARM926EJ-S CPU Core
- 64-way set-associative cache with I-Cache (8KB) and D-Cache (8KB)
- Write through or write back cache operation
- ARM's Jazelle Java technology enhanced ARM architecture
- MMU to support WinCE, Symbian and Linux

System Manager
- Address space: 128M bytes for each bank (total 1G bytes)
- Little/Big Endian support
- Eight memory banks:
  - Six memory banks for ROM, SRAM, and others
  - Two memory banks for SDRAM
  - Mobile SDRAM Interface
  - 100/133MHz address and command bus speed
  - Supports a synchronous static memory-mapped devices including RAM, ROM and flash
- Nand Flash Bootloader

Operating Conditions
- Internal: 1.2V
- External I/O: 3.3V
- Speed: 200MHz @ 1.2V
  266MHz @ 1.4V
- Memory : 1.8V/2.5V/3.0V memory,

On-chip Peripherals
- Power management
  : Normal, Idle, stop, and sleep mode
  *Idle mode: The clock for only CPU is stopped.
  Stop mode: All clocks are stopped.
  Sleep mode: The Core power including all peripherals is shut down.
- ATA Interface
- 2-port USB Host /1- port USB Device
- 4-ch DMAs with external request pins
- 3-ch UART
- 2-ch SPI
- Watch Dog Timer
- 1ch multi-master IIC-BUS/1-ch IIS-BUS controller
- 115-bit GPIO Ports /24-ch external interrupt source
- LCD controller (up to 65K color STN and 256K color TFT) with 1-ch LCD-dedicated DMA
- SD Host interface version 1.0 & Multimedia Card Protocol version 2.11 compatible
- 4-ch PWM timers & 1-ch internal timer
- 8-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- On-chip clock generator with PLL

Package
- 272-FBGA 14 x 14

Benefits

- Low-power and Cost-effective Solution
- Built-in NAND Flash Boot loader
- Various Embedded IPs
- Various Design applications

Key Applications

- PDA/Smart Phone
- Car Navigation
- POS terminal
- Portable Game Player

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