Application Report
SLVA103 - July 2001

Comparing Performance of Current Ramp and Voltage Ramp Hot Swap Controller ICs

Bang S. Lee — *Power Management*

ABSTRACT

This application note addresses the current ramp and voltage ramp performance characteristics of hot swap controller ICs. It discusses practical aspects of applying current ramp or voltage ramp and presents a comparison of performance.

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1 Introduction

Hot swap is the ability to safely insert a module into or remove it from a host system without first interrupting power to the host. This feature is generally designed in wherever a need exists to replace modules on the fly. Such a requirement may be for purposes of repair, reconfiguration, redundancy, or system upgrade. Hot swap is useful in systems with high availability requirements such as PCI, Compact PCI, USB, 1394, and telecom/datacom applications.

Hot swap design considerations must be addressed early in the system design program to achieve the desired high availability feature required by the application. The design considerations address a number of phenomena that occur with live insertion and removal events. These phenomena include contact bounce, arcing between connector pins, and large voltage and current transients. The most important hot swap phenomena concerns are to reduce inrush current and to avoid input voltage droop when a discharged capacitive load add-in card is plugged in a live backplane.

Today's design engineers are faced with a variety of choices when selecting a protection hot swap IC to meet their system design requirements. It is very important to understand the exact requirements of the system before selecting a hot swap IC solution. Features on some hot swap ICs may not meet the high availability system requirements under certain system power conditions. By fully understanding the system implementation requirements and the function of the available hot swap ICs, a proper hot swap solution can be selected to meet the high availability system needs.

Texas Instruments (TI) has developed a variety of hot swap IC solutions to meet high availability system requirements. TI provides a large number of hot swap ICs with a wide variety of features. Figure 1 shows the classification of the TI hot swap controller ICs. The TI hot swap IC controllers are classified as either current ramp (di/dt) or voltage ramp (dv/dt) controller ICs. TI current ramp and voltage ramp hot swap controller ICs are available with adjustable ramp and fixed ramp.

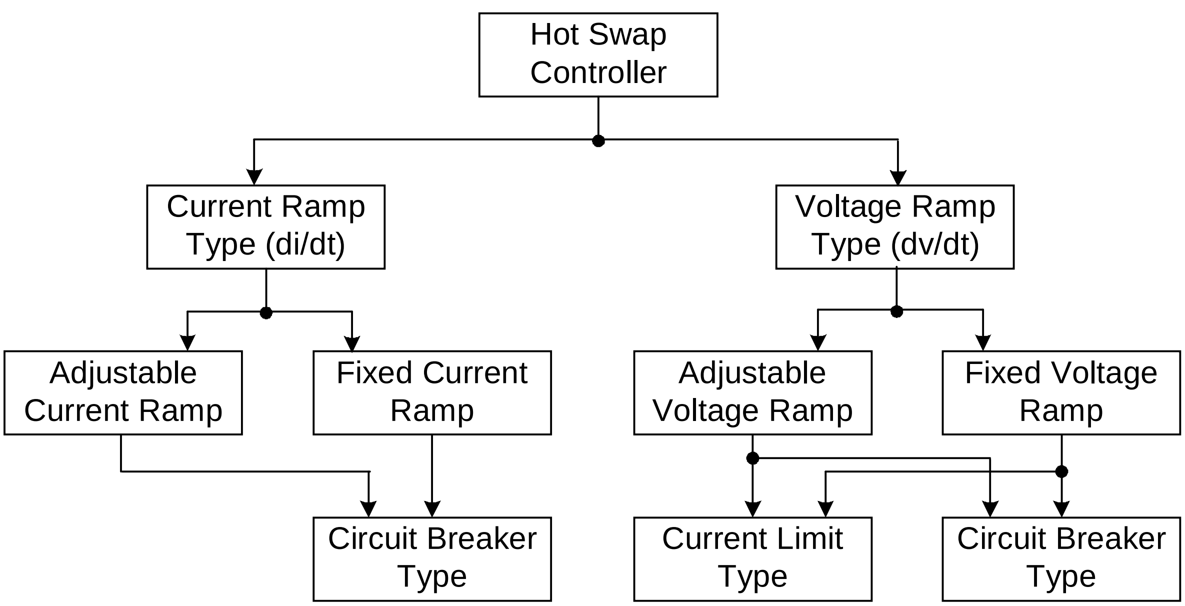


Figure 1. Classification of TI Hot Swap Controllers

This application note compares the current ramp (di/dt) and the voltage ramp (dv/dt) hot swap controllers UCC3919 and TPS2301 ICs, respectively. The comparison offers system designers understanding of the hot swap controller IC differences and assistance in selecting the proper hot swap IC for their system needs. The comparison is completed using the UCC3919 Evaluation Module (EVM) and the TPS2310 Evaluation Module (EVM) available from TI.

2 Principle Operation of Voltage Ramp Hot Swap Controller IC

Figure 2 shows the simplified equivalent circuit for a voltage ramp hot swap controller IC similar to the TPS2301. The ramp rate of the output voltage follows the gate voltage ramp rate without output voltage feedback. Therefore, the series pass element operates like a source-follower during ramp-up, and then it transits to a low impedance supply path for steady state operation. Output voltage ramp rate is roughly controlled by gate voltage.

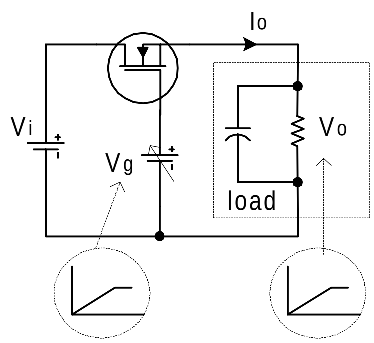


Figure 2. Equivalent Circuit of Voltage Type of Hot Swap Controller

$$\frac{dV_o}{dt} \propto \frac{dV_g}{dt} \tag{1}$$

Figure 3 illustrates that the output voltage is controlled to keep slew rates fixed using four different load capacitors (0 µF, 47 µF, 470 µF, and 940 µF). Note that the output current ramp rate on the TPS2301 is not controlled by the load capacitors but is determined by the load impedance as follows:

$$I_{o,inrush} = C_o \frac{dV_o}{dt} + \frac{V_o}{R_o} \quad \text{During start-up} \tag{2}$$

By using equation (2), the load capacitor and the voltage ramp rate determine the peak inrush current produced with the TPS2301. In most cases, the inrush current slew rate is not controllable with voltage ramp hot swap controllers. Figure 3 shows the inrush currents at a high peak current during start up. The inrush currents shown in Figure 3 may cause severe voltage droops below the power specifications at input terminal if an up-stream power supply does not have enough capacity to handle the sharp current demand. Larger load capacitors result in higher inrush peak currents.

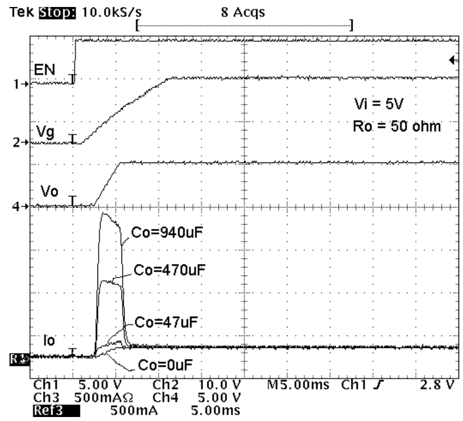


Figure 3. Voltage Ramp Hot Swap Controller (TPS2301-EVM) Inrush Currents

Most of the Texas Instruments voltage ramp controllers have a fixed ramp. However, the voltage ramp rate can be adjusted by placing an external capacitor between the gate of the MOSFET and ground. The voltage ramp time is proportional to the value of external capacitor.

2.1 Current Protections of Voltage Ramp Hot Swap Controllers

Two current protection technologies, current limit and circuit breaker, are available to limit the inrush current. Current limited controllers clamp the MOSFET output currents at a maximum peak value. The limiting current may cause a rise time delay of the output voltage due to a different charging time of output capacitor, resulting in slower slew rate of the output voltage than that of gate voltage. Circuit breaker types of controllers turn off the controller when the output current reaches a fault level and exceeds a programmed time interval. Figure 4 and Figure 5 illustrate the two types of current protection.

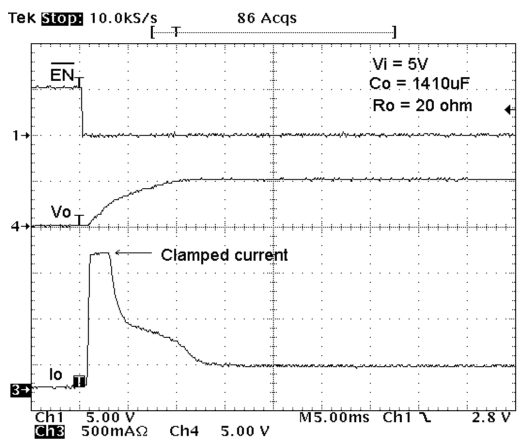


Figure 4. Current Limit Type of Voltage Ramp Controller (TPS2022-EVM)

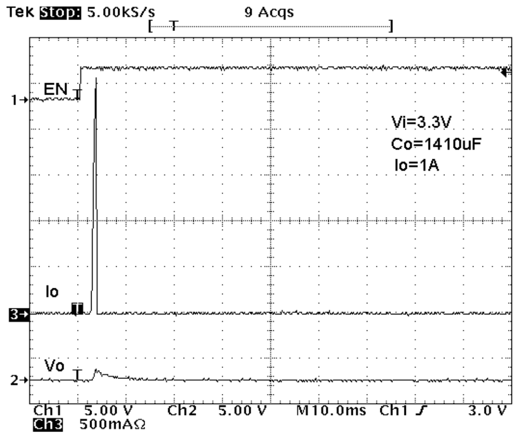


Figure 5. Circuit Breaker Type of Voltage Ramp Controller (TPS2301-EVM)

3 Principle Operation of Current Ramp Hot Swap Controller IC

The simplified equivalent circuit of current ramp controller is shown in Figure 6. The load current is typically sensed with a low value resistor and compared to a reference level, which generates a programmed slew rate of inrush current. The voltage divider (R1, R2) and a capacitor CIMAX generate a voltage ramp at the IMAX pin of TI current ramp controllers, which is used to control the output current. Basically, the resistor divider (R1 and R2) sets the output current limit. The inrush current ramp rate is determined by the time constant of R1, R2, and CIMAX. Most TI current ramp hot swap controllers have an external pin for IMAX, so users can program the inrush current slew rate using a time constant by external components (CIMAX, R1, and R2). The IMAX pin programs the maximum allowable sourcing current.

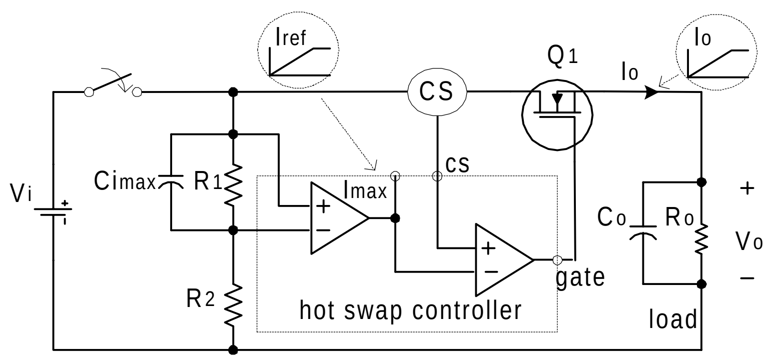


Figure 6. Simplified Equivalent Circuit of Current Ramp Hot Swap Controller IC

Figure 7 illustrates the programmed inrush current slew rates for Vi = 5V, Co = 47 µF, and Ro = 11 ohm. The inrush current slew rates are programmed by the time constant of R1 (5K ohm), R2 (100k ohm), and CIMAX (0.1 µF, 1 µF, and 10 µF). As CIMAX increases, the current slew rates reduce such that the inrush peak current mitigates, while the output capacitor charging time increases as shown in the figure. Figure 7 shows how an external CIMAX controls the inrush current. The corresponding output voltages are also shown.

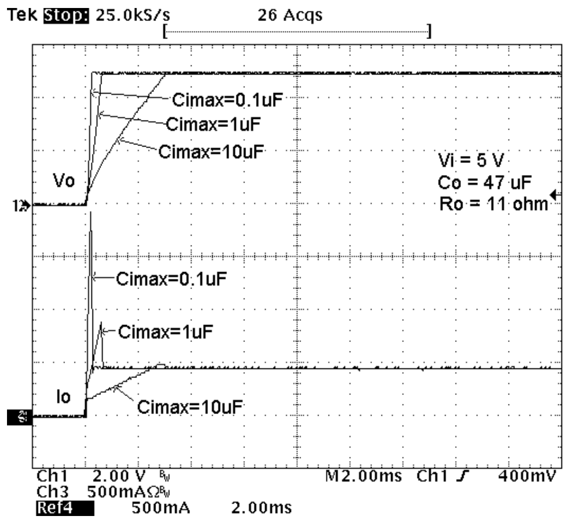
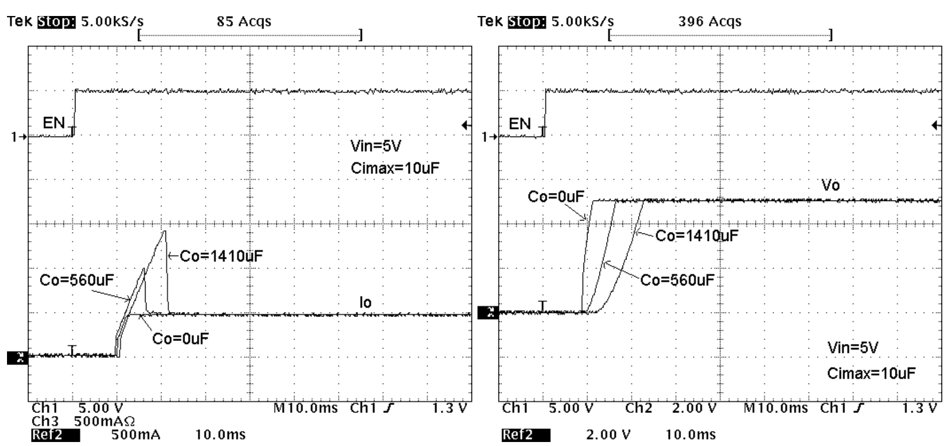


Figure 7. UCC3919-EVM (di/dt) Experimental Results With CIMAX = 0.1 µF, 1 µF, and 10 µF

3.1 Current Ramp Controllers With Various Output Capacitors and Load Currents

Figure 8 shows current ramp controller inrush current and the corresponding output voltage responses to three different load capacitors (0 µF, 560 µF, and 1410 µF). Since inrush current slew rate is programmed, it ramps up at a programmed fixed rate until the CIMAX capacitor is fully charged. Different charging times with the three capacitors produce different shapes of inrush current. Figure 9 shows inrush current responses to different load currents (Io = 1A, 1.8A, 2.5A, and 4.5A). Both Figure 8 and Figure 9 illustrate how current ramp controllers react to unknown load impedance. Regardless of the load conditions, the inrush current slew rates of current ramp controllers are controlled to keep a programmed rate, which is a good feature for current ramp controllers. It allows the hot swap designers to limit the load slew rates and maximum values within the system supply's capabilities where the load is unknown. In addition, the programmed current ramp slew rate results in lower impact on voltage drop throughout the backplane. The output voltage slew rates are also indirectly controlled as shown in the figure.



(a) programmed inrush current **(b) corresponding output voltages**

Figure 8. UCC3919-EVM (di/dt) in Terms of Co = 0 µF, 560 µF, 1410 µF With Ro = 10 ohm

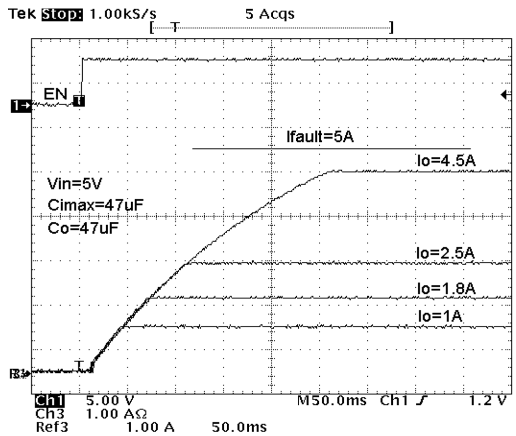


Figure 9. UCC3919-EVM (di/dt) Inrush Currents in Terms of Io = 1 A, 1.8 A, 2.5 A, 4.5 A

For high current applications (>20 A), current ramp controllers can exhibit unstable ramp-up current since the gate capacitance of MOSFET is so large that the FET can oscillate. The current ramp hot swap contoller IC TPS2306 can be used with the largest available power FETs and not have any stability problems.

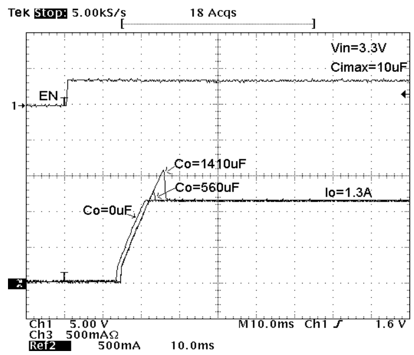
4 Experimental Comparison Between Current Ramp and Voltage Ramp

The turn-on and turn-off comparisons are made using different load capacitors, load currents, and voltages. Section 4.1 shows the comparison under different load capacitors. Section 4.2 shows the comparison under different load currents.

4.1 Current Ramp and Voltage Ramp Comparison Under Different Load Capacitors

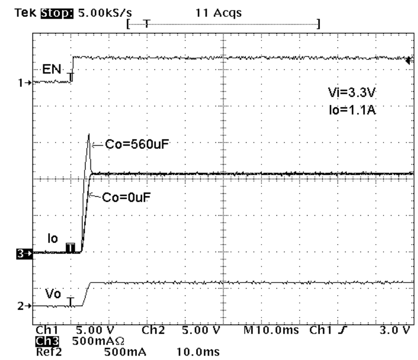
Figure 10 and Figure 11 show the turn-on characteristics of both current ramp and voltage ramp devices under different load capacitors. Figure 10 and Figure 11 were measured at Vi = 3.3 V and Vi = 5 V, respectively. Figure 12 shows the turn off characteristics under different load capacitors at both Vi = 3.3 V and Vi = 5 V.

di/dt (UCC3919-EVM)	dv/dt (TPS2301-EVM)



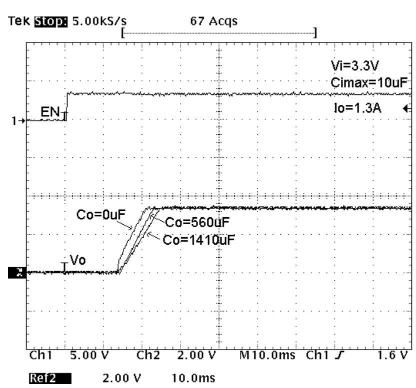
a) inrush current responses

- Current slew rate is controlled, resulting in fixed current ramp rate under various load capacitors (compare to (b)).
- A larger capacitor requires more charging time than that of smaller capacitor. The current ramps up until the CIMAX capacitor is fully charged.



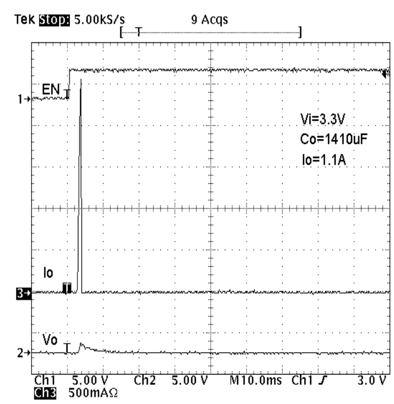
b) inrush current and voltage responses

- A larger load capacitor causes higher inrush peak current, which can result in voltage droop at input back plane (compare to (a)).
- Voltage slew rate is nearly fixed under various load capacitors (compare to (c)).



(c) corresponding voltage responses to above figure (a)

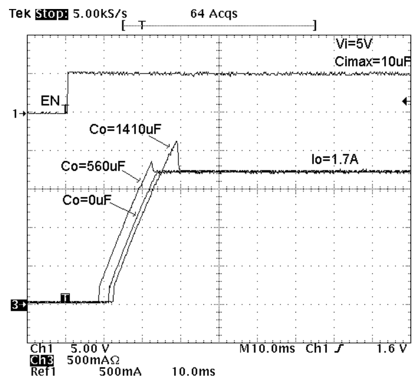
- The voltage ramp rate is determined by load capacitor charging time and load current (see Figure 13(c)).



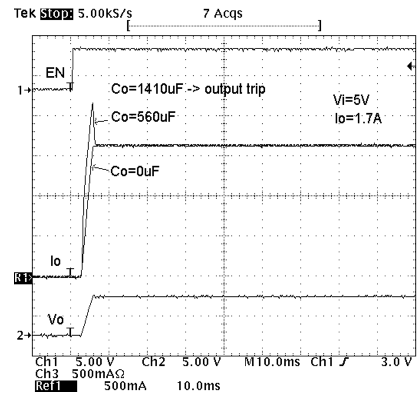
(d) over current trip

- This figure shows an output trip occurred with Co = 1410 μF (compare to (a)).
- Current limited controllers can limit the inrush current till the voltage ramps up fully without output trip.

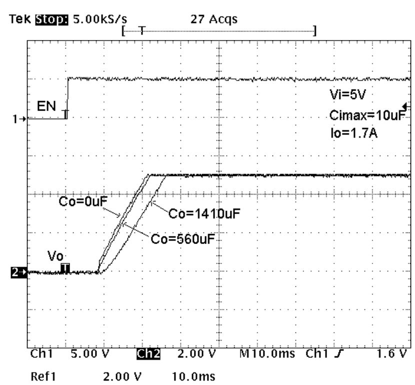
Figure 10. Turn-On Characteristics Under Different Load Capacitors (Vi = 3.3 V)

<table>
<tr><th>di/dt (UCC3919-EVM)</th><th>dv/dt (TPS2301-EVM)</th></tr>
<tr><td>


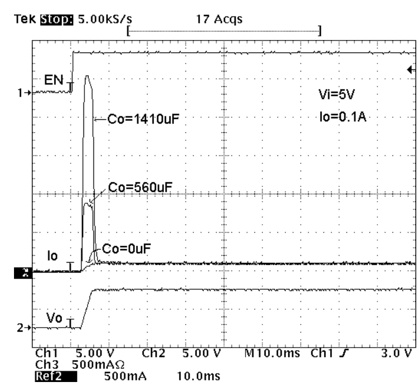
(a) inrush current responses

- Current slew rate is controlled, resulting in fixed current ramp rate under various load capacitors (compare to (b)).
- Test results are nearly same as Figure 10 (a) except for a different voltage and the corresponding load currents.
</td><td>


(b) Inrush current and voltage responses

- A larger load capacitor causes higher inrush peak current, which can result in voltage droop at input back plane (compare to (a)).
- Voltage slew rate is nearly fixed under various load capacitors (compare to (c)).
</td></tr>
<tr><td>


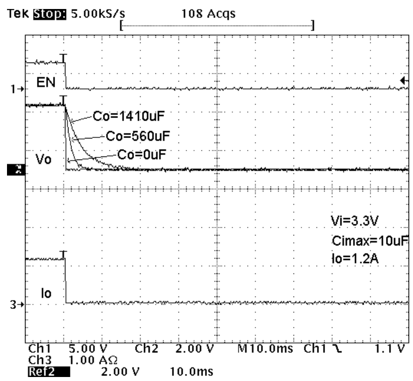
(c) corresponding voltage responses to above figure (a)

- The voltage ramp rate is determined by load capacitor charging time and load current (see Figure 14(c)).
</td><td>


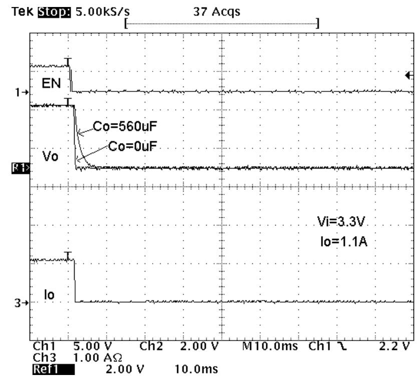
(d) inrush current and voltage responses with load current of 0.1 A

- Larger load capacitor causes higher peak inrush current even at low load current (0.1A)
- Current limited controllers can limit the inrush peak current. Sharp current slew rate may cause voltage drop at input terminal.
</td></tr>
</table>

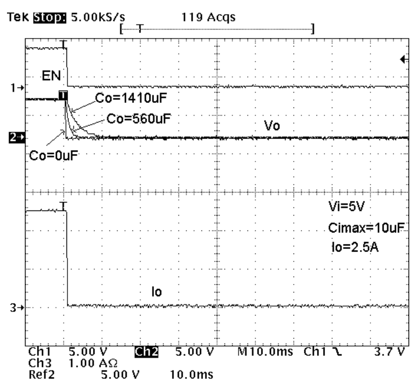
Figure 11. Turn-On Characteristics Under Different Load Capacitors at (Vi = 5 V)

<table>
<tr><th>di/dt (UCC3919-EVM)</th><th>dv/dt (TPS2301-EVM)</th></tr>
<tr><td>


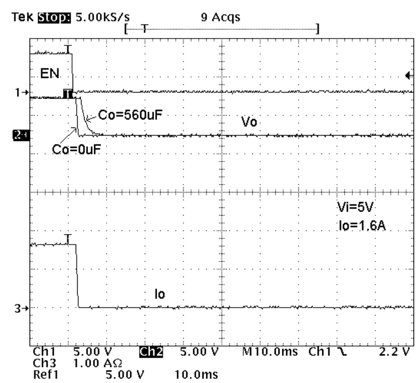
(a) output voltage(3.3V) and load current responses

- The output voltage is naturally discharged through the load impedance.
- The load currents are immediately disconnected.
</td><td>


(b) output voltage(3.3V) and load current responses

- The output voltage is naturally discharged through the load impedance
- The load currents are immediately disconnected.
</td></tr>
<tr><td>


(c) output voltage(5 V) and load current responses

- The output voltage is naturally discharged through the load impedance.
- The load currents are immediately disconnected.
</td><td>


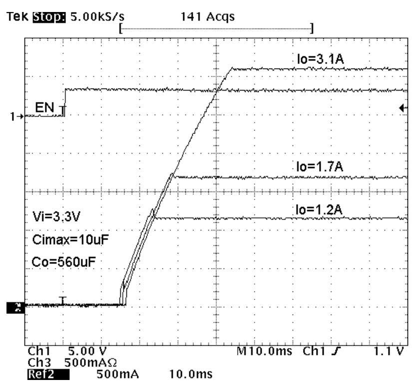
(d) output voltage(5V) and load current responses

- The output voltage is naturally discharged through the load impedance.
- The load currents are immediately disconnected.
</td></tr>
</table>

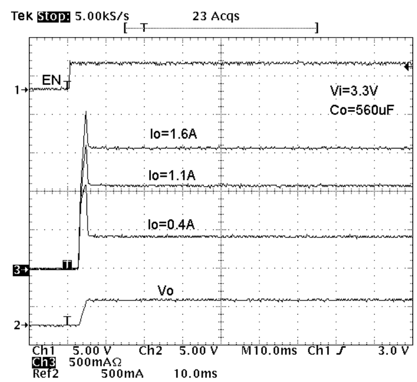
Figure 12. Turn-Off Characteristics, Different Load Capacitors (Vi = 5 V) and (Vi = 3.3 V)

4.2 Current Ramp and Voltage Ramp Comparison in Terms of Different Load Currents

Figure 13 and Figure 14 were measured at Vi = 3.3 V and Vi = 5 V, respectively. Figure 15 shows the turn-off characteristics under different load currents at Vi = 3.3 V. Figure 16 shows the turn-off characteristics at Vi = 5 V under the same conditions as Figure 15.

<table>
<tr><th>di/dt (UCC3919-EVM)</th><th>dv/dt (TPS2301-EVM)</th></tr>
<tr><td>


(a) inrush current responses

• Current slew rate is controlled, resulting in fixed current ramp rate under various load currents (compare to (b)).
</td><td rowspan="2">


(b) inrush current and voltage responses

• Voltage slew rate is nearly fixed under various load currents (compare to (c)).

• A higher load current causes higher inrush peak current, which can result in voltage droop at input back plane (compare to (a)). (The reason the higher current has less peak portion of inrush current in the figure is because capacitor charging current is constant while load current increases.)

• Current limited controllers can limit the peak inrush current, but the sharp current slew rate may still cause voltage droop at input terminal.
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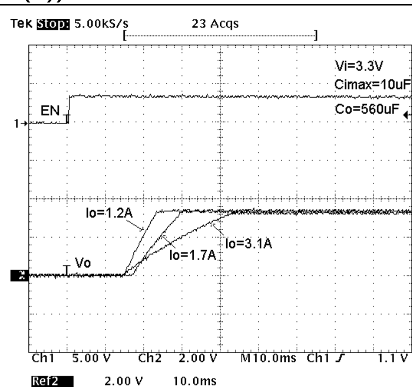
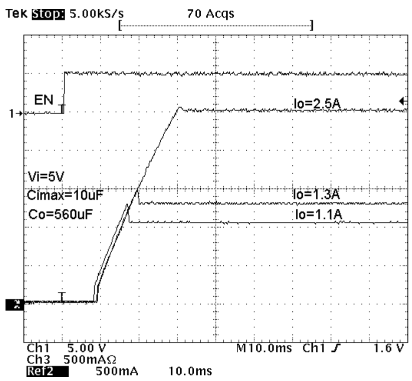
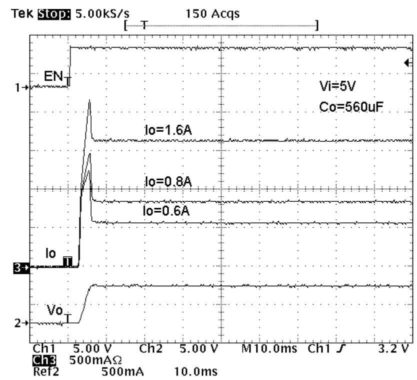
<tr><td>


(c) corresponding voltage responses to above figure (a)

• The voltage ramp rate is determined by load capacitor charging time and load current (see Figure 10(c)).
</td></tr>
</table>

Figure 13. Turn-On Characteristics Under Different Load Currents (Vi = 3.3 V)

<table>
<tr><th>di/dt (UCC3919-EVM)</th><th>dv/dt (TPS2301-EVM)</th></tr>
<tr><td>


(a) inrush current responses
Current slew rate is controlled, resulting in fixed current ramp rate under various load currents (compare to (b)).
</td>
<td rowspan="2">


(b) Inrush current and voltage responses
Higher load currents causes higher inrush peak current (compare to (a))
Voltage slew rate is nearly fixed under various load currents (compare to (c)).
Higher voltage result in higher inrush peak current (see Figure 13 (b)).
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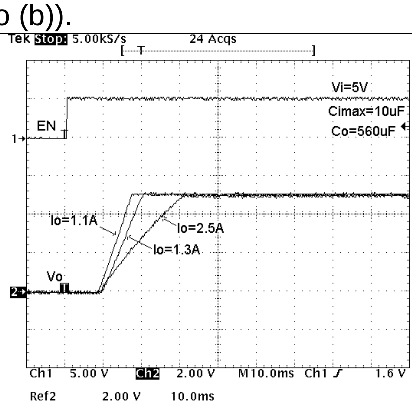
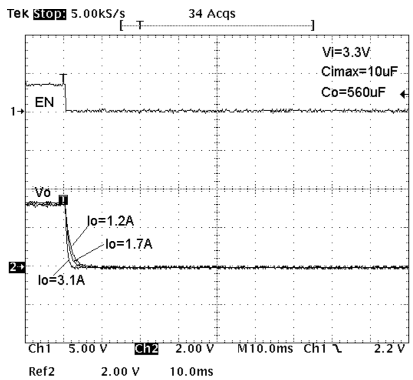
<tr><td>


(c) corresponding voltage responses to above figure (a)
The voltage ramp rate is determined by load capacitor charging time and load current (see Figure 11(c)).
</td></tr>
</table>

Figure 14. Turn-On Characteristics Under Different Load Currents (Vi = 5 V)

<table>
<tr><th>di/dt (UCC3919-EVM)</th><th>dv/dt (TPS2301-EVM)</th></tr>
<tr><td>



(a) output voltage responses

- The output voltage is naturally discharged through the load impedance.

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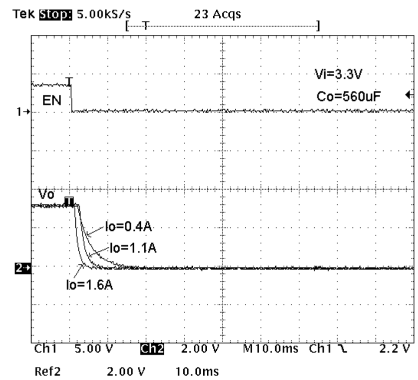
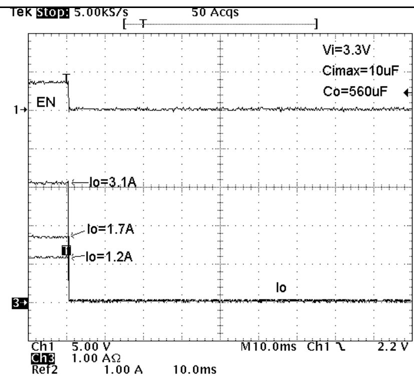


(b) output voltage responses

- The output voltage is naturally discharged through the load impedance.

</td></tr>
<tr><td>



(c) load current responses

- The load currents are immediately disconnected.

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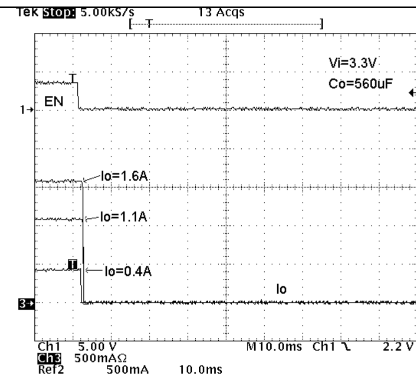


(d) load current responses

- The load currents are immediately disconnected.

</td></tr>
</table>

Figure 15. Turn-Off Characteristics Under Different Load Currents at (Vi = 3.3 V)

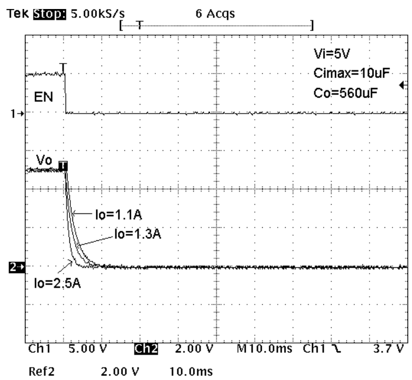
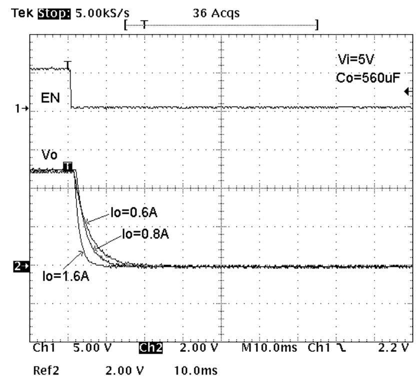
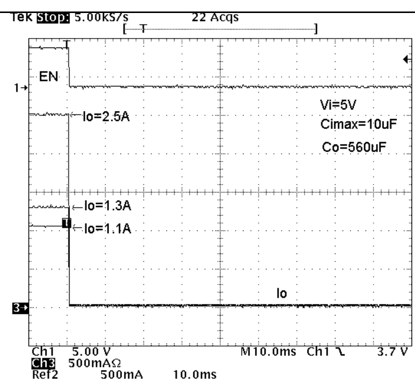
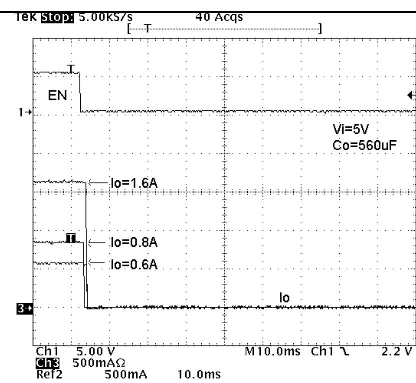
di/dt (UCC3919-EVM)	dv/dt (TPS2301-EVM)
 **(a) output voltage responses** • The output voltage is naturally discharged through the load impedance.	 **(b) output voltage responses** • The output voltage is naturally discharged through the load impedance.
 **(c) load current responses** • The load currents are immediately disconnected.	 **(d) load current responses** • The load currents are immediately disconnected.

Figure 16. Turn-Off Characteristics Under Different Load Currents at (Vi = 5 V)

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5 Conclusion

Figure 17 shows a simplified equivalent block diagram of a hot swap system. Table 1 summarizes the comparison between two hot swap devices based on Figure 17.

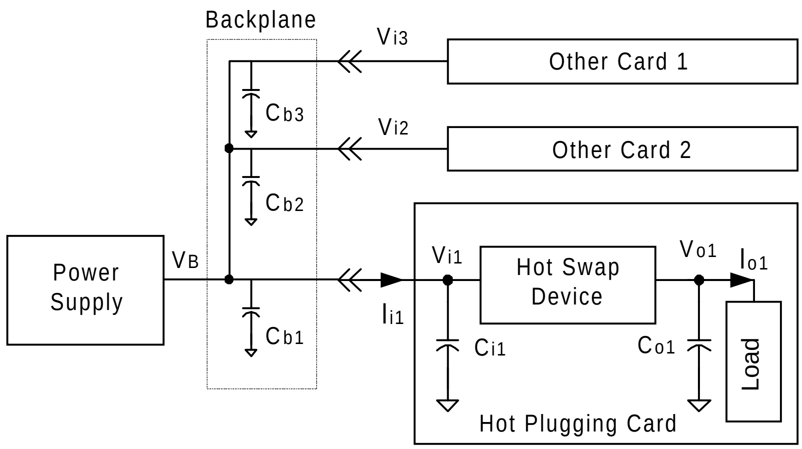

Figure 17. Simplified Equivalent Block Diagram of a Hot Swap System

Table 1. Summary of the Comparison Between Two Hot Swap Devices

	Current Ramp Hot Swap Controller IC	Voltage Ramp Hot Swap Controller IC
Device Complexity	The circuit design and component selection for a current ramp controlled hot swap approach is more complex than that for a voltage ramp controlled approach. This complexity adds flexibility to develop robust hot swap solutions for systems with unknown capacitance load or large capacitance load.	The application simplicity of a voltage ramp controlled hot swap device makes it easier to use. This simplicity is applicable to develop robust hot swap solutions for systems with known low capacitance load.
Inrush Current	❑ The programmed current ramp results in lower impact on voltage drop throughout the backplane (V_B, V_{i2}, and V_{i3}) than that for the voltage ramp controller device. ❑ Due to the programmed inrush current (di_{i1}/dt), a current ramp controlled hot swap device is more applicable for unknown loads (C_{i1}, C_{o1}, and load impedance). ❑ Due to the programmed inrush current (di_{i1}/dt), the backplane capacitors (C_{b1}, C_{b2}, and Cb3) can be minimized if no requirement exists.	❑ A constant value or nearly constant value of dV_{o1}/dt causes an inrush current (I_{i1}) to flow into the card being plugged-in or enabled. This spike current (I_{i1}) can cause voltage drops throughout the backplane (V_B, V_{i2}, and V_{i3}) or power distribution system. Depending upon the magnitude of the current step (dI_{i1}/dt), the power supply output impedance, the power supply distribution impedance, the hot plugging card input impedance (C_{i1}, C_{o1}, and load), and the sensitivity to voltage deviations of other portions of the system, total system functionality can be impacted by plugging this card in. ❑ The backplane capacitors (C_{b1}, C_{b2}, C_{b3}) must be bigger than that of a current ramp controlled approach to handle the voltage drop caused by an inrush current.

	Current Ramp Hot Swap Controller IC	Voltage Ramp Hot Swap Controller IC
Miscellaneous	The harmonic content of a ramp current (I_{i1}) is lower than that of a step current from voltage ramp devices, particularly at the higher frequencies; therefore, the noise generated in the power distribution is lower with a di_{i1}/dt controlled approach than with a voltage ramp controlled approach.	The step of current that must be supplied in a dV_{o1}/dt controlled hot swap device has a large harmonic content extending into high frequencies. The noise generated by theses harmonics can impact other portions of the system (Card 1 and Card 2), depending upon the sensitivity of other system elements.

6 References

User's Guide for TPS2301-EVM, SLVU026, March 2000.

TPS202x/3x and TPS204x/5x USB Power Distribution, SLVA049, March 2000.

UCC3919 Hot Swap Power Manager Evaluation Circuit and List of Materials, SLUS374, November 1999.

For more information on hot swap controllers;

http://www.ti.com/

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265