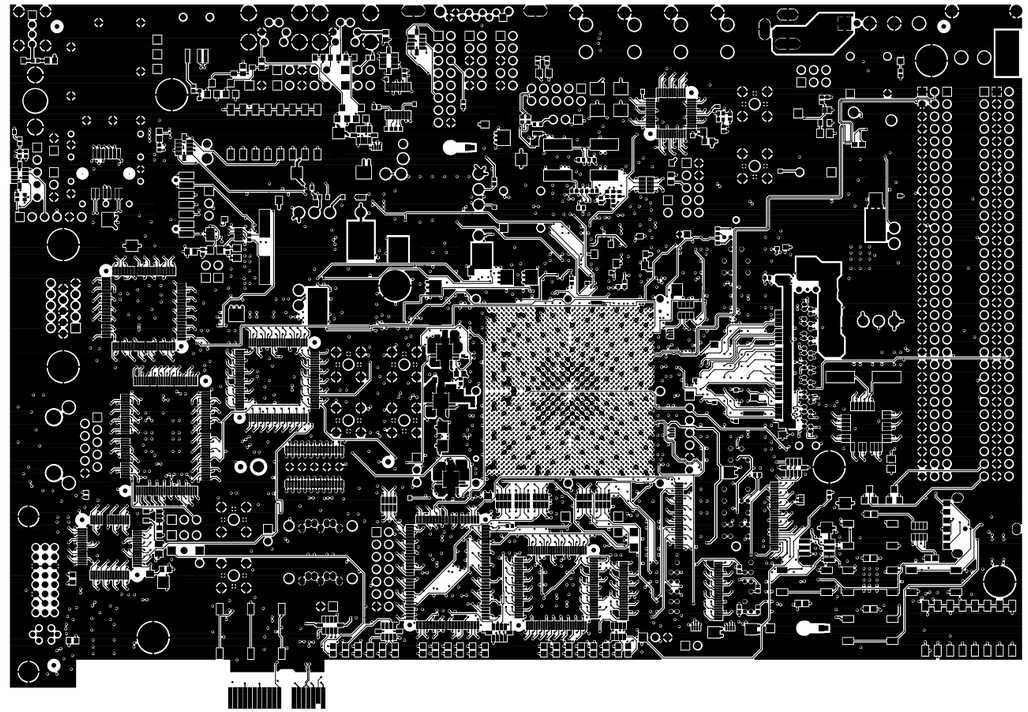
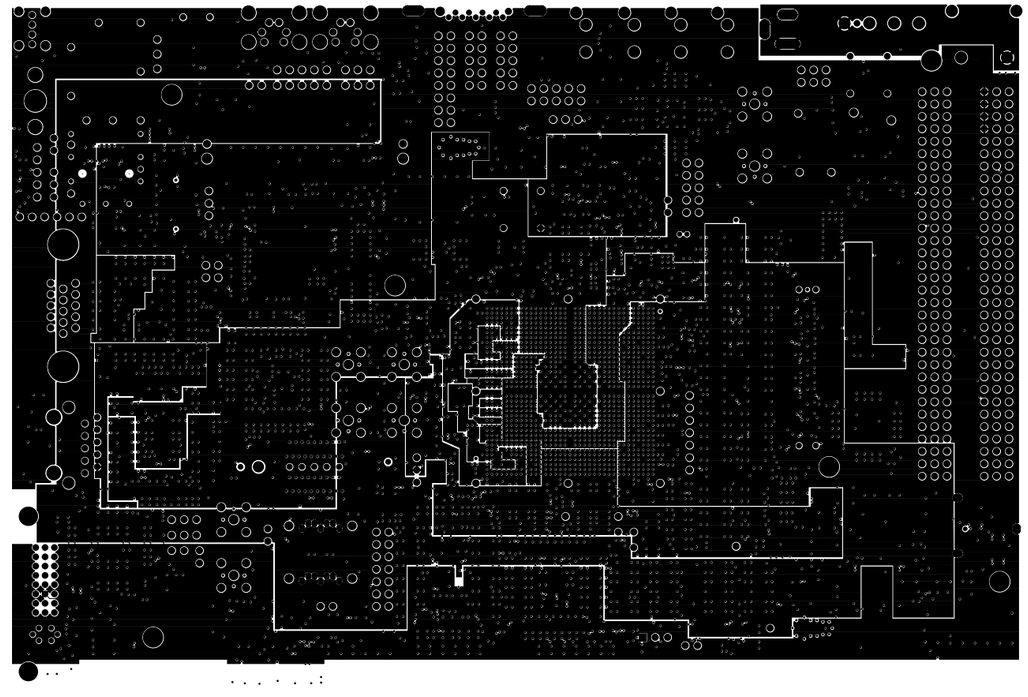
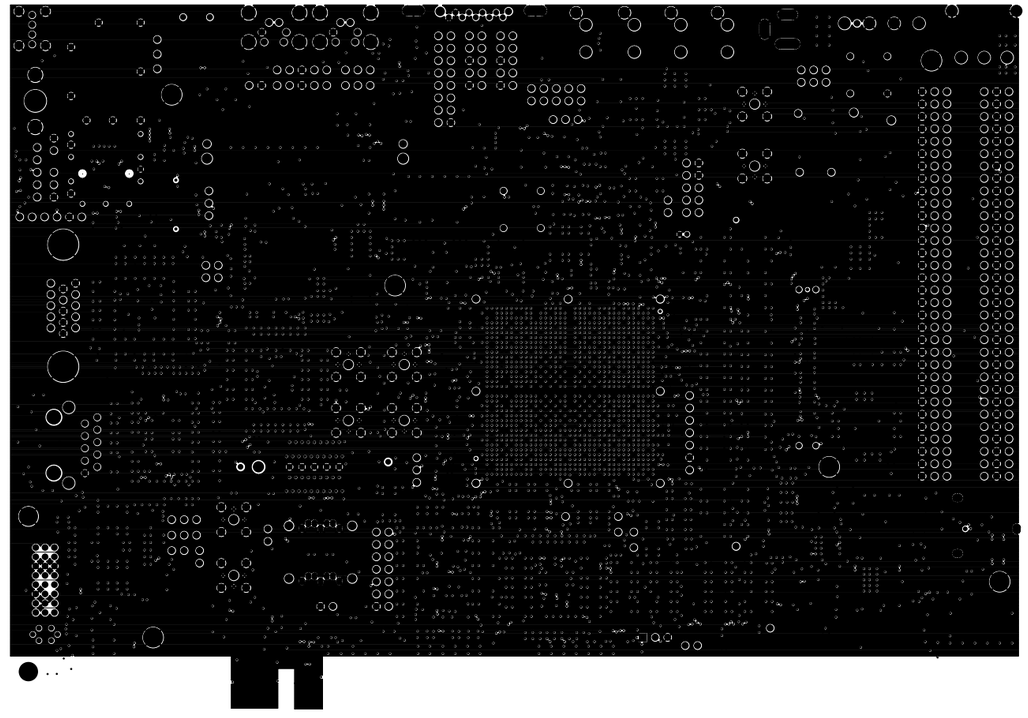


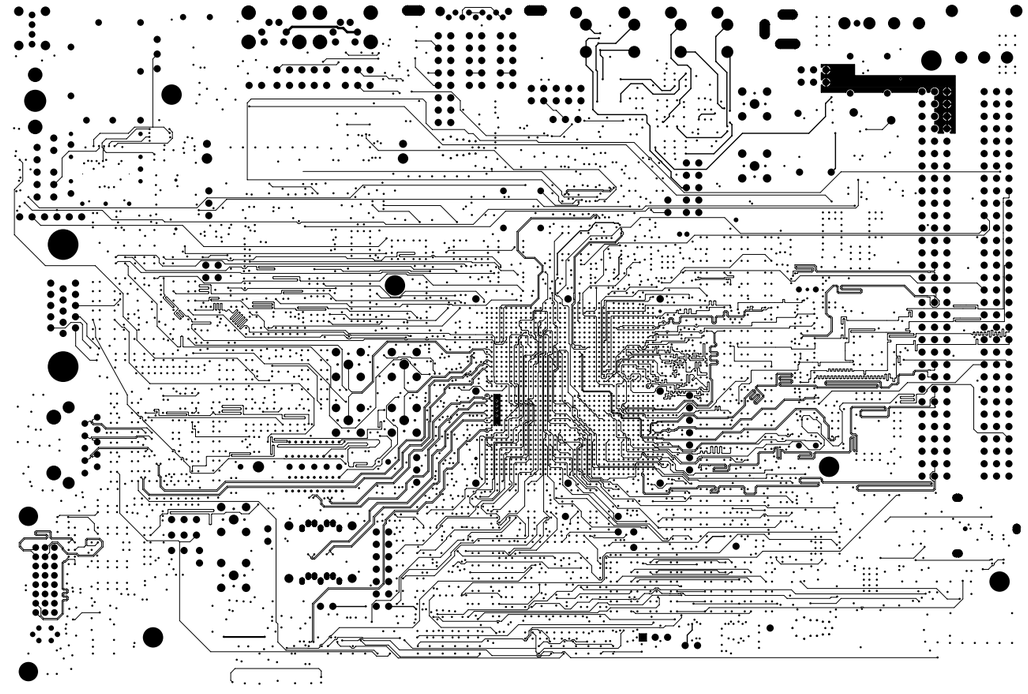
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 01 OF 25 L1 TOP



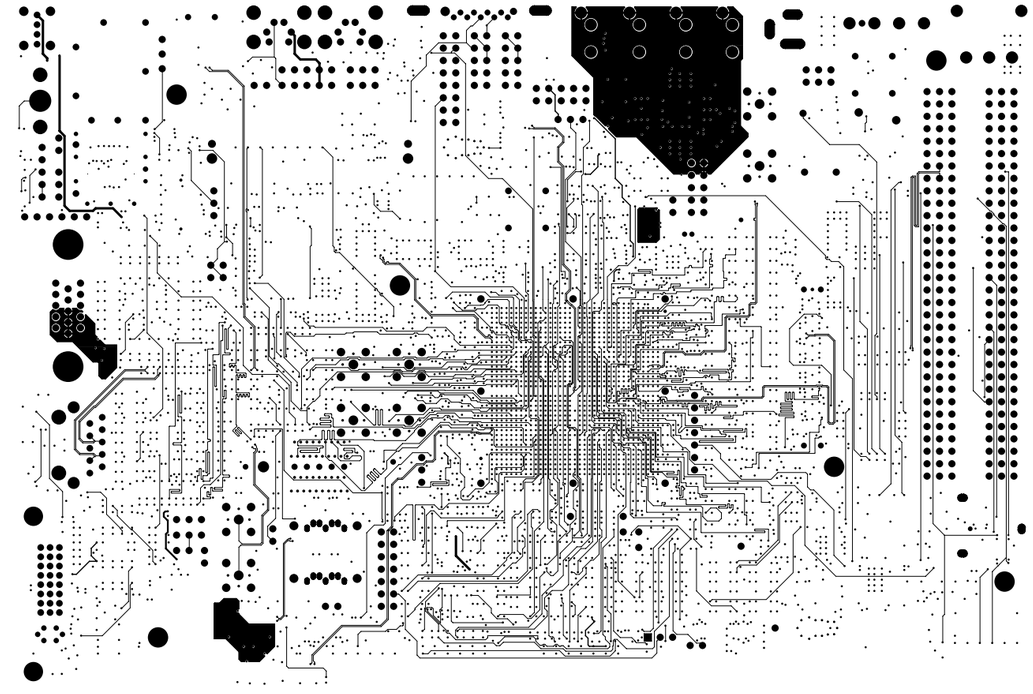
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 02 OF 25 L2_PWR



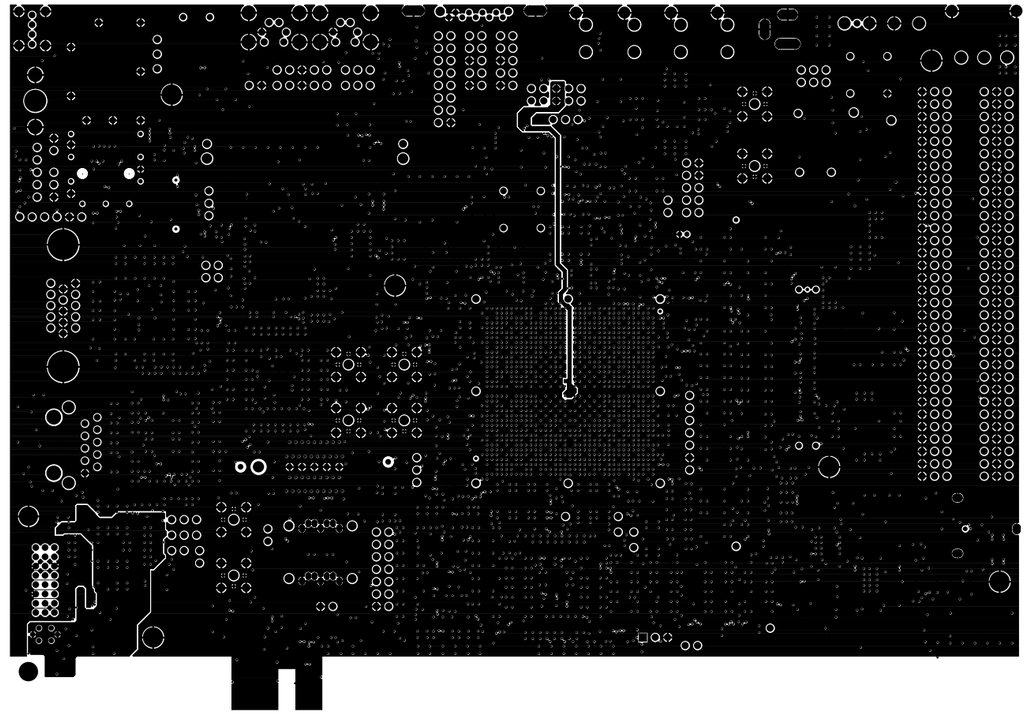
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 03 OF 25 L3_GND



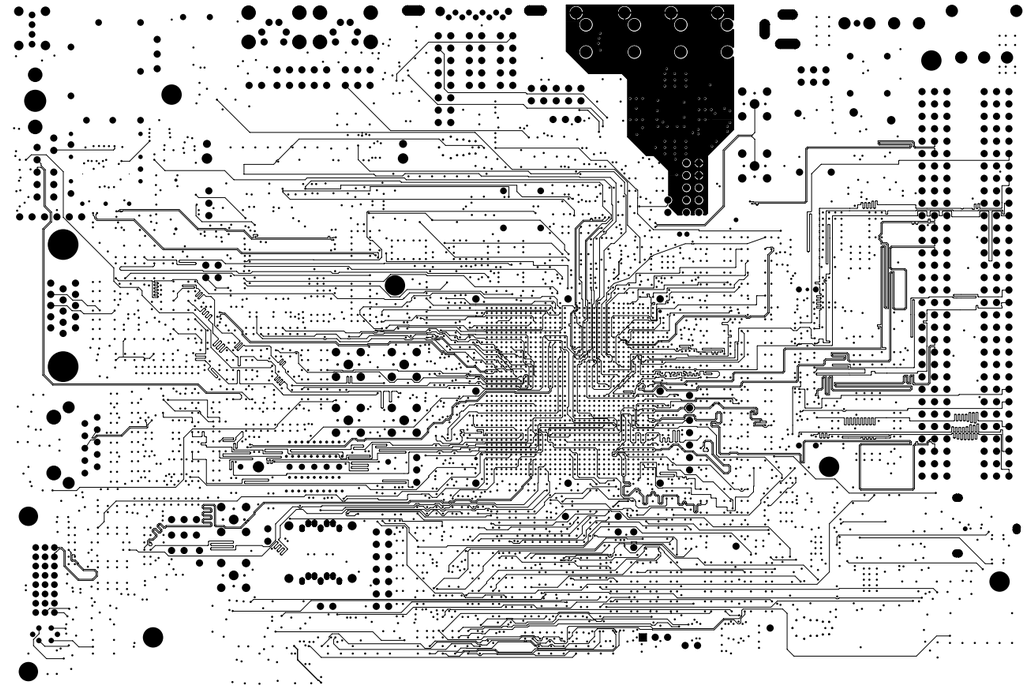
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 04 OF 25 L4_SIG



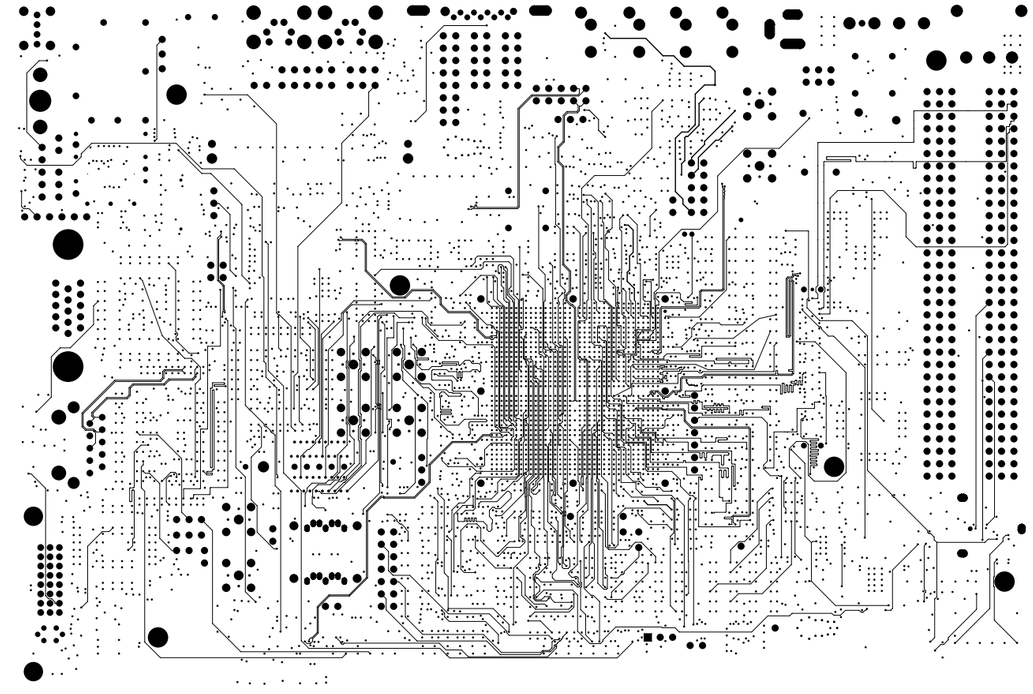
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 05 OF 25 L5_SIG



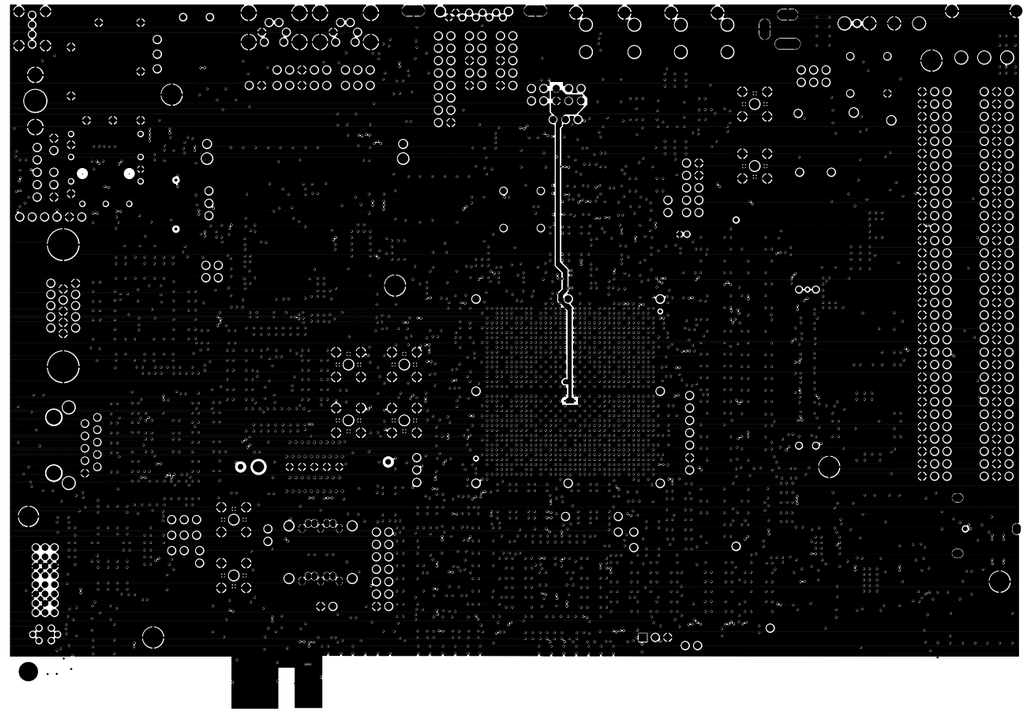
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 06 OF 25 L6 GND



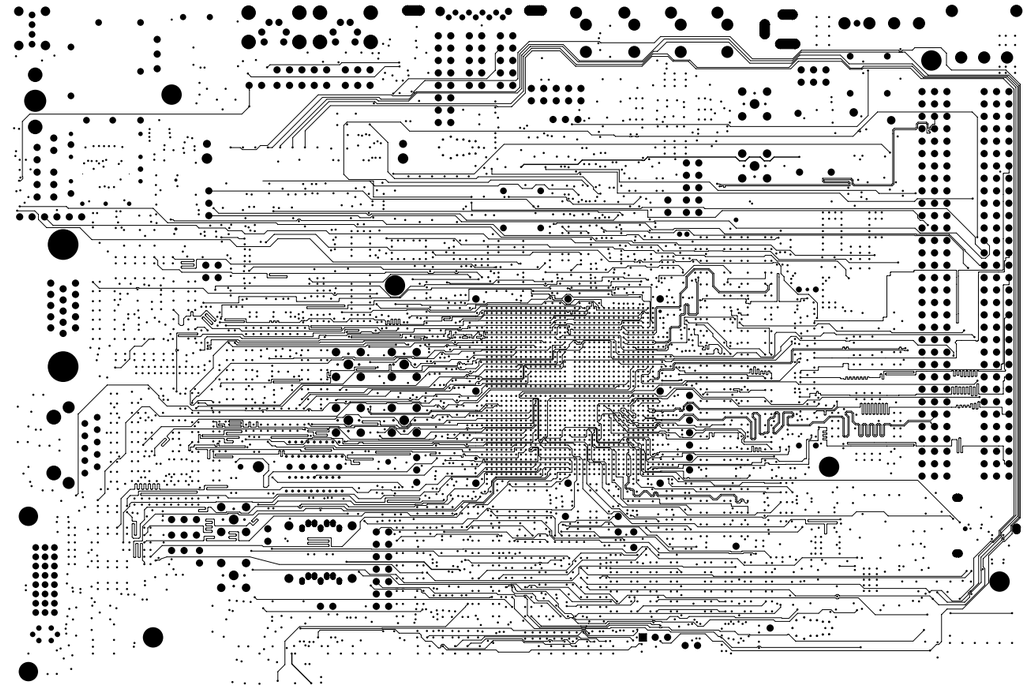
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 07 OF 25 L7_SIG



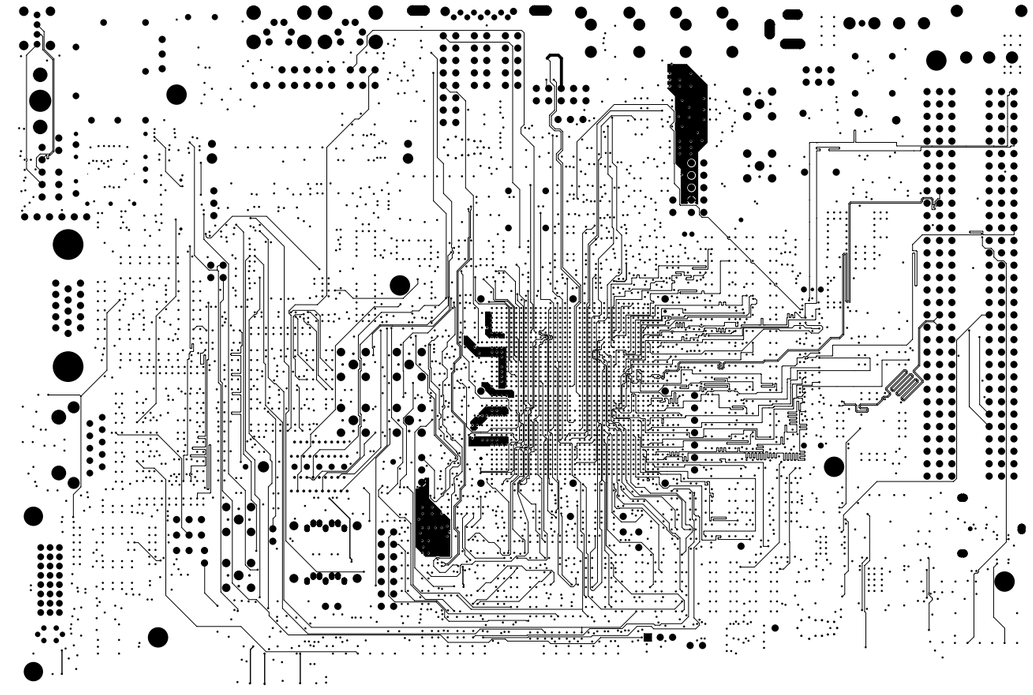
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 08 OF 25 L8 SIG



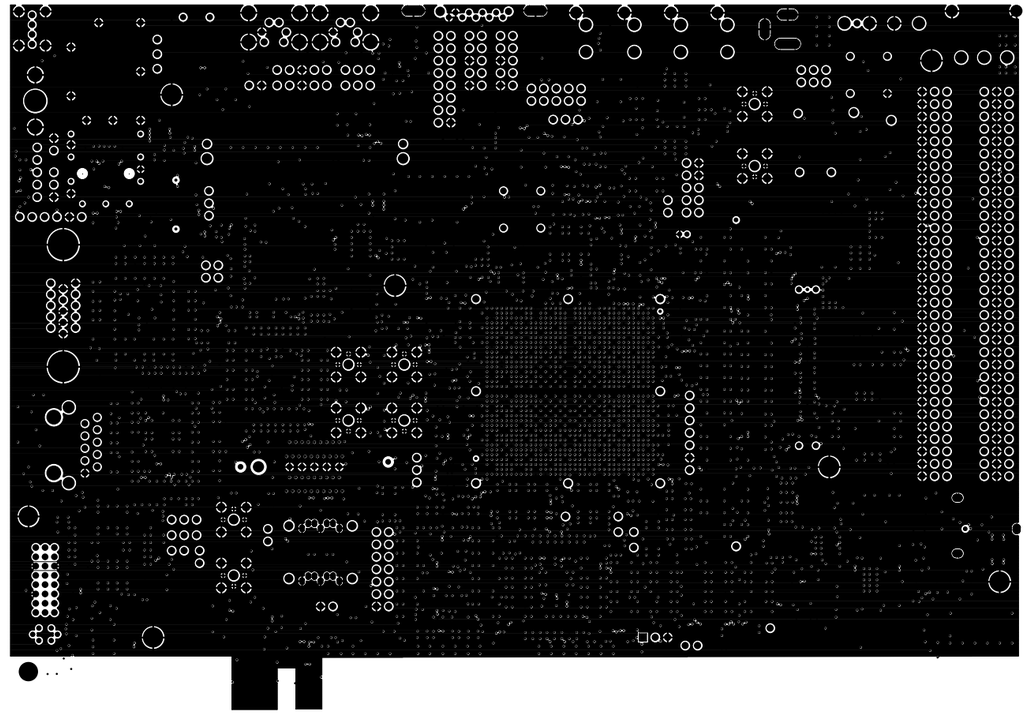
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 09 OF 25 L9 GND



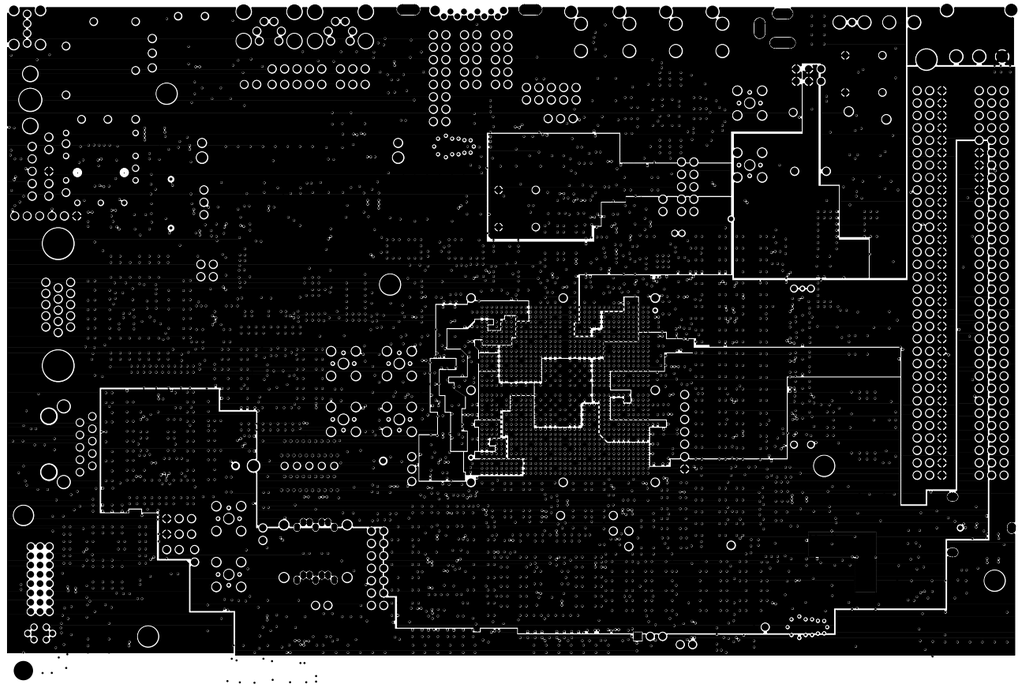
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 10 OF 25 L10_SIG



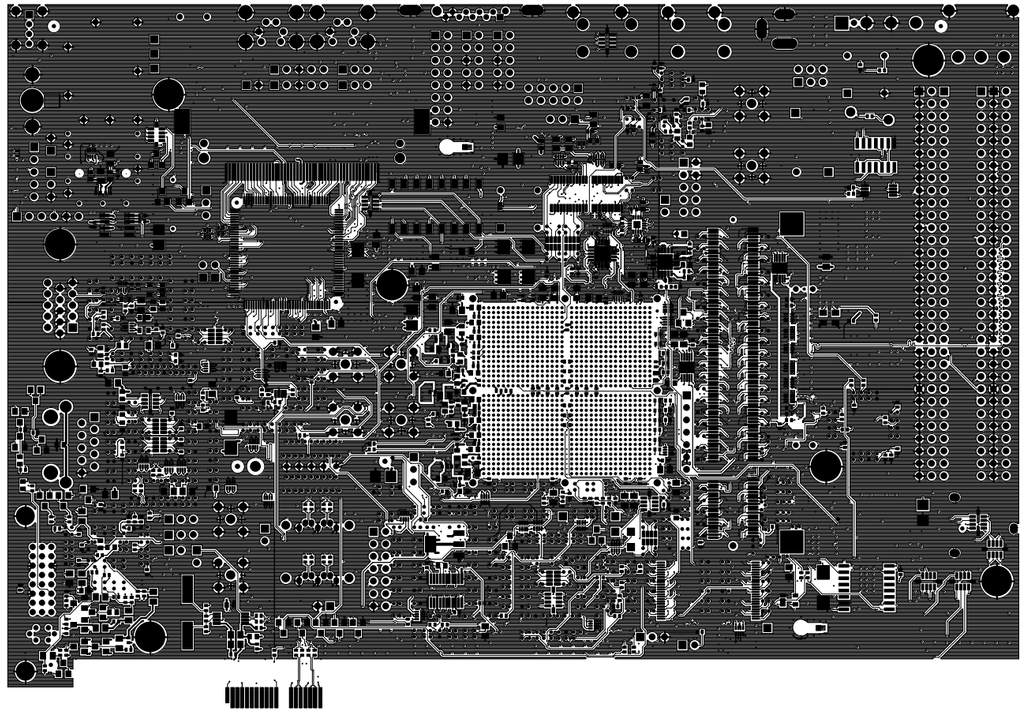
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 11 OF 25 L11_PWR



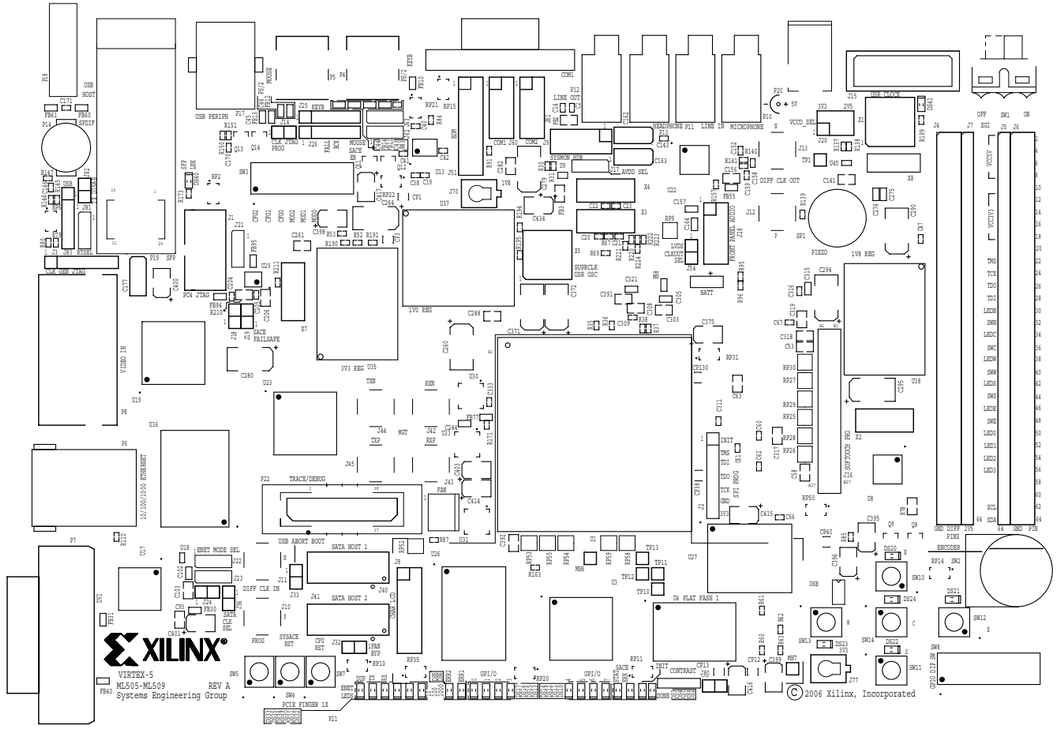
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 12 OF 25 L12 GND



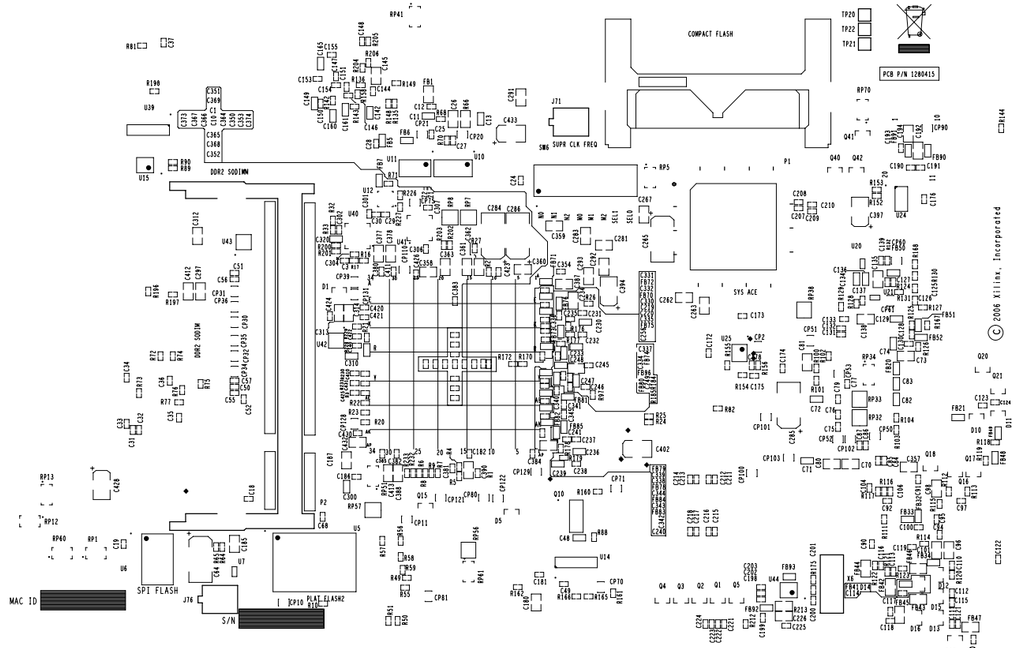
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 13 OF 25 L13 GND



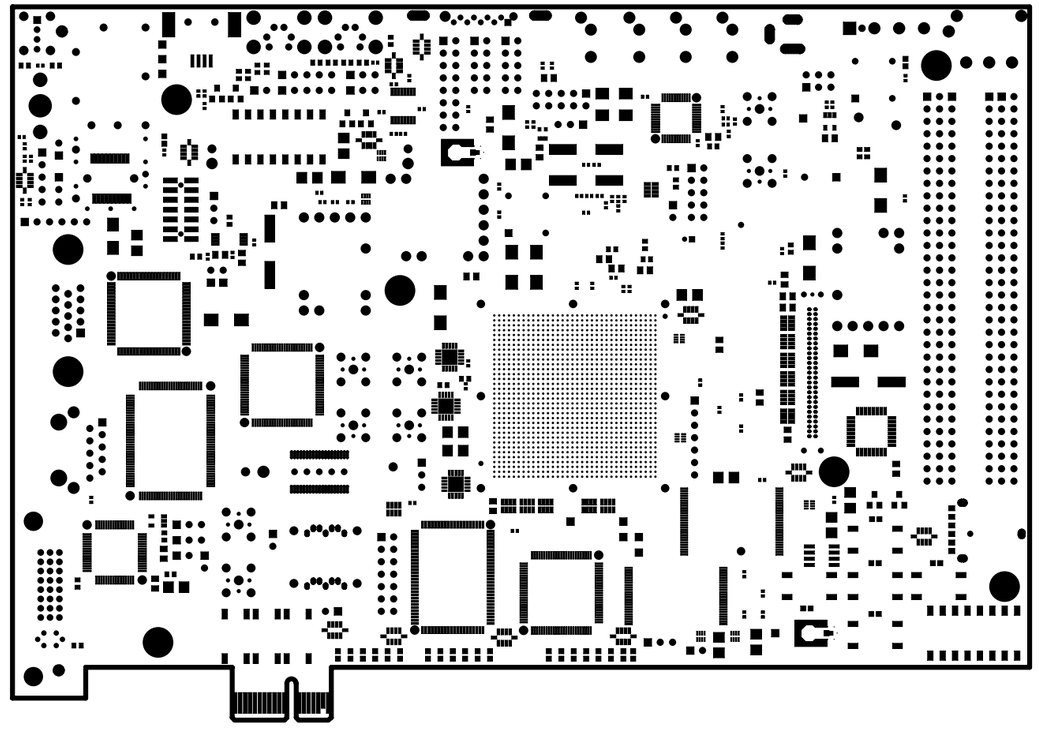
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 14 OF 25 L14 BOTTOM



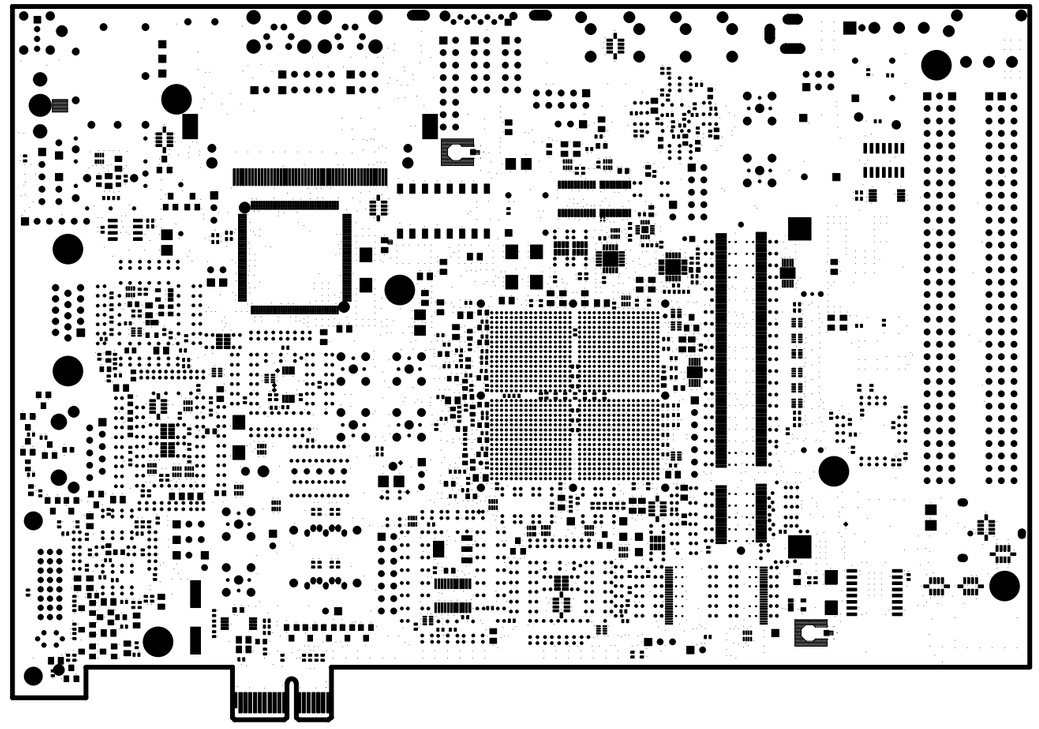
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER:
19 OF 25 SILK-SCREEN TOP



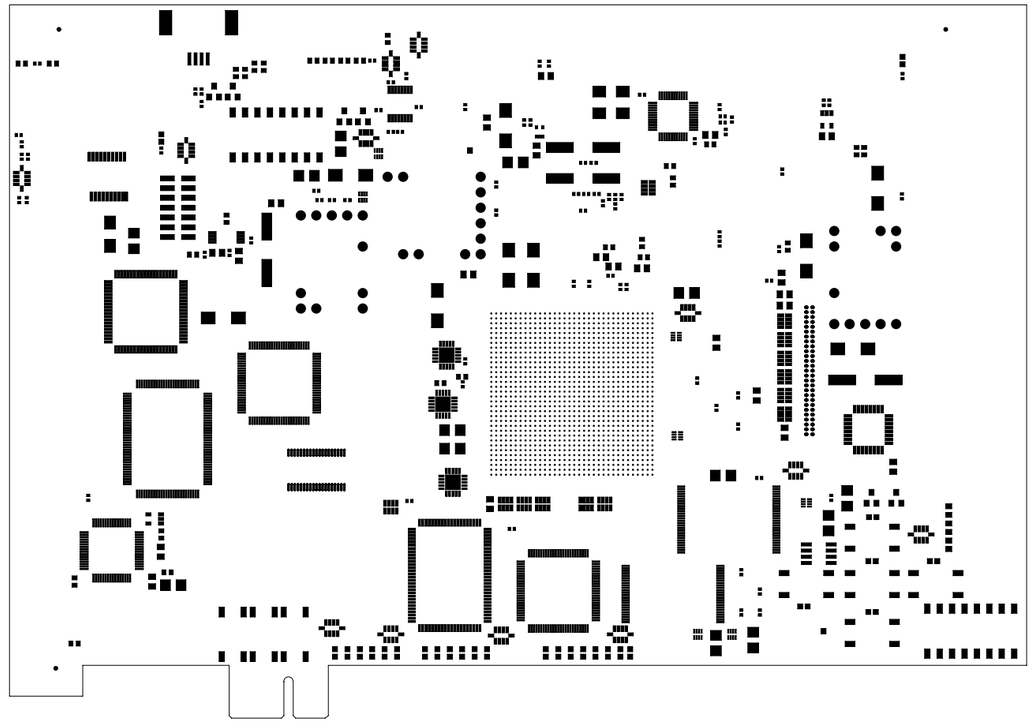
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER:
20 OF 25 SILK_SCREEN_BOTTOM



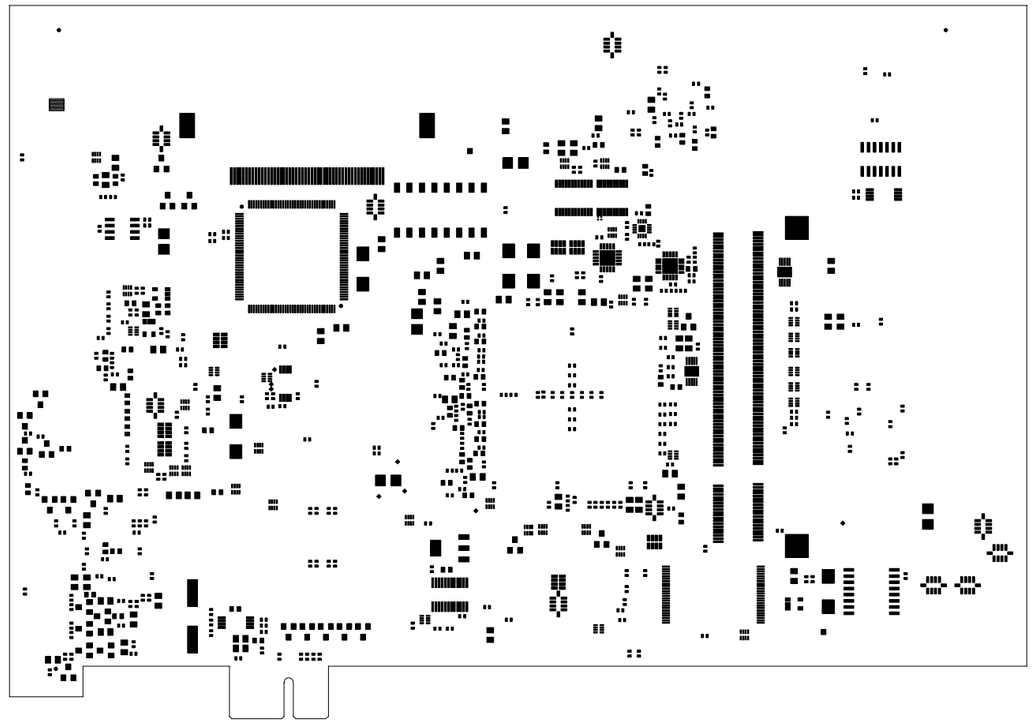
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 15 OF 25 MASK_TOP



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 16 OF 25 MASK BOTTOM



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 17 OF 25 PASTE TOP



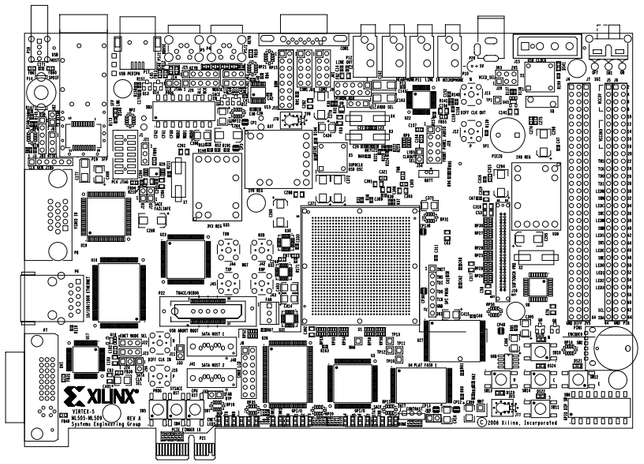
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 18 OF 25 PASTE BOTTOM

REV	DESCRIPTION	DWG NO.
01		0431402

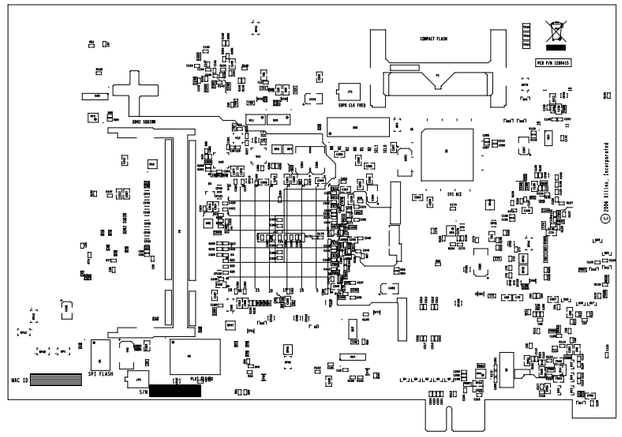
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	INITIAL RELEASE		

ASSEMBLY NOTES:

1- INSTALL SHUNT WHERE SHOWN.
2- ASSEMBEL SCREWS, BUMPERS AND STANDOFS ON SIDE CLOSEST TO THE POWER JACK



VIEWED FROM TOP SIDE



VIEWED FROM BOTTOM SIDE

ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 25 OF 25 ASSEMBLY

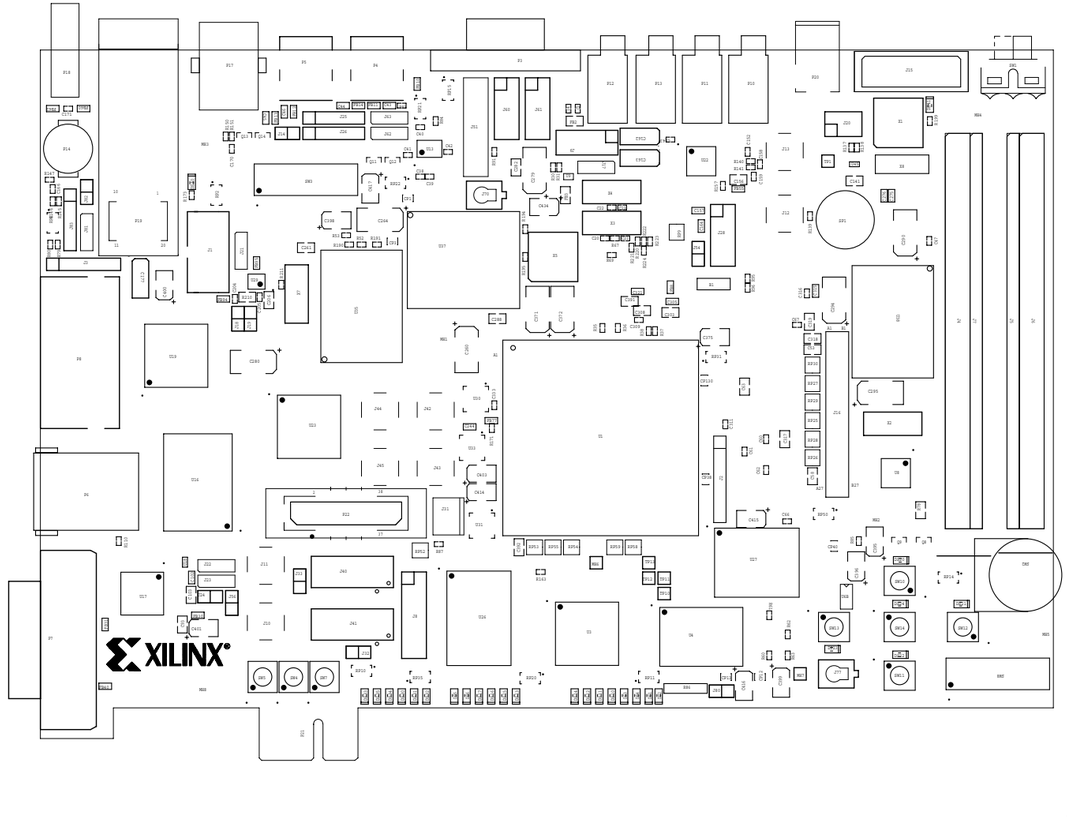
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX± .02 .XXX± .010 ANGLES ± 10	CAD GENERATED DRAWING, DO NOT MANUALLY UPDATE
MATERIAL SEE SEPARATE BILL OF MATERIALS	APPROVALS / DATE: DRAWN WHIZZ; CHECKED; RES ENG; MFG ENG; QUAL ENG; APPROVED
FINISH	
DO NOT SCALE DRAWING	

XILINX® 2100 LOGIC DRIVE SAN JOSE, CALIFORNIA 95124

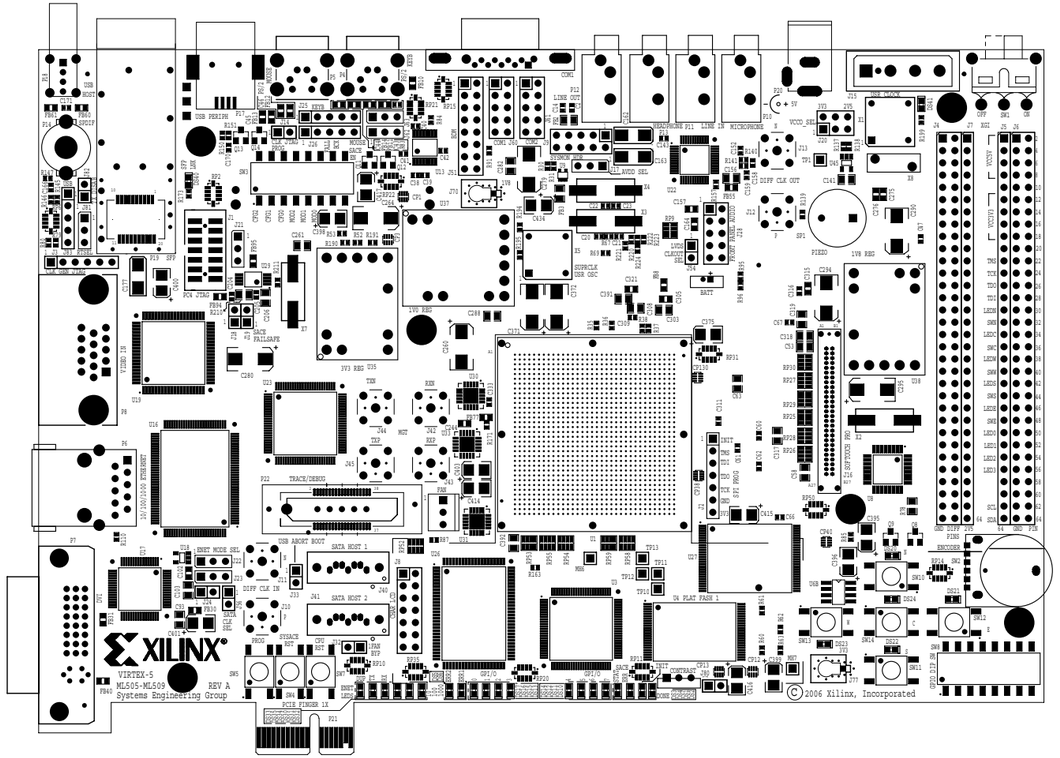
TITLE: ASSY, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM

SIZE	FSCM NO.	DWG NO.	REV.
B		0431402	01

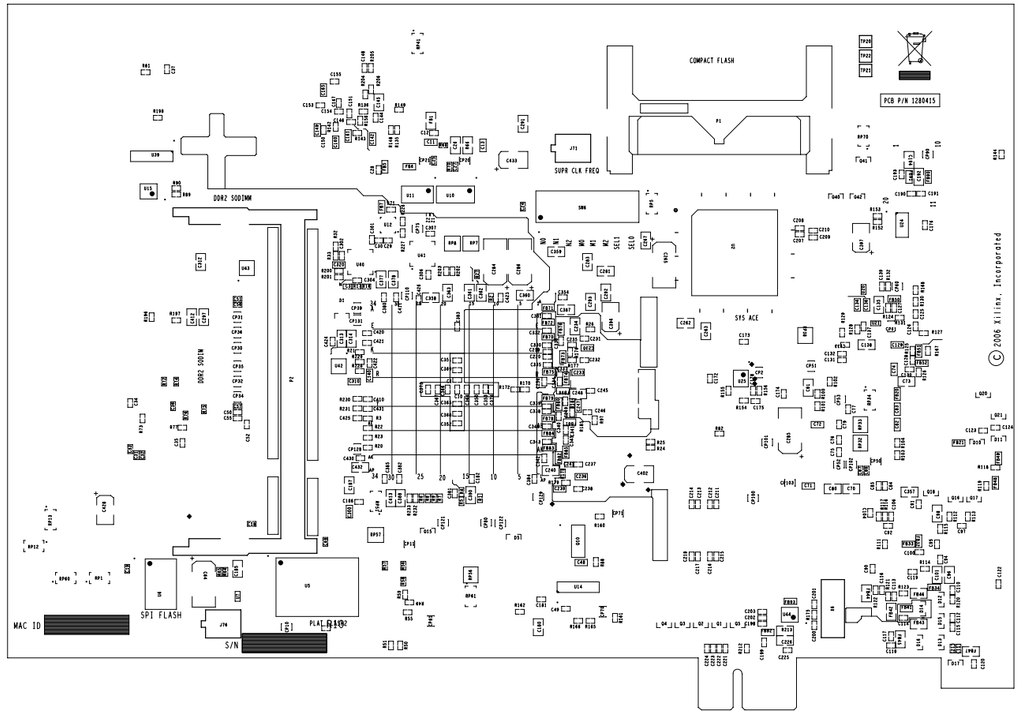
SCALE 1 : 1 SHEET 1 OF 1



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 22 OF 25 ASSY TOP



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 22 OF 25 ASSY TOP
19 OF 25 SILK=SCREEN TOP



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 23 OF 25 ASSY BOTTOM
20 OF 25 SILK SCREEN BOTTOM

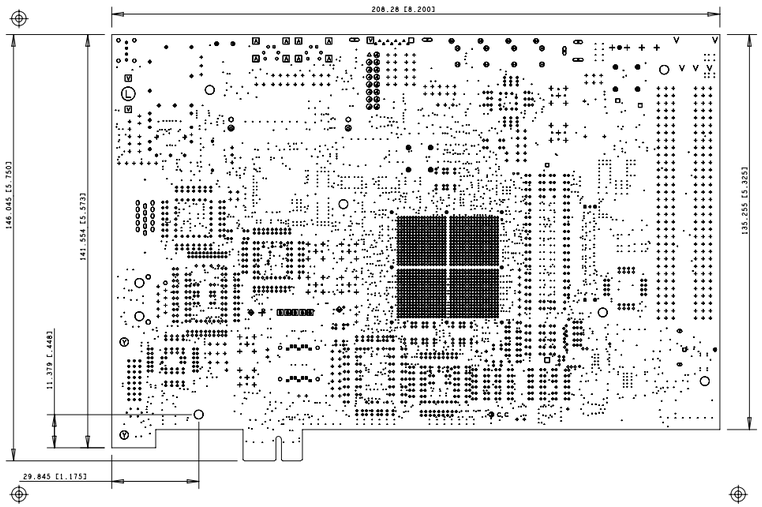
REV 01

DESCRIPTION

DWG NO. 1280412

NOTES:

1. FABRICATE TO IPC-A-600,CURRENT REVISION.
2. BOARD SHALL MEET THE INSPECTION CRITERIA OF IPC-A-600,CLASS 2,CURRENT REVISION.
3. MATERIAL: HIGH TEMP FR4 Tg160C OR GREATER
4. WEIGHT OF ALL COPPER LAYERS SHALL NOT BE LESS 0.5 OZ. PER SQUARE FOOT.
5. IMPEDANCE TOLERANCE+/- 10%
6. APPLY SOLDER MASK OVER BARE COPPER(SMBOC) IAW IPC-SM-840,BOTH SIDES,USING LPI,COLOR GREEN
7. FINISH: GOLD IMMERSION.
8. SILKSCREEN TOP SIDE/BOTH SIDES WITH NON-CONDUCTIVE EPOXY BASED INK. COLOR SHALL BE WHITE A CONTRASTING INK WITH RESPECT TO SOLDER MASK COLOR. DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON PLATED LANDS IS NOT ACCEPTABLE.
9. VENDOR LOGO AND DATE CODE TO BE MAKED FAR SIDE. MAXIMUM HEIGHT .12 INCHES.
10. 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A UL RATING OF 94V-0. UL SYMBOL AND RATING SHAL BE MARKED FARSIDE.
11. REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.
12. SOLDER MASK FOLLOW GERBER DATA FOR TOP & BOTTOM SIDE.
13. SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF + / - 0.002 WITH APPLICABLE HOLE / PAD.
14. 274X GERBERS/ODB++ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST.
15. USE ARTMASTER # 0531573



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 21 OF 25 FAB_DWG

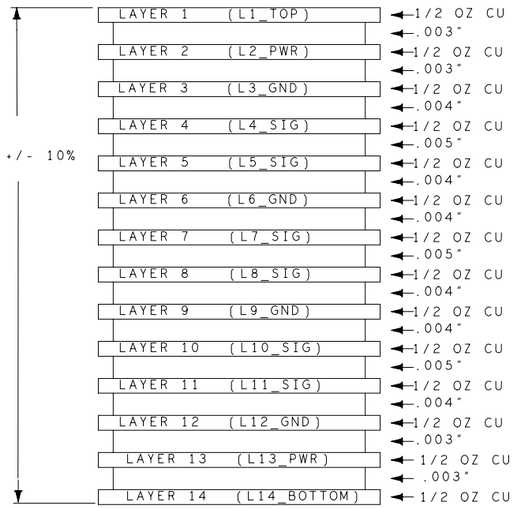
DRILL CHART (TOL ± +/- 3 mils)

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY	ADDITIONAL
·	10.0	+ 0/- 10	PLATED	2502	MAY BE PLUGGED
•	10.0	+ 0/- 10	PLATED	2209	MAY BE PLUGGED
	12.0	+ 0/- 12	PLATED	38	MAY BE PLUGGED
·	15.748	+/- 3	PLATED	24	
·	25.98	+/- 3	PLATED	6	
•	27.559	+/- 3	PLATED	2	
•	27.949	+/- 3	PLATED	4	
•	30.0	+/- 3	PLATED	14	
•	31.5	+/- 3	PLATED	9	
▣	32.0	+/- 3	PLATED	5	
◉	32.0	+/- 3	PLATED	8	
·	33.0	+/- 3	PLATED	1	
•	33.858	+/- 3	PLATED	24	
⊂	35.0	+/- 3	PLATED	2	
+	35.0	+/- 3	PLATED	9	
⊕	35.0	+/- 3	PLATED	1	
◇	35.429	+/- 3	PLATED	12	
○	36.0	+/- 3	PLATED	1	
•	36.22	+/- 3	PLATED	4	
⊕	40.0	+/- 3	PLATED	15	
+	40.0	+/- 3	PLATED	336	
△	40.0	+/- 3	PLATED	1	
•	41.0	+/- 3	PLATED	10	
◎	43.0	+/- 3	PLATED	15	
○	53.15	+/- 3	PLATED	4	
○	53.15	+/- 3	PLATED	4	
□	54.0	+/- 3	PLATED	2	
+	55.0	+/- 3	PLATED	32	
+	60.0	+/- 3	PLATED	8	
○	62.988	+/- 3	PLATED	2	
+	70.0	+/- 3	PLATED	4	
V	73.0	+/- 3	PLATED	5	
⊕	74.799	+/- 3	PLATED	12	
⊠	85.0	+/- 3	PLATED	2	
⊡	90.551	+/- 3	PLATED	8	
·	122.051	+/- 3	PLATED	2	
Ⓥ	123.11	+/- 3	PLATED	2	
○	125.0	+/- 3	PLATED	6	
Ⓛ	160.0	+/- 3	PLATED	1	
·	33.071	+/- 3	NON-PLATED	1	
·	33.461	+/- 3	NON-PLATED	2	
•	37.402	+/- 3	NON-PLATED	9	
•	39.37	+/- 3	NON-PLATED	2	
□	43.311	+/- 3	NON-PLATED	2	
◆	47.0	+/- 3	NON-PLATED	2	
⊗	55.118	+/- 3	NON-PLATED	2	
●	59.059	+/- 3	NON-PLATED	1	
✦	61.0	+/- 3	NON-PLATED	2	
□	62.988	+/- 3	NON-PLATED	2	
•	63.39	+/- 3	NON-PLATED	8	
○	67.0	+/- 3	NON-PLATED	2	
⊠	82.681	+/- 3	NON-PLATED	1	
◎	87.0	+/- 3	NON-PLATED	2	
✦	94.0	+/- 3	NON-PLATED	1	
○	127.949	+/- 3	NON-PLATED	2	
•	47.24x39.37		PLATED	1	
⊗	62.988x39.37		PLATED	2	
▯	118.11x39.37		PLATED	1	
⊂⊃	118.11x39.37		PLATED	1	
⊂⊃	127.949x39.37		PLATED	2	
⊂⊃	137.799x39.37		PLATED	1	

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
01	INTIAL RELEASE		



SCALE:NONE

3

LINE WIDTH IMPEDANCE CHART FOR REFERENCE

LAYER	SINGLE ENDED LINE WIDTH	DIFF LINE WIDTH	SPACE CENTER 2 CENTER	SINGLE	DIFF
L1,L14	5.5 MILS	4.5 MILS	10.5 MILS	50-55 OHMS	100 OHMS
INNER	4.5 MILS	4.5 MILS	10.5 MILS	50-55 OHMS	100 OHMS

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX± .02 .XXX± .010 ANGLES ± 1°

MATERIAL
SEE SEPARATE BILL OF MATERIALS

FINISH

DO NOT SCALE DRAWING

CAD GENERATED DRAWING, DO NOT MANUALLY UPDATE

APPROVALS	DATE
DRAWN WHIZZ	
CHECKED	
RES ENG	
MFG ENG	
QUAL ENG	
APPROVED	

XILINX® 2100 LOGIC DRIVE SAN JOSE, CALIFORNIA 95124

TITLE PCB, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM

SIZE	FSCM NO.	DWG NO.	REV.
B		1280415	01

SCALE 1 : 1 SHEET 1 OF 1