

# **Virtex-6 FPGA GTX Transceiver CPRI Electrical Standard**

## ***Characterization Summary Report***

RPT122 (v1.0) November 3, 2010



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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/03/10	1.0	Initial Xilinx release.

# Table of Contents

---

Revision History .....	2
<b>Virtex-6 FPGA GTX Transceiver CPRI Electrical Standard</b>	
Introduction .....	5
Test Conditions .....	5
Summary of Results .....	6
<b>Electrical Characterization Details</b> .....	15
Transmitter Near-End Output Eye .....	15
Test Methodology .....	15
Test Results .....	16
Transmitter Output Jitter .....	19
Test Methodology .....	19
Test Results .....	20
Transmitter Output Differential Amplitudes .....	24
Test Methodology .....	24
Test Results .....	25
Transmitter Output Rise and Fall Times .....	26
Test Methodology .....	26
Test Results .....	26
Transmitter Differential and Common Mode Output Return Loss .....	27
Test Methodology .....	27
Test Results .....	28
Receiver Input Jitter Tolerance .....	30
Test Methodology .....	30
Test Results .....	33
Receiver Differential and Common Mode Input Return Loss .....	35
Test Methodology .....	35
Test Results .....	36



# Virtex-6 FPGA GTX Transceiver CPRI Electrical Standard

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## Introduction

This protocol compatibility report compares the physical layer (PHY) electrical performance of the Virtex®-6 FPGA GTX transceiver against the Common Public Radio Interface (CPRI) specification, v4.1. The data presented in this report is extracted from the volume generic transceiver characterization across process, voltage, and temperature. The transmitter and receiver electrical characteristics were measured using a combination of lab bench setups and a high volume characterization (HVC) system. The methods used to characterize the transceiver are based on the standard specifications and also follow the best practice methods for some parameters.

The tests included in this report are:

- [Transmitter Near-End Output Eye, page 15](#)
- [Transmitter Output Jitter, page 19](#)
- [Transmitter Output Differential Amplitudes, page 24](#)
- [Transmitter Output Rise and Fall Times, page 26](#)
- [Transmitter Differential and Common Mode Output Return Loss, page 27](#)
- [Receiver Input Jitter Tolerance, page 30](#)
- [Receiver Differential and Common Mode Input Return Loss, page 35](#)

## Test Conditions

[Table 1](#) and [Table 2](#) show the supply voltage and temperature conditions used in the CPRI tests, respectively.

**Table 1: Supply Voltage Test Conditions**

Condition	MGTAVCC (V)	MGTAVTT (V)
V <sub>MIN</sub>	Note <sup>(1)</sup>	1.14
V <sub>MAX</sub>	Note <sup>(1)</sup>	1.26

**Notes:**

1. Depends on the speed grade and PLL frequency. See [DS152](#), *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics* for the MGTAVCC values.

Table 2: Temperature Test Conditions

Condition	Temperature (°C)
T <sub>-40</sub>	-40
T <sub>100</sub>	100

## Summary of Results

The summaries in [Table 3](#) through [Table 10](#) compare the Virtex-6 FPGA GTX transceiver against the CPRI specification requirements. Data reported in these tables represents the worst-case voltage, temperature, and performance corner tested. The results in this report represent line rates compatible with CPRI HV, LV, and LV-II technologies.

The test results presented in [Table 3](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, with a 650 Mb/s line rate and a 130 MHz reference clock frequency.

Table 3: Summary of CPRI Test Results for E.6.HV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter (DJ)		0.14			UI	-
Transmitter Total Jitter		0.279		0.07	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	1100	2000	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	85	327	115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	85	327	122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See <a href="#">Figure 15, page 28</a>	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See <a href="#">Figure 16, page 29</a>	dB	Yes
Differential Skew		25		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter		0.40		Note <sup>(3)</sup>	UI	Yes
Receiver Total Input Jitter Tolerance		0.66		Note <sup>(3)</sup>	UI	Yes

Table 3: Summary of CPRI Test Results for E.6.HV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
Receiver Differential Input Return Loss		Frequency Profile		See Figure 21, page 36	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See Figure 22, page 36	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.
3. The receiver jitter tolerance results are derived from [RPT124](#), *Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report* at a 3.125 Gb/s line rate. See [Table 8](#).

The test results presented in [Table 4](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, at the line rate of 1250 Mb/s and 125 MHz reference clock frequency.

Table 4: Summary of CPRI Test Results for E.12.HV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter		0.14		0.06	UI	Yes
Transmitter Total Jitter		0.279		0.11	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	1100	2000	Programmable <sup>(2)</sup>		mV p-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	85	327	115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	85	327	122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See Figure 15, page 28	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See Figure 16, page 29	dB	Yes
Differential Skew		25		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter		0.40		Note <sup>(3)</sup>	UI	Yes

Table 4: Summary of CPRI Test Results for E.12.HV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
Receiver Total Input Jitter Tolerance		0.66		Note <sup>(3)</sup>	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See Figure 21, page 36	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See Figure 22, page 36	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.
3. The receiver jitter tolerance results are derived from [RPT124](#), *Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report* at a 3.125 Gb/s line rate. See [Table 8](#).

The test results presented in [Table 5](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, with a 650 Mb/s line rate and a 130 MHz reference clock frequency. The CPRI E.6.LV transmitter and receiver parameters are based on the XAUI electrical interface (IEEE 802.3-2005 [1], clause 47).

Table 5: Summary of CPRI Test Results for E.6.LV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter		0.17			UI	–
Transmitter Total Jitter		0.35		0.07	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1600	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	60		115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	60		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See Figure 15, page 28	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See Figure 16, page 29	dB	Yes
Differential Skew		15		8	ps	Yes

Table 5: Summary of CPRI Test Results for E.6.LV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter		0.37		Note <sup>(3)</sup>	UI	Yes
Receiver Sinusoidal Jitter (SJ @ 20 MHz)		0.10		Note <sup>(3)</sup>	UI	Yes
Receiver Total Input Jitter Tolerance		0.65		Note <sup>(3)</sup>	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See Figure 21, page 36	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See Figure 22, page 36	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.
3. The receiver jitter tolerance results are derived from [RPT124](#), *Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report* at a 3.125 Gb/s line rate. See [Table 8](#).

The test results presented in [Table 6](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, with a 1250 Mb/s line rate and a 125 MHz reference clock frequency. The CPRI E.12.LV transmitter and receiver parameters are based on the XAUI electrical interface (IEEE 802.3-2005 [1], clause 47).

Table 6: Summary of CPRI Test Results for E.12.LV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter		0.17		0.06	UI	Yes
Transmitter Total Jitter		0.35		0.11	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1600	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	60		115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	60		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See Figure 15, page 28	dB	Yes

Table 6: Summary of CPRI Test Results for E.12.LV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
Transmitter Common Mode Output Return Loss		Frequency Profile		See <a href="#">Figure 16, page 29</a>	dB	Yes
Differential Skew		15		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter		0.37		Note <sup>(3)</sup>	UI	Yes
Receiver Sinusoidal Jitter (SJ@20 MHz)		0.10		Note <sup>(3)</sup>	UI	Yes
Receiver Total Input Jitter Tolerance		0.65		Note <sup>(3)</sup>	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See <a href="#">Figure 21, page 36</a>	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See <a href="#">Figure 22, page 36</a>	dB	Yes

**Notes:**

- These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
- The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366, Virtex-6 FPGA GTX Transceivers User Guide](#).
- The receiver jitter tolerance results are derived from [RPT124, Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report](#) at a 3.125 Gb/s line rate. See [Table 8](#).

The test results presented in [Table 7](#), unless otherwise noted, are derived from [RPT120, Virtex-6 FPGA GTX Transceiver Characterization Report](#), with a 2500 Mb/s line rate and a 100 MHz reference clock frequency. The CPRI E.24.LV transmitter and receiver parameters are based on the XAUI electrical interface (IEEE 802.3-2005 [1], clause 47).

Table 7: Summary of CPRI Test Results for E.24.LV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter		0.17		0.14	UI	Yes
Transmitter Total Jitter		0.35		0.25	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1600	Programmable <sup>(2)</sup>		mV p-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	60		115.1	131.3	ps	Yes

Table 7: Summary of CPRI Test Results for E.24.LV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
Transmitter Output Fall Time <sup>(1)</sup>	60		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See Figure 15, page 28	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See Figure 16, page 29	dB	Yes
Differential Skew		15		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter		0.37		Note <sup>(3)</sup>	UI	Yes
Receiver Sinusoidal Jitter (SJ @ 20 MHz)		0.10		Note <sup>(3)</sup>	UI	Yes
Receiver Total Input Jitter Tolerance		0.65		Note <sup>(3)</sup>	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See Figure 21, page 36	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See Figure 22, page 36	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the “Configurable TX Driver” section of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.
3. The receiver jitter tolerance results are derived from [RPT124](#), *Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report* at a 3.125 Gb/s line rate. See [Table 8](#).

The test results presented in [Table 8](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, with a 3200 Mb/s line rate and a 160 MHz reference clock frequency. The CPRI E.30.LV transmitter and receiver parameters are based on the XAUI electrical interface (IEEE 802.3-2005 [1], clause 47).

Table 8: Summary of CPRI Test Results for E.30.LV

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Deterministic Jitter		0.17		0.15	UI	Yes
Transmitter Total Jitter		0.35		0.26	UI	Yes

Table 8: Summary of CPRI Test Results for E.30.LV (Cont'd)

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1600	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	60		115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	60		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See Figure 15, page 28	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See Figure 16, page 29	dB	Yes
Differential Skew		15		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Deterministic Jitter <sup>(3)</sup>		0.37		0.464	UI	Yes
Receiver Sinusoidal Jitter (SJ @ 20 MHz) <sup>(3)</sup>		0.10		0.229	UI	Yes
Receiver Total Input Jitter Tolerance <sup>(3)</sup>		0.65		0.8736	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See Figure 21, page 36	dB	Yes
Receiver Common Mode Input Loss		Frequency Profile		See Figure 22, page 36	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.
3. The receiver jitter tolerance results are derived from [RPT124](#), *Virtex-6 FPGA GTX Transceiver XAUI Protocol Characterization Summary Report* at a 3.125 Gb/s line rate.

The test results presented in [Table 9](#), unless otherwise noted, are derived from [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*, with a 5000 Mb/s line rate and a 250 MHz reference clock frequency. The CPRI E.48.LV-II transmitter and receiver parameters are based on the CEI-6G-LR electrical interface (OIF-CEI-02.0[17], clause 7).

Table 9: Summary of CPRI Test Results for E.48.LV-II

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Total Jitter		0.30		0.25	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1200	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	30		115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	30		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See <a href="#">Figure 15, page 28</a>	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See <a href="#">Figure 16, page 29</a>	dB	Yes
Differential Skew		15		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Sinusoidal Jitter (SJ @ 22 kHz)		5		Note <sup>(3)</sup>	UI	Yes
Receiver Sinusoidal Jitter (SJ @ 28 MHz)		0.05		Note <sup>(3)</sup>	UI	Yes
Receiver Total Input Jitter Tolerance		0.825		Note <sup>(3)</sup>	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See <a href="#">Figure 21, page 36</a>	dB	Note <sup>(4)</sup>
Receiver Common Mode Input Loss		Frequency Profile		See <a href="#">Figure 22, page 36</a>	dB	Yes

**Notes:**

1. These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (.11000001111100...) generated internally in the FPGA logic.
2. The programmable transmitter output amplitude settings can be found in the “Configurable TX Driver” section of [UG366, Virtex-6 FPGA GTX Transceivers User Guide](#).
3. The receiver jitter tolerance results are derived from [RPT123, Virtex-6 FPGA GTX Transceiver CEI-6G Electrical Standard Characterization Report](#) at a 6.25 Gb/s line rate. See [Table 10](#).
4. Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTX transceiver meets or exceeds OIF-CEI-02.0.

The test results presented in [Table 10](#), unless otherwise noted, are derived from [RPT120, Virtex-6 FPGA GTX Transceiver Characterization Report](#), with a 6250 Mb/s line rate and a 312.5 MHz reference clock frequency. The CPRI E.60.LV-II transmitter and receiver parameters are based on the CEI-6G-LR electrical interface (OIF-CEI-02.0[17], clause 7).

Table 10: Summary of CPRI Test Results for E.60.LV-II

Test	CPRI Specification		Worst-Case Test Result		Units	Compatible
	Min	Max	Min	Max		
<b>Transmitter Specifications</b>						
Transmitter Total Jitter		0.30		0.28	UI	Yes
Transmitter Output Differential Amplitude <sup>(1)</sup>	800	1200	Programmable <sup>(2)</sup>		mVp-p	Yes
Transmitter Output Rise Time <sup>(1)</sup>	30		115.1	131.3	ps	Yes
Transmitter Output Fall Time <sup>(1)</sup>	30		122.5	137.3	ps	Yes
Transmitter Differential Output Return Loss		Frequency Profile		See <a href="#">Figure 15, page 28</a>	dB	Yes
Transmitter Common Mode Output Return Loss		Frequency Profile		See <a href="#">Figure 16, page 29</a>	dB	Yes
Differential Skew		15		8	ps	Yes
<b>Receiver Specifications</b>						
Receiver Sinusoidal Jitter (SJ @ 22 kHz) <sup>(3)</sup>		5		230	UI	Yes
Receiver Sinusoidal Jitter (SJ @ 28 MHz) <sup>(3)</sup>		0.05		0.0985	UI	Yes
Receiver Total Input Jitter Tolerance <sup>(3)</sup>		0.825		>0.825	UI	Yes
Receiver Differential Input Return Loss		Frequency Profile		See <a href="#">Figure 21, page 36</a>	dB	Note <sup>(4)</sup>
Receiver Common Mode Input Loss		Frequency Profile		See <a href="#">Figure 22, page 36</a>	dB	Yes

**Notes:**

- These tests were performed at 2.5 Gb/s with a five 1s and five 0s clock pattern (..11000001111100...) generated internally in the FPGA logic.
- The programmable transmitter output amplitude settings can be found in the "Configurable TX Driver" section of [UG366, Virtex-6 FPGA GTX Transceivers User Guide](#).
- The receiver jitter tolerance results are derived from [RPT123, Virtex-6 FPGA GTX Transceiver CEI-6G Electrical Standard Characterization Report](#) at a 6.25 Gb/s line rate.
- Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTX transceiver meets or exceeds OIF-CEI-02.0.

## Electrical Characterization Details

This section contains the test methodology and test results for each test summarized in Table 3 through Table 10. The GTX transceiver is configured using the Virtex-6 FPGA GTX Transceiver Wizard v1.6, including attribute settings. GTX attribute settings that differ from the GTX Wizard default setting are identified in the “Test Setup and Conditions” table for each test.

Table 11 shows the PLL settings during the characterization.

Table 11: Line Rate PLL Settings for E.6, E.12, E.24, E.30, E.48, E.60

CPRI	Line Rate (Gb/s)	PLL Frequency (GHz)	REFCLK Frequency (MHz)	TXPLL_DIVSEL_REF/ RXPLL_DIVSEL_REF	TXPLL_DIVSEL45_FB/ RXPLL_DIVSEL45_FB * TXPLL_DIVSEL_FB/ RXPLL_DIVSEL_FB	PLL_TXDIVSEL_OUT/ PLL_RXDIVSEL_OUT
E.60	6.144	3.072	307.2	1	5 x 2 = 10	1
E.48	4.9152	2.4576	307.2	1	4 x 2 = 8	1
E.30	3.072	1.536	153.6	1	5 x 2 = 10	1
E.24	2.4576	2.4576	122.88	1	5 x 4 = 20	2
E.12	1.2288	2.4576	122.88	1	5 x 4 = 20	4
E.6	0.6144	1.2288	122.88	1	5 x 2 = 10	4

## Transmitter Near-End Output Eye

### Test Methodology

The device is configured to transmit a PRBS7 pattern on each of the TX data pins, and the resulting eye is captured using an Agilent 86100C Infiniium DCA-J wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module at nominal voltage and room temperature conditions. The screen capture is provided as a representative diagram and is not intended to quantify the device performance. The driver settings might not be optimal on these measurements.

Table 12 defines the test setup and conditions for the transmitter near-end output eye.

Table 12: Transmitter Near-End Output Eye Test Setup and Conditions

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	Nominal
Temperature	Room temperature
Pattern	PRBS7
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board (FF1156) <sup>(1)</sup>
TX Amplitude	Maximum amplitude, TXDIFFCTRL = 4' b1111

Table 12: Transmitter Near-End Output Eye Test Setup and Conditions (Cont'd)

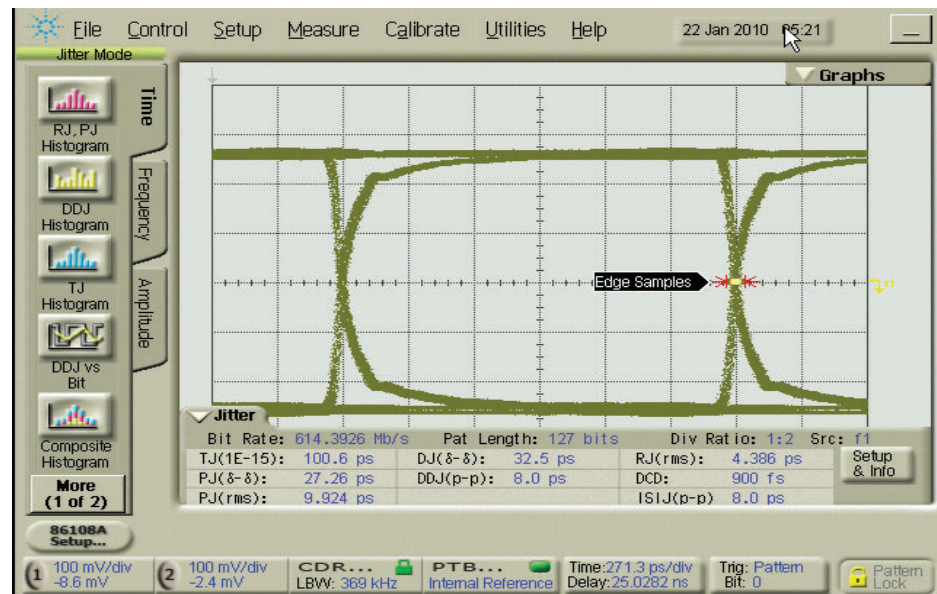
Parameter	Value
REFCLK	Sourced from Agilent 81133A pulse generator

**Notes:**

1. Refer to [UG724](#), *ML623 Virtex-6 FPGA GTX Transceiver Characterization Board User Guide* for more details.

**Test Results**

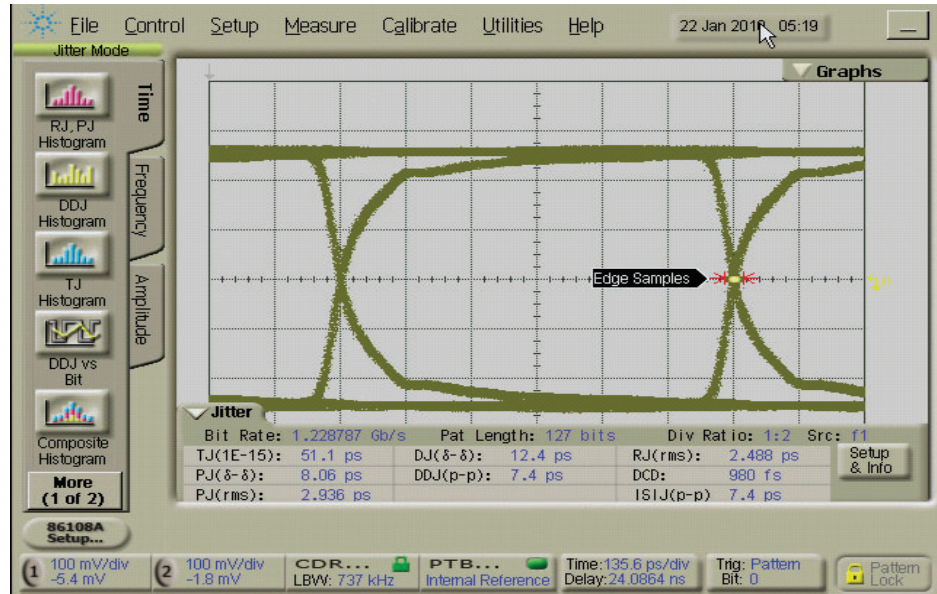
Figure 1 shows the transmitter near-end output eye at 0.6144 Gb/s with a 122.88 MHz reference clock frequency.



RPT122\_01\_051310

Figure 1: Transmitter Near-End Output Eye (0.6144 Gb/s)

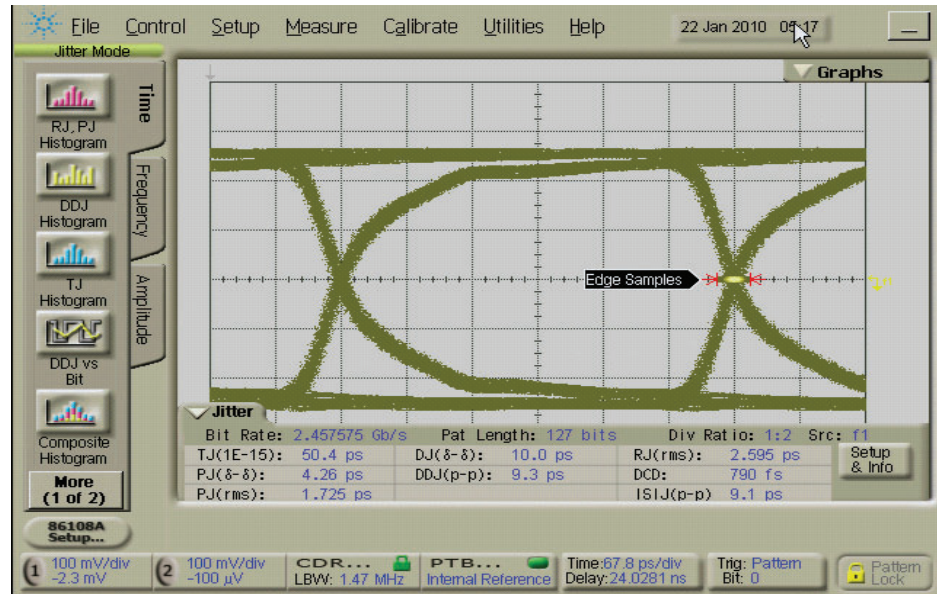
Figure 2 shows the transmitter near-end output eye at 1.2288 Gb/s with a 122.88 MHz reference clock frequency.



RPT122\_02\_051310

Figure 2: Transmitter Near-End Output Eye (1.2288 Gb/s)

Figure 3 shows the transmitter near-end output eye at 2.4576 Gb/s with a 122.88 MHz reference clock frequency.



RPT122\_03\_051310

Figure 3: Transmitter Near-End Output Eye (2.4576 Gb/s)

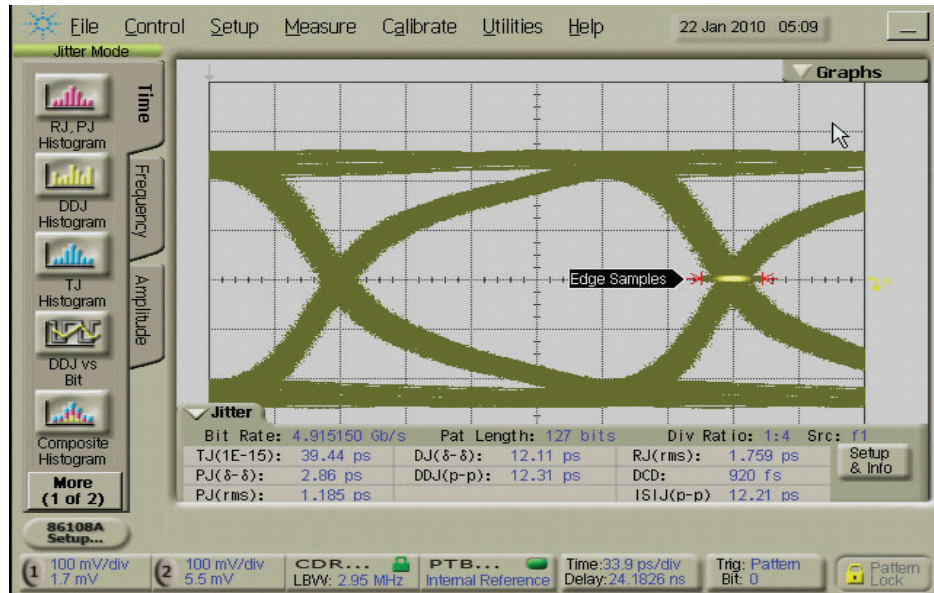
Figure 4 shows the transmitter near-end output eye at 3.072 Gb/s with a 153.6 MHz reference clock frequency.



RPT122\_04\_051310

Figure 4: Transmitter Near-End Output Eye (3.072 Gb/s)

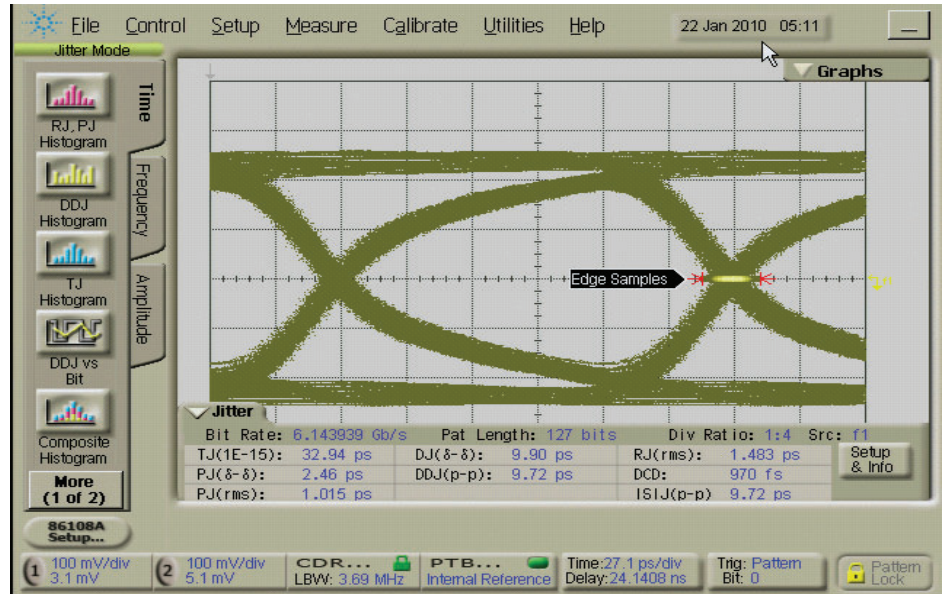
Figure 5 shows the transmitter near-end output eye at 4.9152 Gb/s with a 307.2 MHz reference clock frequency.



RPT122\_05\_051310

Figure 5: Transmitter Near-End Output Eye (4.9152 Gb/s)

Figure 6 shows the transmitter near-end output eye at 6.144 Gb/s with a 307.2 MHz reference clock frequency.



RPT122\_06\_051310

Figure 6: Transmitter Near-End Output Eye (6.144 Gb/s)

## Transmitter Output Jitter

### Test Methodology

TX jitter data was collected using the HVC system. Data for 12 transceiver channels is collected simultaneously. The primary instrument used to collect the data is an Agilent Parallel BERT (ParBERT) analyzer. The instrument determines the bit error rate (BER) at various sample points across the TX eye. The data is analyzed in the ParBERT and the resulting total jitter (TJ), deterministic jitter (DJ), and random jitter (RJ) are reported back to the controlling test program.

Table 13 defines the test setup and conditions for the transmitter output jitter.

Table 13: Transmitter Output Jitter Test Setup and Conditions

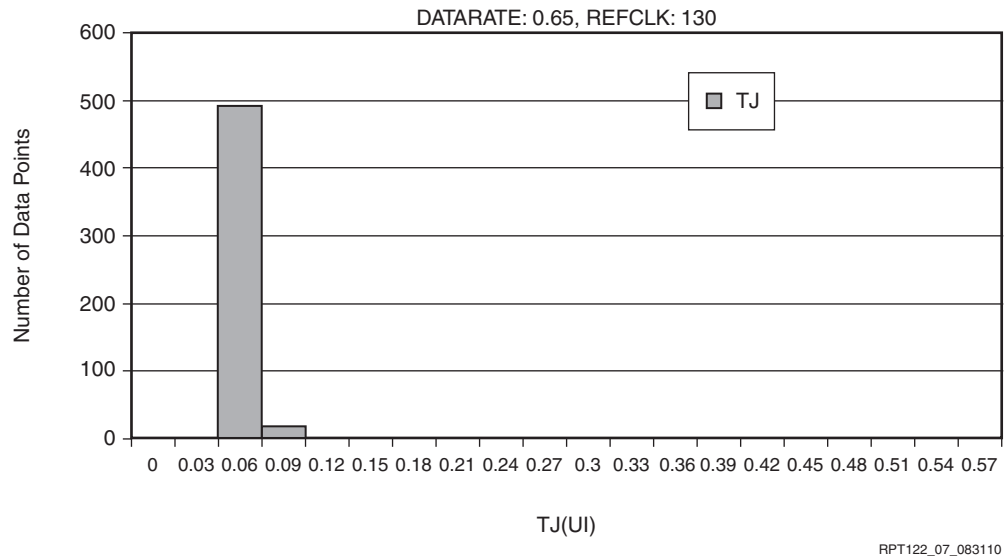
Parameter	Value
Measurement Instrument	HVC ParBERT Analyzer
TX Coupling	AC coupled using DC blocks
Voltage	$V_{MIN}$ , $V_{MAX}$
Temperature	$T_{-40}$ , $T_{100}$
Pattern	PRBS7
BER	$10^{-12}$
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)

**Table 13: Transmitter Output Jitter Test Setup and Conditions (Cont'd)**

Parameter	Value
TX Amplitude/Post-Emphasis	GTX transceiver attributes: <ul style="list-style-type: none"> <li>• TXDIFFCTRL = 4' b1111</li> <li>• TXBUFDIFFCTRL = 3' b100</li> <li>• TXPREEMPHASIS = 4' b0000</li> <li>• TXPOSTEMPHASIS = 5' b00000</li> </ul>
REFCLK	Sourced from Agilent ParBERT E4862B Module

**Test Results**

Figure 7 through Figure 12 show the output jitter test results with a PRBS7 pattern (BER of  $10^{-12}$ ). Tests were performed at line rate which are targeted for CPRI E.6, E.12, E.24, E.30, E.48, and E.60 requirements. The measured output jitter was not filtered and represents a pessimistic broadband jitter.



**Figure 7: Transmitter Output Jitter Test Results Targeted for E.6 @ 614.4 Mb/s**

Table 14 shows the maximum transmitter output jitter test result with a 650 Mb/s line rate, 130 MHz reference clock, PRBS7 pattern, and BER of  $10^{-12}$ .

**Table 14: Transmitter Output Jitter Test Results Targeted for E.6 @ 614.4 Mb/s**

Parameter	Pattern	BER	TJ (U)
Maximum Transmitter Output Jitter	PRBS7	$10^{-12}$	0.07

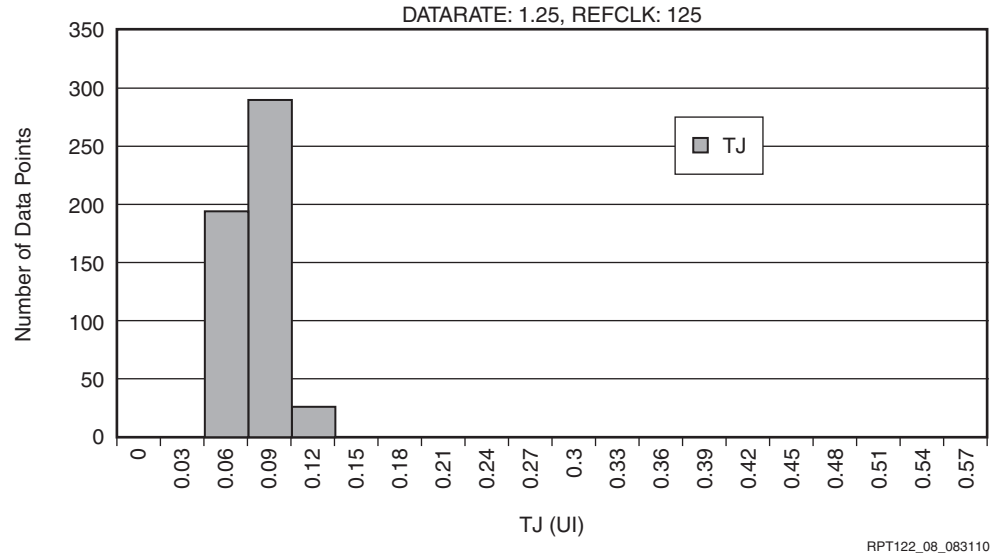


Figure 8: Transmitter Output Jitter Test Results Targeted for E.12 @ 1.2288 Gb/s

Table 15 shows the maximum transmitter output jitter test result with a 1250 Mb/s line rate, 125 MHz reference clock, PRBS7 pattern, and BER of  $10^{-12}$ .

Table 15: Transmitter Output Jitter Test Results Targeted for E.12 @ 1.2288 Gb/s

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ <sub>RMS</sub> (UI)
Maximum Transmitter Output Jitter	PRBS7	$10^{-12}$	0.11	0.06	0.08

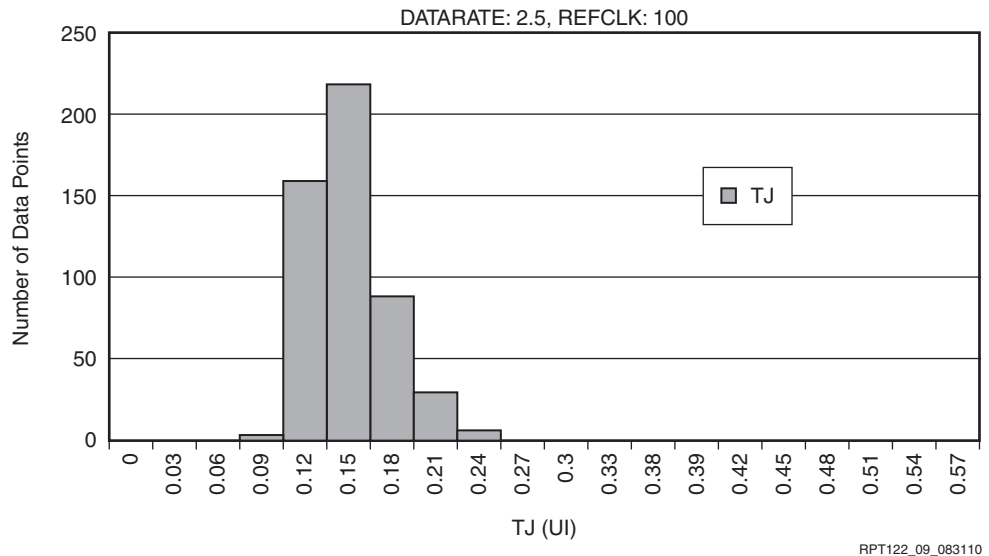


Figure 9: Transmitter Output Jitter Test Results Targeted for E.24 @ 2.4576 Gb/s

Table 16 shows the maximum transmitter output jitter test result with a 2500 Mb/s line rate, 100 MHz reference clock, PRBS7 pattern, and BER of  $10^{-12}$ .

Table 16: Transmitter Output Jitter Test Results Targeted for E.24 @ 2.4576 Gb/s

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ <sub>RMS</sub> (UI)
Maximum Transmitter Output Jitter	PRBS7	10 <sup>-12</sup>	0.25	0.14	0.17

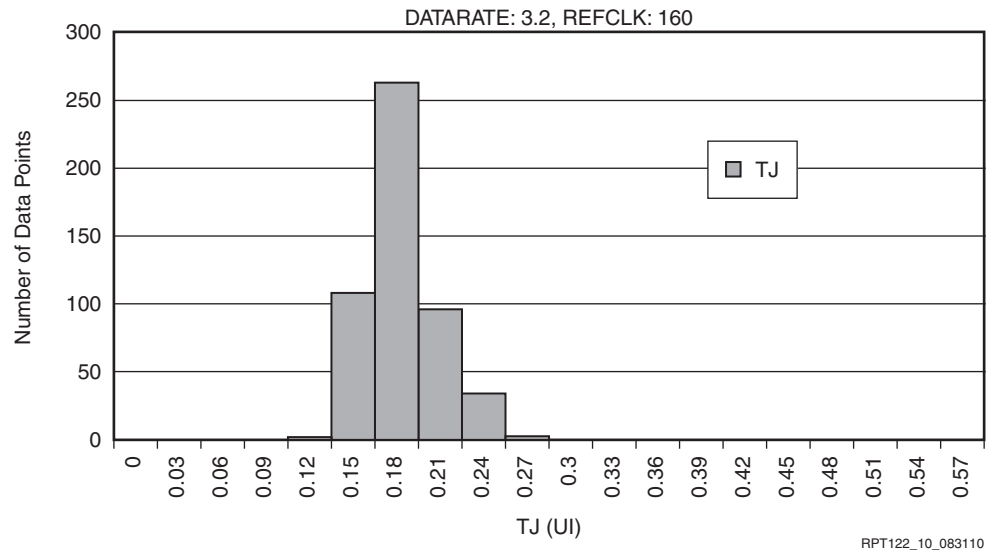


Figure 10: Transmitter Output Jitter Test Results Targeted for E.30 @ 3.072 Gb/s

Table 17 shows the maximum transmitter output jitter test result with a 3200 Mb/s line rate, 160 MHz reference clock, PRBS7 pattern, and BER of 10<sup>-12</sup>.

Table 17: Transmitter Output Jitter Test Results Targeted for E.30 @ 3.072 Gb/s

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ <sub>RMS</sub> (UI)
Maximum Transmitter Output Jitter	PRBS7	10 <sup>-12</sup>	0.26	0.15	0.23

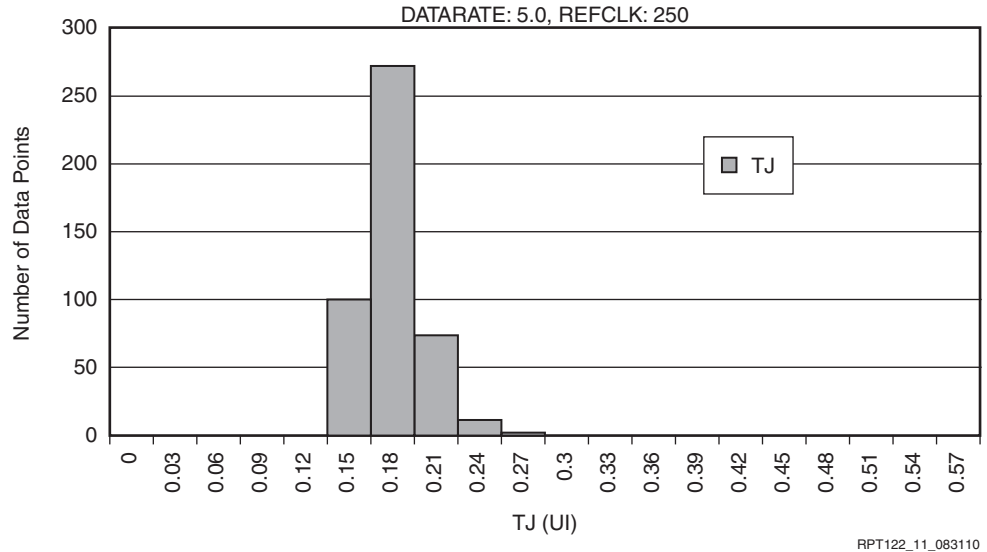


Figure 11: Transmitter Output Jitter Test Results Targeted for E.48 @ 4.9152 Gb/s

Table 18 shows the maximum transmitter output jitter test result with a 5000 Mb/s line rate, 250 MHz reference clock, PRBS7 pattern, and BER of  $10^{-12}$ .

Table 18: Transmitter Output Jitter Test Results Targeted for E.48 @ 4.9152 Gb/s

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ <sub>RMS</sub> (UI)
Maximum Transmitter Output Jitter	PRBS7	$10^{-12}$	0.25	0.13	0.16

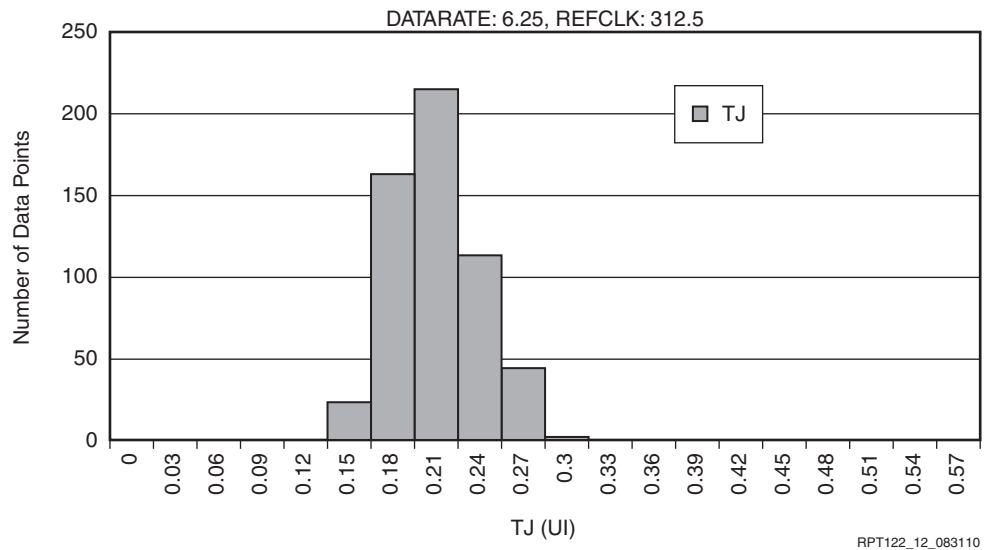


Figure 12: Transmitter Output Jitter Test Results Targeted for E.60 @ 6.144 Gb/s

Table 19 shows the maximum transmitter output jitter test result at 6250 Mb/s line rate with 312.5 MHz reference clock, PRBS7 pattern, and BER of  $10^{-12}$ .

Table 19: Transmitter Output Jitter Test Results Targeted for E.60 @ 6.144 Gb/s

Parameter	Pattern	BER	TJ (UI)	DJ (UI)	RJ <sub>RMS</sub> (UI)
Maximum Transmitter Output Jitter	PRBS7	10 <sup>-12</sup>	0.28	0.16	0.18

## Transmitter Output Differential Amplitudes

### Test Methodology

The transmitter output differential amplitudes are measured using the transmitter characterization bench setup as specified in [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*.

The TXDIFFCTRL parameter provides variable amplitude control to the transmitter. This test measures the varying amount of TX amplitude with each setting. Data was measured at TX line rate of 2.5 Gb/s with a five 1s and five 0s clock pattern to observe exclusively the effects of varying the TXDIFFCTRL. This is a typical representation of GTX transceiver behavior at CPRI E.6, E.12, E.24, E.30, E.48, and E.60 line rates. [Table 20](#) defines the test setup and conditions.

Table 20: Transmitter Output Differential Amplitude Test Setup and Conditions

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope
TX Coupling	AC coupled using DC blocks
Voltage	V <sub>MIN</sub> , V <sub>MAX</sub>
Temperature	T <sub>-40</sub> , T <sub>100</sub>
Pattern	Five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
TX Amplitude/Post-Emphasis	GTX transceiver attributes: <ul style="list-style-type: none"> <li>• TXDIFFCTRL = from 4'b0000 to 4'b1111 (programmable)</li> <li>• TXBUFDIFFCTRL = 3'b100</li> <li>• TXPREEMPHASIS = 4'b0000</li> <li>• TXPOSTEMPHASIS = 5'b00000</li> </ul>
REFCLK	125 MHz sourced from Agilent 81133A pulse generator

### Test Results

The transmitter output differential amplitude test results are shown in [Figure 13](#) and [Table 21](#).

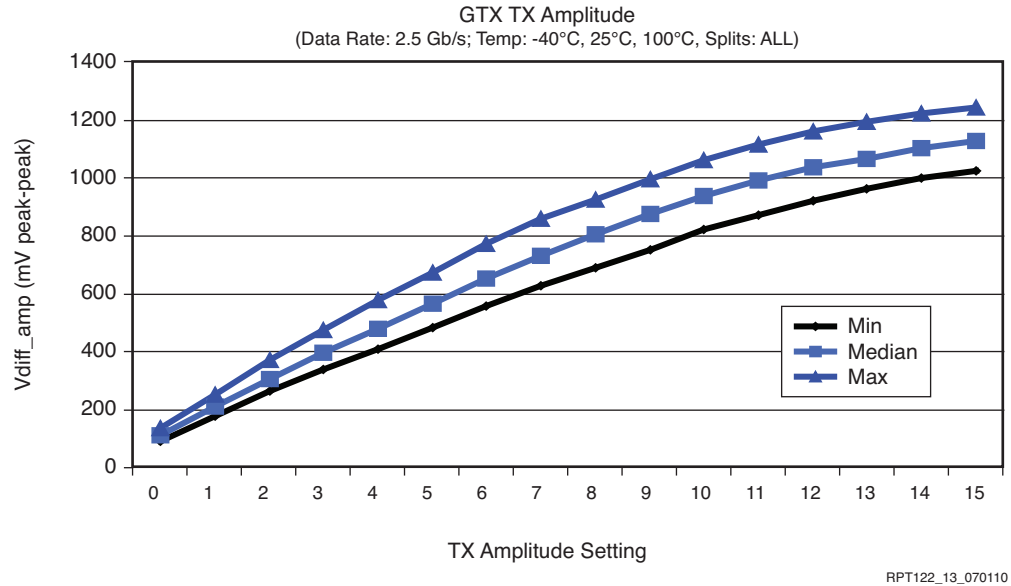


Figure 13: Transmitter Output Differential Amplitude

Table 21: TX Amplitude (2500 Mb/s, 125 MHz)

Parameter	Min	Max	Avg	Stdev	Units
TX Amplitude 0	90	140	110	10	mV
TX Amplitude 1	180	250	210	20	mV
TX Amplitude 2	270	370	310	20	mV
TX Amplitude 3	340	480	400	30	mV
TX Amplitude 4	410	580	480	40	mV
TX Amplitude 5	480	680	570	40	mV
TX Amplitude 6	560	780	660	50	mV
TX Amplitude 7	630	860	740	50	mV
TX Amplitude 8	690	930	810	50	mV
TX Amplitude 9	760	1000	880	60	mV
TX Amplitude 10	820	1070	940	60	mV
TX Amplitude 11	880	1120	990	60	mV
TX Amplitude 12	920	1160	1040	60	mV
TX Amplitude 13	970	1200	1080	60	mV
TX Amplitude 14	1000	1230	1110	60	mV
TX Amplitude 15	1030	1250	1130	60	mV

## Transmitter Output Rise and Fall Times

### Test Methodology

The transmitter output rise and fall times are measured using the transmitter characterization bench setup as specified in [RPT120](#), *Virtex-6 FPGA GTX Transceiver Characterization Report*. Due to board limitations, the measurement is taken with approximately 4 to 11 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML623 board. Data was measured at TX line rate of 2.5 Gb/s with a five 1s and five 0s clock pattern. This is a typical representation of GTX transceiver behavior at CPRI E.6, E.12, E.24, E.30, E.48, and E.60 line rates. [Table 22](#) defines the test setup and conditions.

**Table 22: Transmitter Output Rise and Fall Time Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope
TX Coupling	AC coupled using DC blocks
Voltage	$V_{MIN}$ , $V_{MAX}$
Temperature	$T_{-40}$ , $T_{100}$
Pattern	Five 1s and five 0s clock pattern (...11000001111100...) generated internally in the FPGA logic
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
TX Amplitude/Post-Emphasis	GTX transceiver attributes: <ul style="list-style-type: none"> <li>• TXDIFFCTRL = 4'b1111</li> <li>• TXBUFDIFFCTRL = 3'b100</li> <li>• TXPREEMPHASIS = 4'b0000</li> <li>• TXPOSTEMPHASIS = 5'b00000</li> </ul>
REFCLK	125 MHz sourced from Agilent 81133A pulse generator

### Test Results

The transmitter output rise and fall time test results are shown in [Table 23](#) and [Table 24](#).

**Table 23: Transmitter Output Rise Time Test Results**

Parameter	Min	Max	Units
Output Rise Time (TXDIFFCTRL = 4'b1111)	115.1	131.3	ps

**Table 24: Transmitter Output Fall Time Test Results**

Parameter	Min	Max	Units
Output Fall Time (TXDIFFCTRL = 4'b1111)	122.5	137.3	ps

## Transmitter Differential and Common Mode Output Return Loss

### Test Methodology

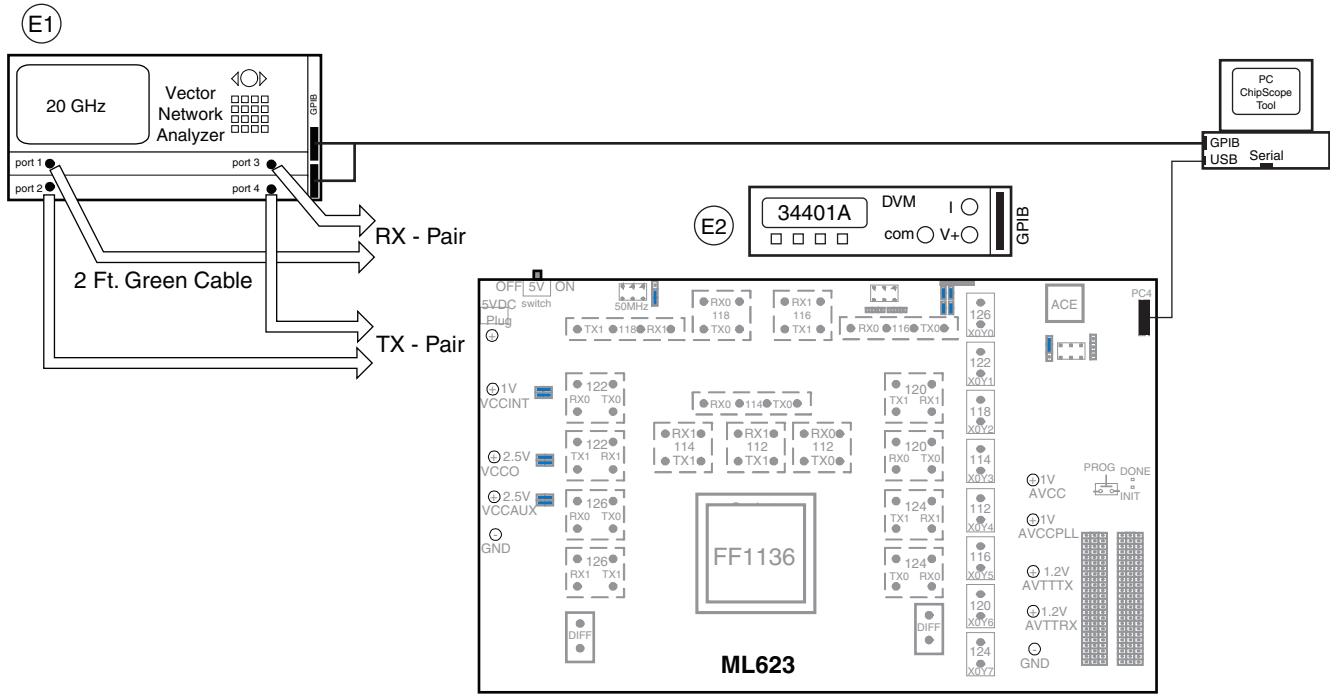
The Vector Network Analyzer (VNA) interfaces to the host PC through the GPIB. After the measurement parameters are set, calibration begins. Four cables are included in the calibration process. VNA measurements are independent of voltage and are accurate up to 11 GHz. A digital multimeter (DVM) confirms the differential resistance is 100Ω before the measurement.

Table 25 defines the test setup and conditions.

**Table 25: Transmitter Differential and Common Mode Output Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES Vector Network Analyzer
TX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical voltage
Temperature	Room temperature
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Test Fixture	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

Figure 14 shows the setup for the return loss measurement.

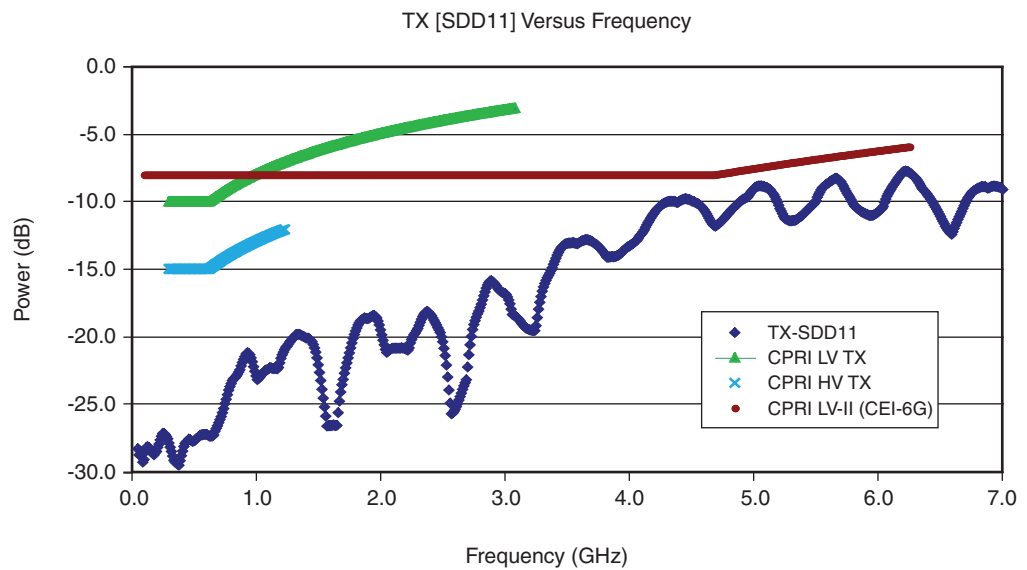


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Figure 14: Return Loss Test Setup Block Diagram

### Test Results

Figure 15 shows the transmitter differential output return loss measurement.



RPT122\_15\_072910

Figure 15: Transmitter Differential Output Return Loss Measurement

Figure 16 shows the transmitter common mode output return loss measurement.

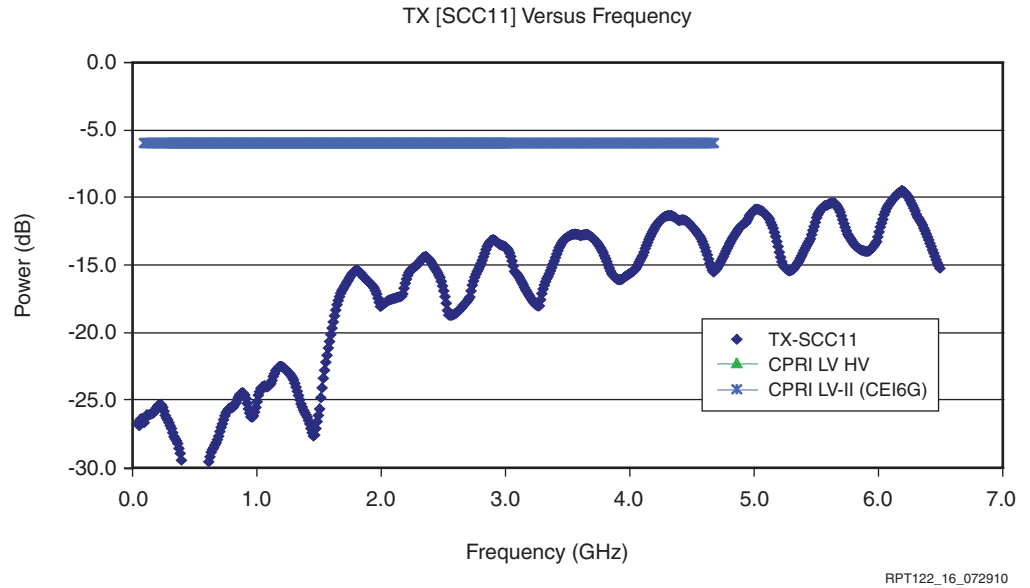


Figure 16: Transmitter Common Mode Output Return Loss Measurement (Informative)

# Receiver Input Jitter Tolerance

## Test Methodology

The receiver input jitter tolerance is measured using the test setup shown in [Figure 17](#).

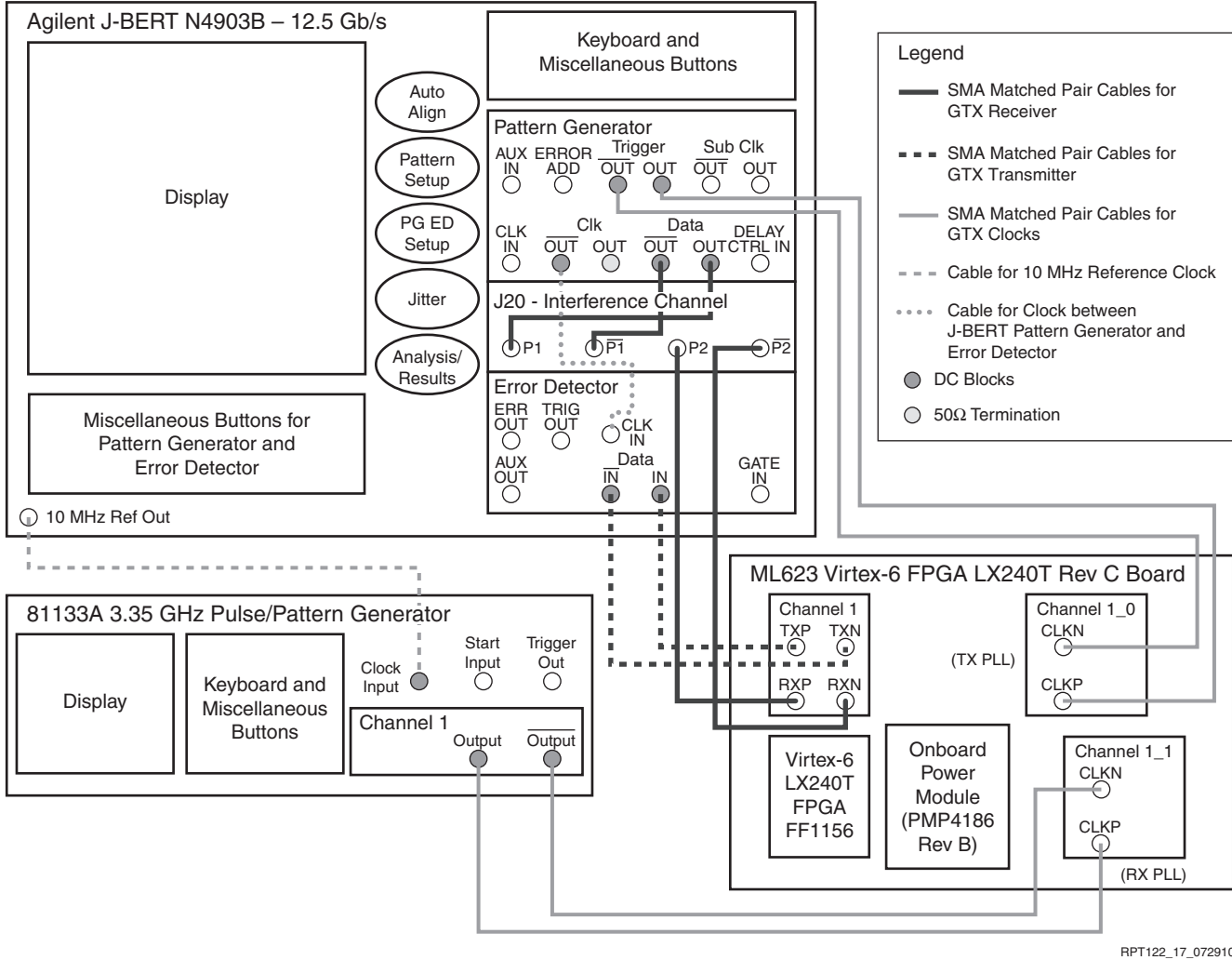


Figure 17: Receiver Jitter Tolerance Setup Block Diagram

For the CPRI HV and LV receiver input jitter tolerance test, the J-BERT generates a CJPAT pattern with random jitter (RJ) and deterministic jitter (DJ) per IEEE 802.3-2005 clause 47 specifications. DJ in the form of intersymbol interference (ISI) and bounded uncorrelated jitter (BUJ) are added with the Agilent built-in features. ISI is added by using Agilent J-BERT interference channel feature (option J20) by selecting 24 inches of board trace (Nelco 4000-6). Sinusoidal jitter (SJ) is swept from 1 kHz to 80 MHz. The GTX transceiver under test recovers the data and transmits the pattern back to the Error Detector input of the J-BERT, where bit errors are measured. The test is performed with a +200 and -200 PPM offset between the J-BERT data generator and the reference clock provided to the GTX transceiver under test.

For the CPRI LV-II receiver input jitter tolerance test, the J-BERT pattern generator data output amplitude is set to 800 mV, and it generates a PRBS31 pattern with RJ and BUJ per

OIF-CEI-02.0. DJ in the form of ISI is added with 20 inches of board trace (Nelco 4000-6) by using the Agilent J-BERT interference channel feature (option 20). Sinusoidal jitter (SJ) is swept from 1 kHz to 80 MHz. The GTX transceiver under test recovers the data and transmits the pattern back to the Error Detector input of the J-BERT, where bit errors are measured. The test is performed with a +200 and -200 PPM offset between the J-BERT data generator and the reference clock provided to the GTX transceiver under test.

Table 26 defines the test setup and conditions for CPRI HV and LV receiver jitter tolerance.

Table 26: Receiver Jitter Tolerance Test Setup and Conditions (CPRI HV and LV)

Parameter	Value
Measurement Instrument	Agilent J-BERT N4903B
RX Coupling	AC coupled using DC blocks
Voltage	$V_{MIN}$ , $V_{MAX}$
Temperature	$T_{-40}$ , $T_{100}$
Pattern	CJPAT
Injected Jitter	Sum of these values: <ul style="list-style-type: none"> <li>• RJ = 0.1806 UI<sub>P-P</sub></li> <li>• DJ = 0.2740 UI<sub>P-P</sub> (with 24 inches of interference channel)</li> <li>• BUJ = 0.1900 UI<sub>P-P</sub></li> <li>• SJ = Tested to failure; Frequency sweep = {1 kHz - 80 MHz}</li> </ul>
BER	$10^{-12}$ (measured at $10^{-9}$ , extrapolated to $10^{-12}$ )
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
Attributes	GTX transceiver attributes: <ul style="list-style-type: none"> <li>• PMA_RX_CFG = 25'h05ce049</li> <li>• RXEQMIX = 3'b110</li> <li>• DFE Disabled:               <ul style="list-style-type: none"> <li>• DFETAP1[3:0] = 4'b0000</li> <li>• DFETAP2[3:0] = 4'b0000</li> <li>• DFETAP3[3:0] = 4'b0000</li> <li>• DFETAP4[3:0] = 4'b0000</li> </ul> </li> </ul>
REFCLK	156.25 MHz sourced from the J-BERT. 156.25 MHz ± 200 PPM offset from the Agilent 81133A pulse generator

Table 27 defines the test setup and conditions for CPRI LV-II receiver jitter tolerance.

Table 27: Receiver Jitter Tolerance Test Setup and Conditions (CPRI LV-II)

Parameter	Value
Measurement Instrument	Agilent J-BERT N4903B
RX Coupling	AC coupled using DC blocks
Voltage	$V_{MIN}$ , $V_{MAX}$
Temperature	$T_{-40}$ , $T_0$ , $T_{100}$

Table 27: Receiver Jitter Tolerance Test Setup and Conditions (CPRI LV-II) (Cont'd)

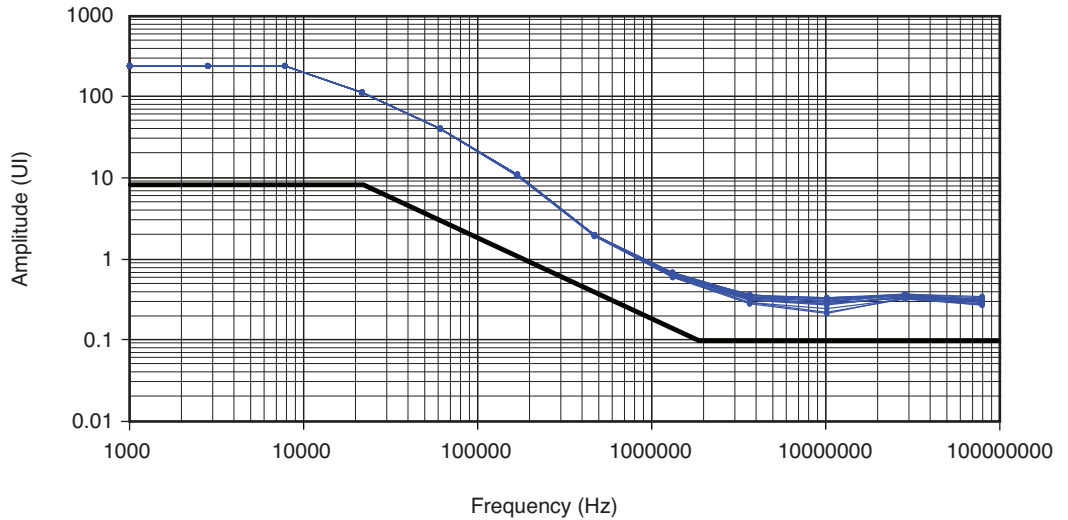
Parameter	Value
Pattern	PRBS31
Injected Jitter	Sum of these values: <ul style="list-style-type: none"> <li>• RJ = 0.150 UI<sub>P-P</sub></li> <li>• BUJ = 0.150 UI<sub>P-P</sub></li> <li>• DJ ≥ 0.525 UI<sub>P-P</sub></li> <li>• SJ = Tested to failure; Frequency sweep = {1 kHz - 80 MHz}</li> </ul>
BER	10 <sup>-15</sup> (measured at 10 <sup>-9</sup> , extrapolated to 10 <sup>-15</sup> )
Load Board	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
Attributes	GTX transceiver attributes: <ul style="list-style-type: none"> <li>• PMA_CDR_SCAN = 27'h640404c</li> <li>• PMA_RX_CFG = 25'h05ce045</li> <li>• RXEQMIX = 3'b110</li> <li>• DFE Enabled: <ul style="list-style-type: none"> <li>• DFCLKDLYADJ = 6'b000000</li> <li>• DFETAP1[4:0] = Self-adapting<sup>(1)</sup></li> <li>• DFETAP2[4:0] = Self-adapting<sup>(1)</sup></li> <li>• DFETAP3[3:0] = Self-adapting<sup>(1)</sup></li> <li>• DFETAP4[3:0] = Self-adapting<sup>(1)</sup></li> <li>• DFE_CAL_TIME[4:0] = 5'b01100</li> <li>• DFE_CFG[7:0] = 8'b00011011</li> </ul> </li> </ul>
REFCLK	390.625 MHz sourced from the J-BERT. 390.625 MHz ± 200 PPM offset from the Agilent 81133A pulse generator

**Notes:**

1. DFETAPOVRD is set to 0 to obtain the optimized self-adapting DFE values. The DFE tap values are captured from the DFETAP<sub>n</sub>MONITOR and DFETAPOVRD is set to 1. The captured DFE tap values are written to each DFETAP<sub>n</sub> port accordingly ( $n = 1, 2, 3, \text{ and } 4$ ).

### Test Results

Figure 18 shows the receiver jitter tolerance SJ sweep for CPRI HV and LV receiver jitter tolerance test. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 26.



RPT122\_18\_070110

Figure 18: CPRI HV and LV Receiver Jitter Tolerance SJ Sweep Test Results (CJPAT, BER = 10<sup>-12</sup>)

Table 28 shows the CPRI HV and LV minimum total receiver jitter tolerance performance.

Table 28: CPRI HV and LV Receiver Jitter Tolerance Test Results

Jitter Tolerance Parameter	BER	Minimum Tolerance	Units
SJ @ 10.3 MHz	10 <sup>-12</sup>	0.219	UI
TJ	10 <sup>-12</sup>	0.864	UI

Figure 19 shows the jitter tolerance SJ sweep for CPRI LV-II. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 27.

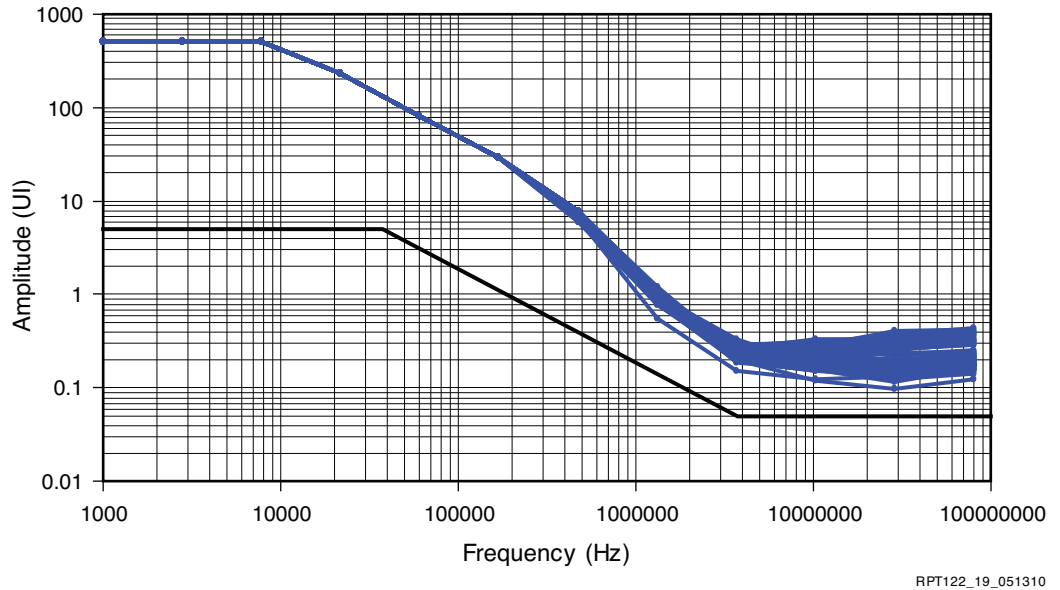


Figure 19: CPRI LV-II Receiver Jitter Tolerance SJ Sweep Test Results (PRBS31, BER = 10<sup>-15</sup>)

Figure 20 shows the SJ at 28 MHz for CPRI LV-II. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 27.

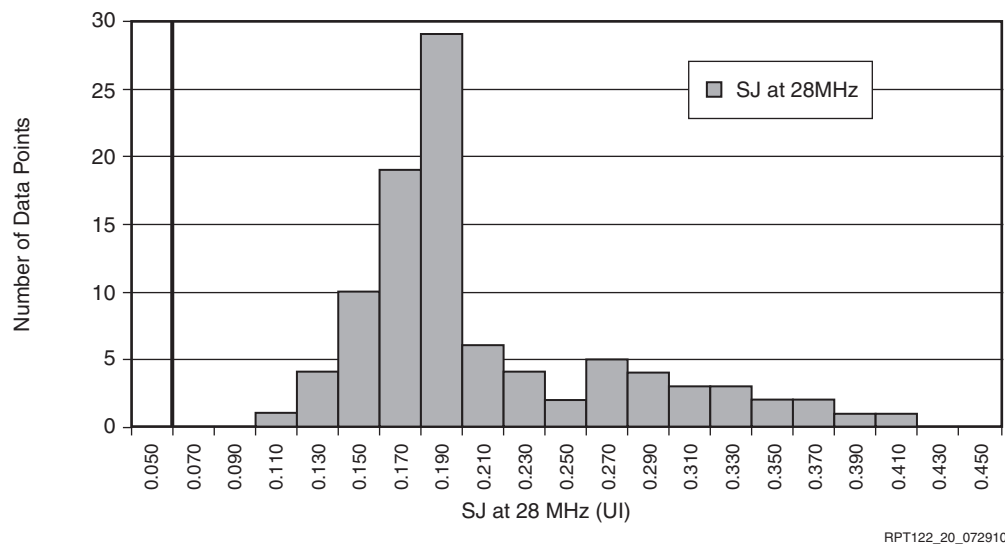


Figure 20: CPRI LV-II Receiver Sinusoidal Jitter Tolerance at 28 MHz Test Results (PRBS31, BER = 10<sup>-15</sup>)

Table 29 shows the minimum CPRI LV-II receiver SJ tolerance for both 22 kHz and 28 MHz. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 27.

**Table 29: CPRI LV-II Receiver Jitter Tolerance Test Results**

Parameter	Test Condition	BER	Minimum SJ Tolerance	Units
Receiver Jitter Tolerance	SJ @ 22 kHz	$10^{-15}$	230	UI
	SJ @ 28 MHz	$10^{-15}$	0.0985	UI

## Receiver Differential and Common Mode Input Return Loss

### Test Methodology

The receiver input differential and common mode return loss specification and setup are the same as the transmitter return loss setup in Figure 14. Table 30 defines the test setup and conditions.

**Table 30: Receiver Differential and Common Mode Input Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES Vector Network Analyzer
RX Configuration/Amplitude	RX is configured for 100Ω differential termination (center tap to GND), and AC coupled using both internal and external capacitors
Voltage	Typical voltage
Temperature	Room temperature
Frequency Sweep	50 MHz to 11 GHz (10 MHz steps)
Test Fixture	ML623 Virtex-6 FPGA GTX Transceiver Characterization Board, Revision C (FF1156)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

### Test Results

Figure 21 shows the receiver differential input return loss measurement.

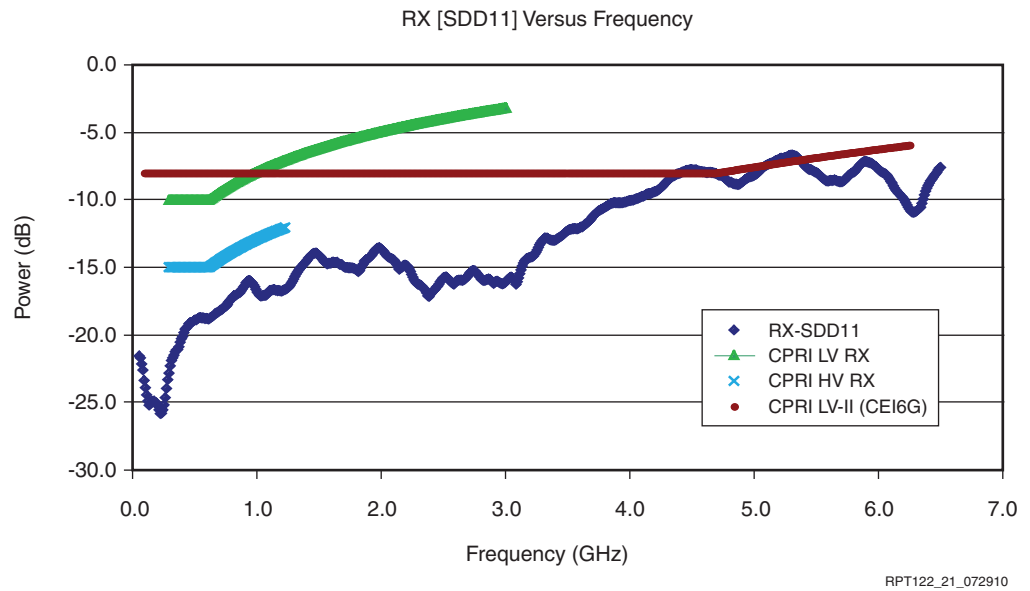


Figure 21: Receiver Differential Input Return Loss Measurement

Figure 22 shows the receiver common mode input return loss measurement.

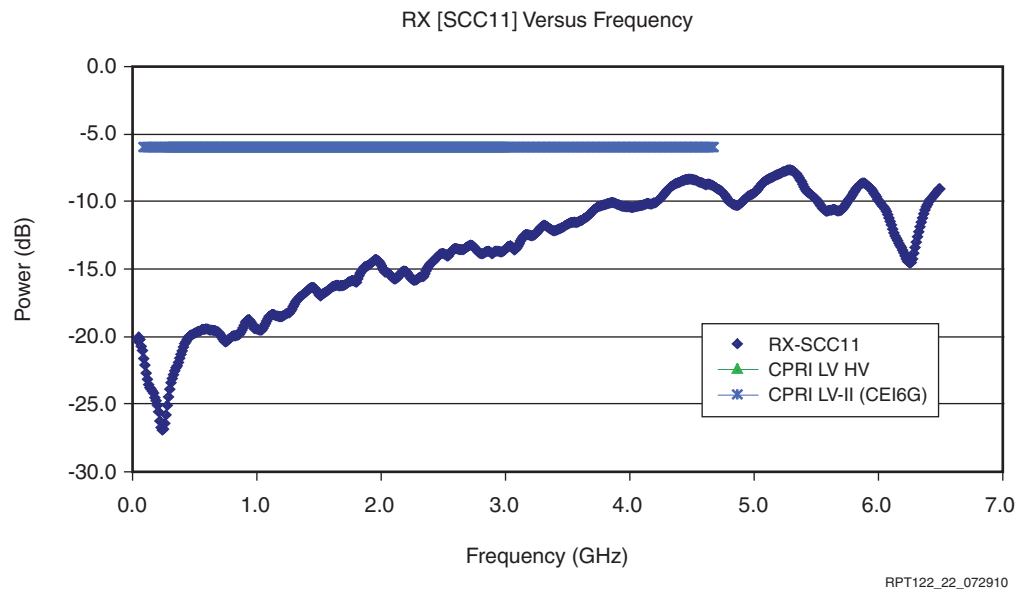


Figure 22: Receiver Common Mode Input Return Loss Measurement