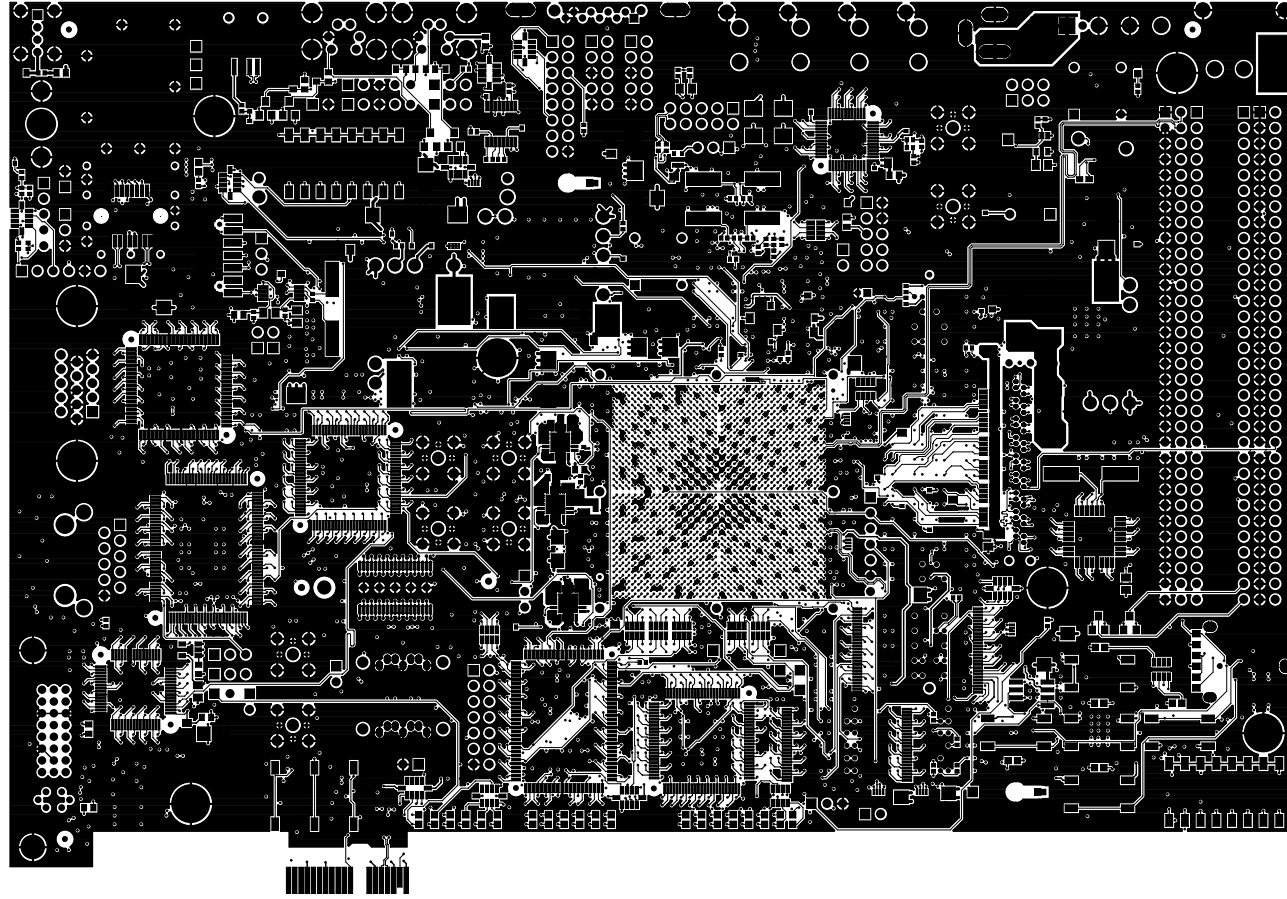
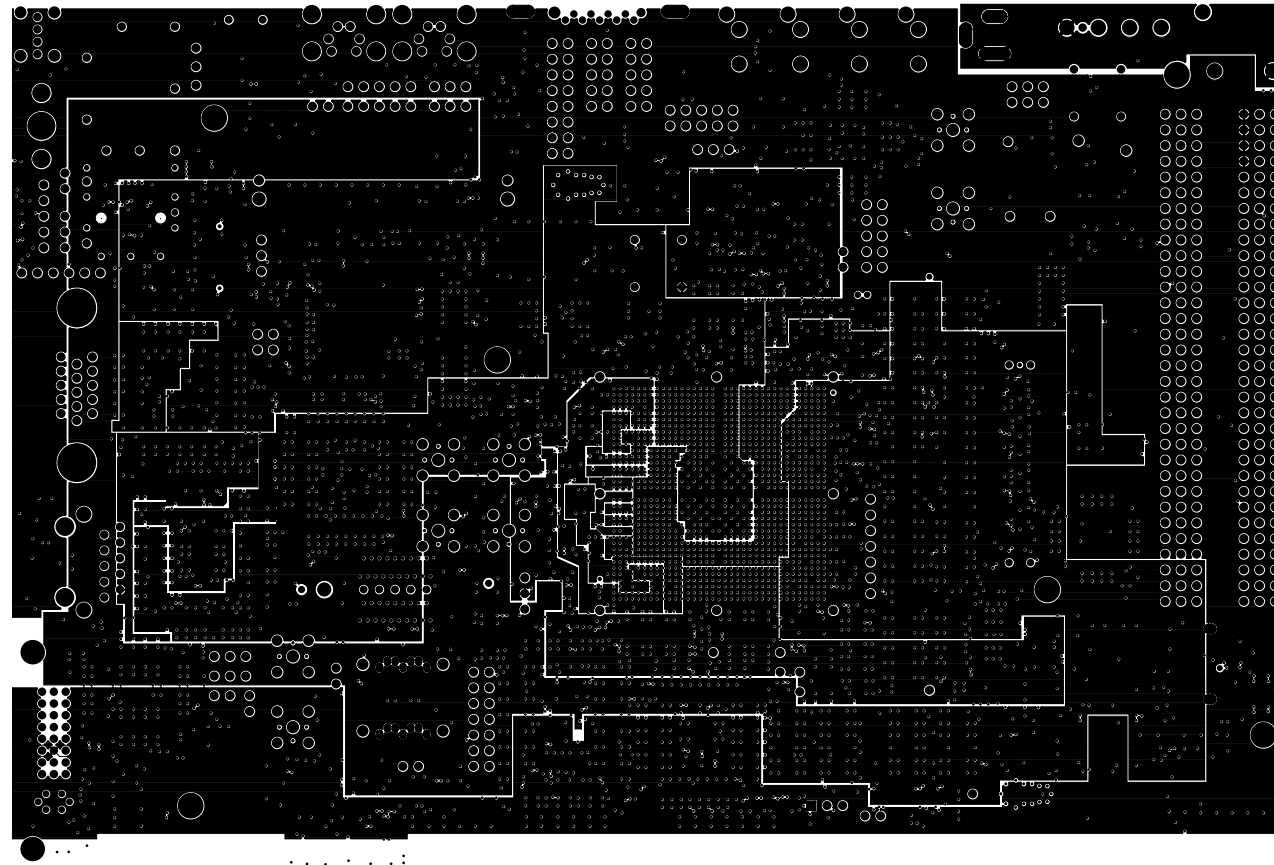
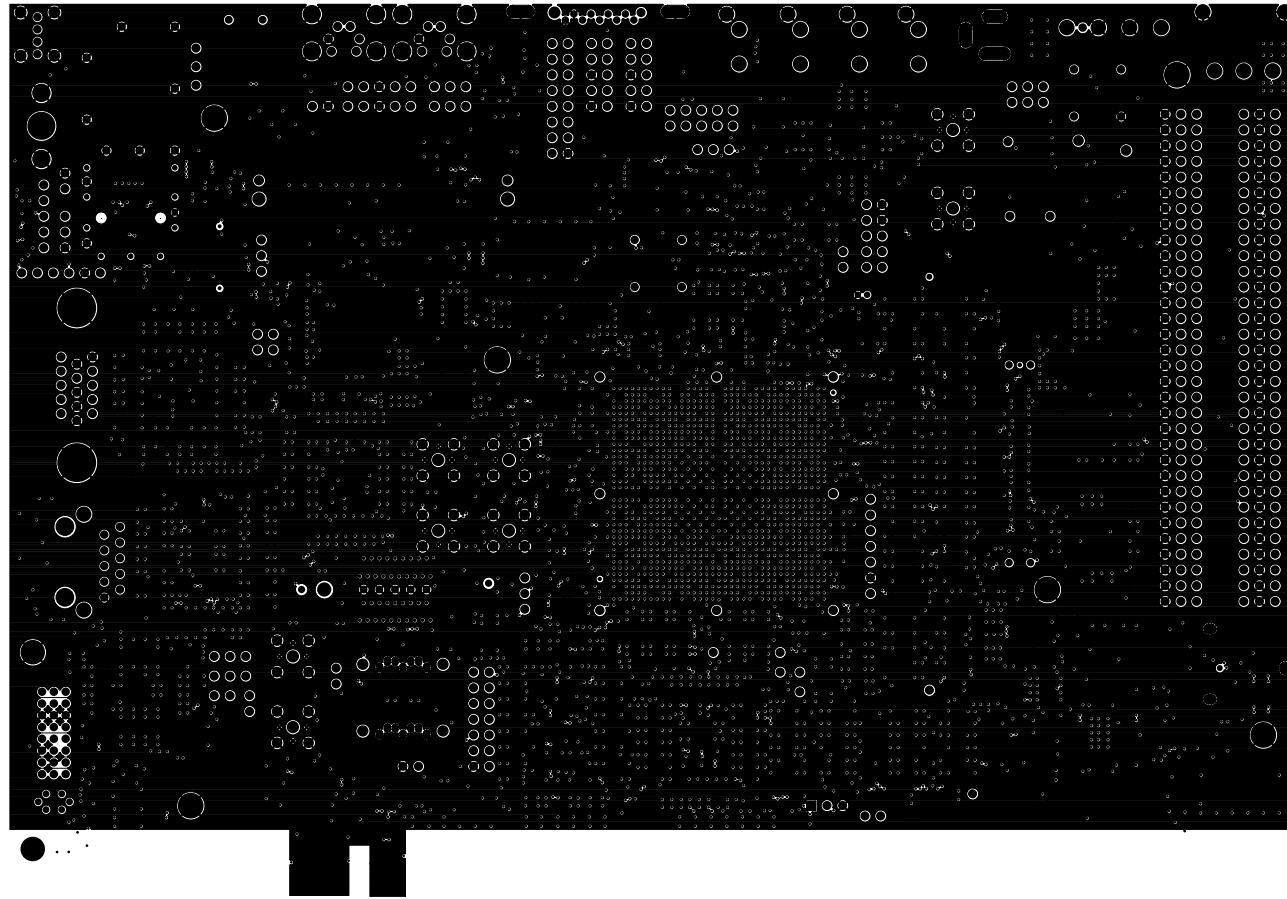


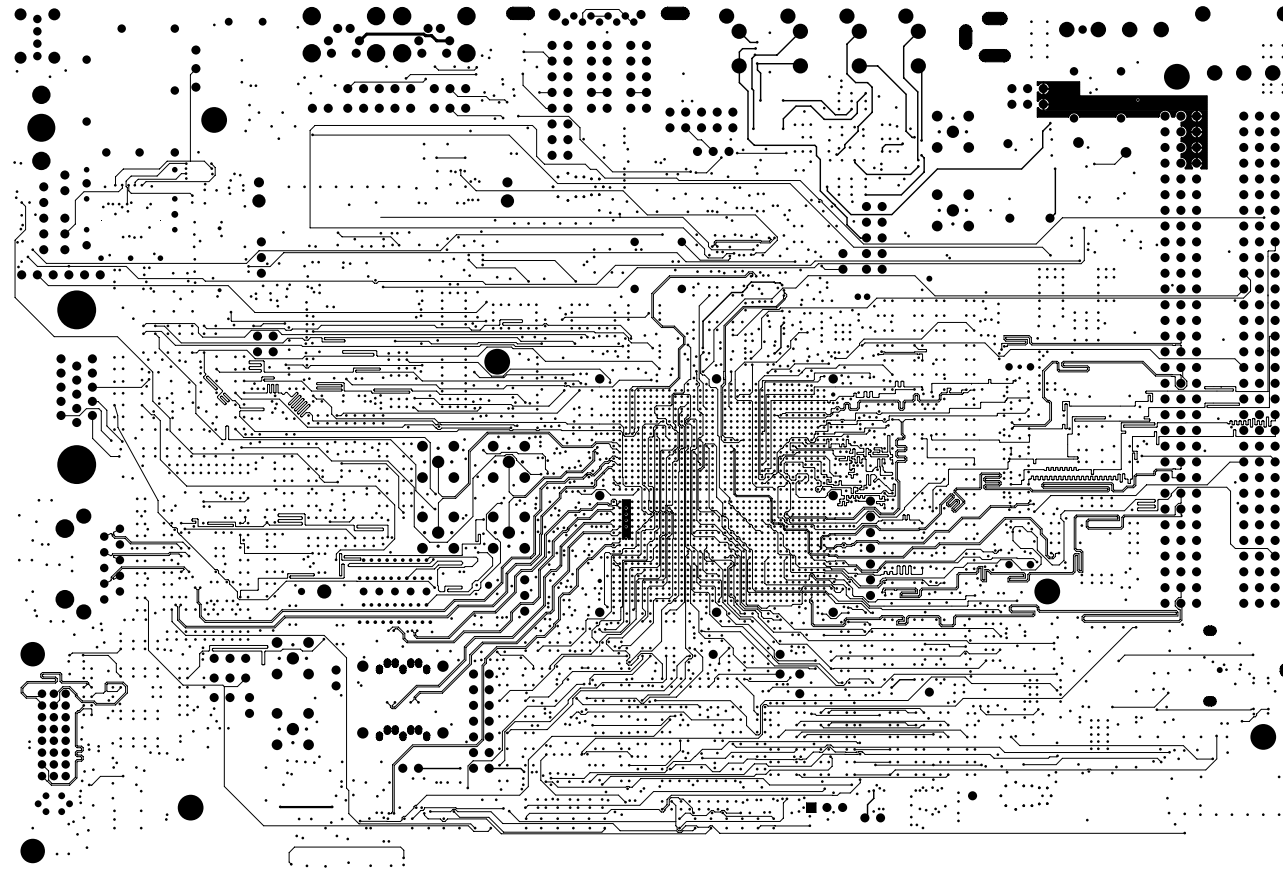


ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 01 OF 25 L1_TOP

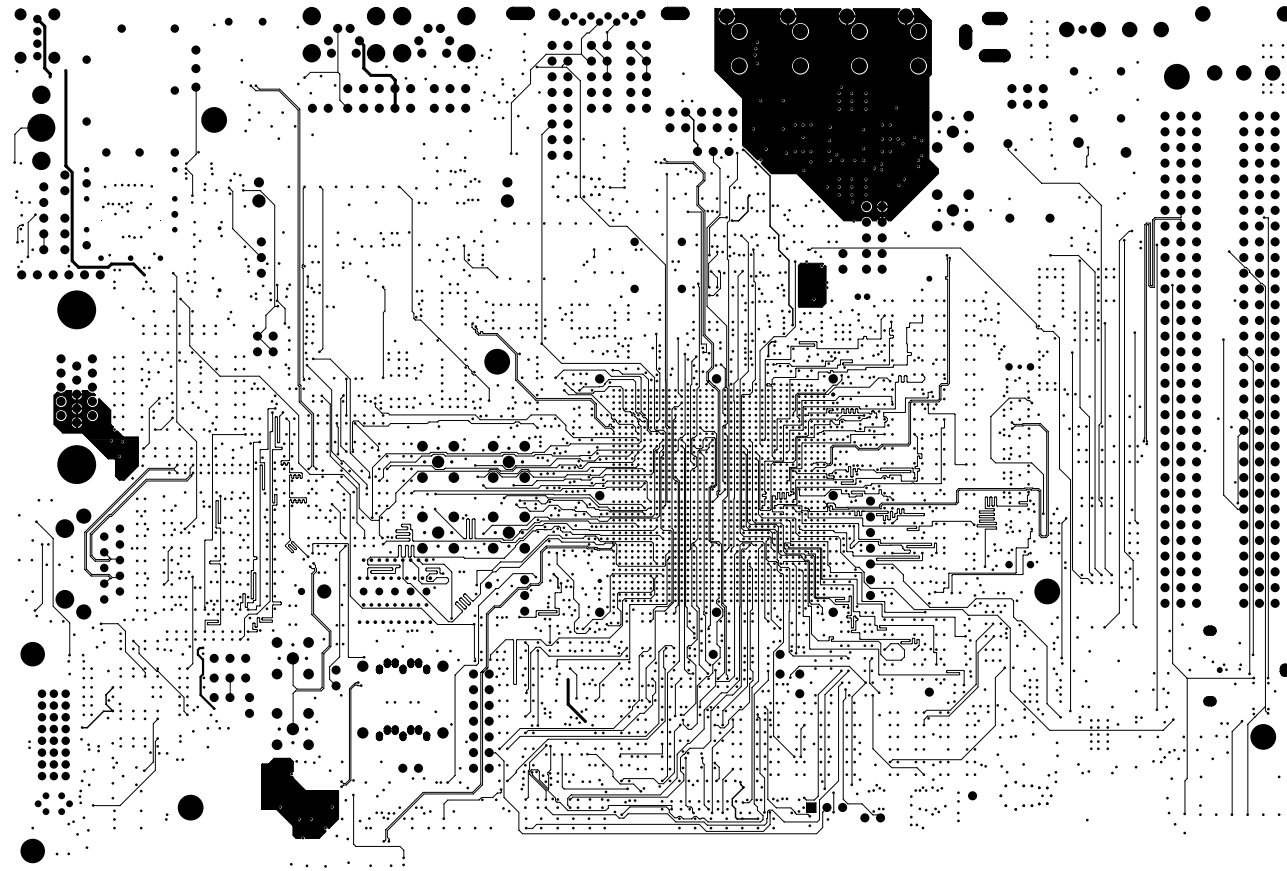




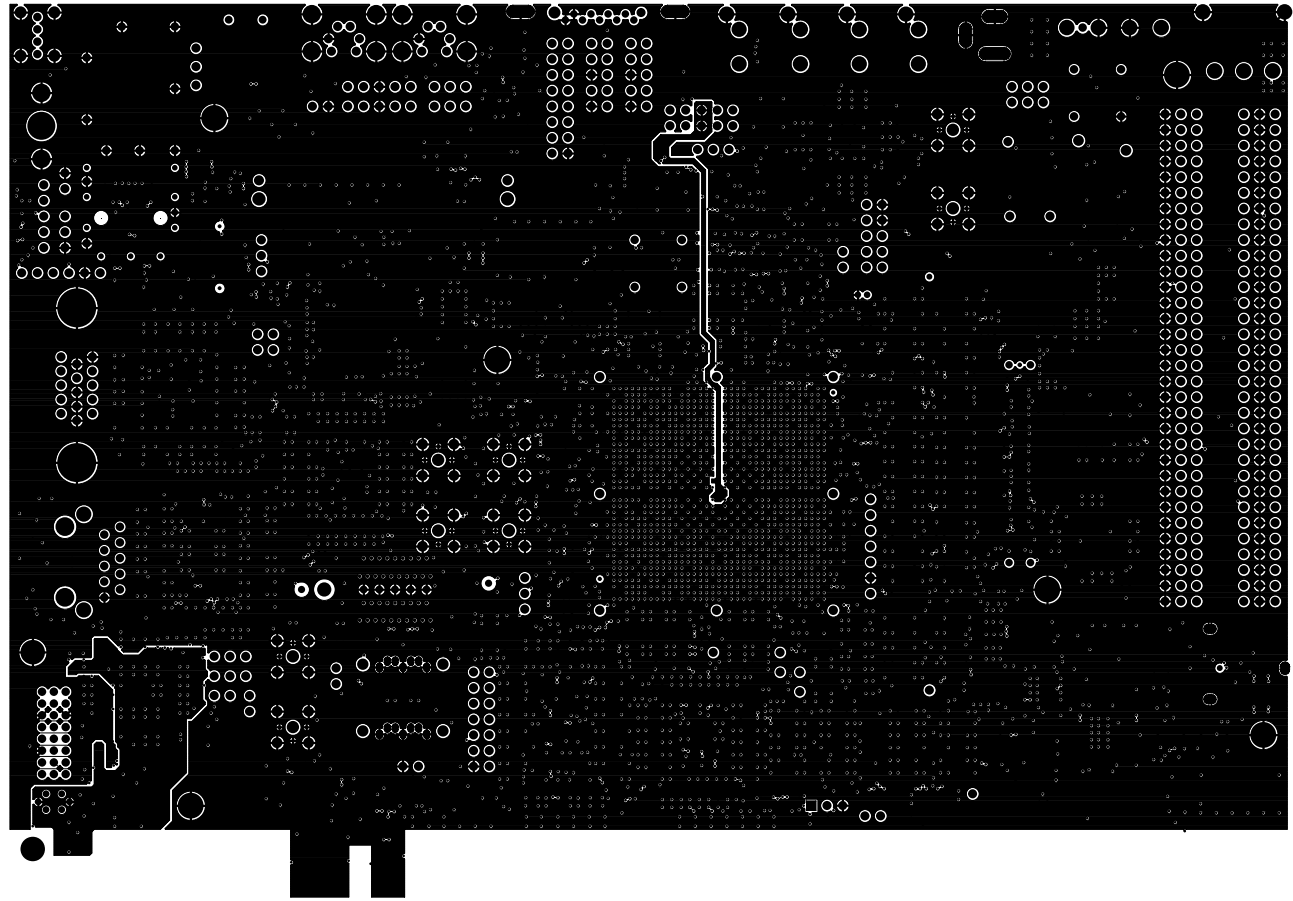
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 03 OF 25 L3_GND



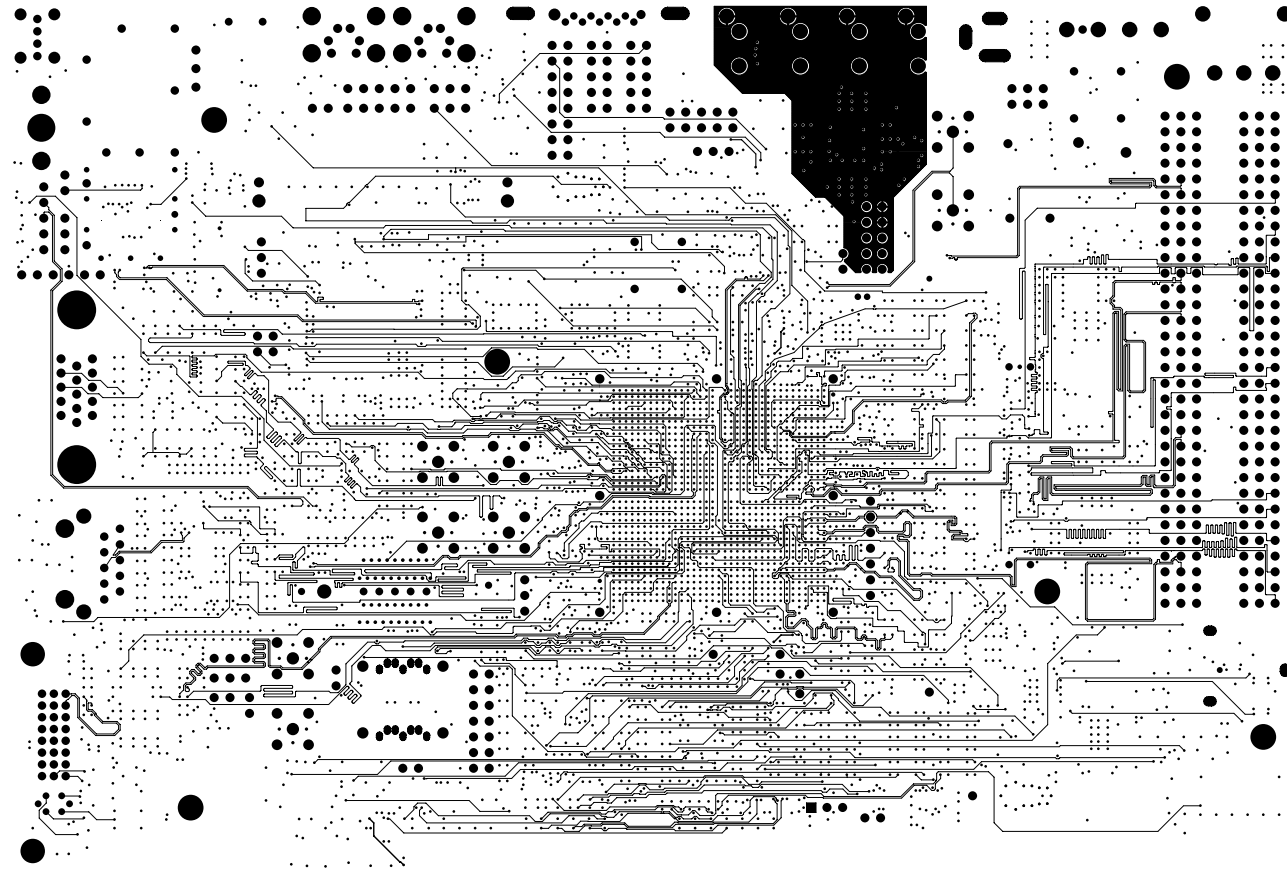
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 04 OF 25 L4_SIG



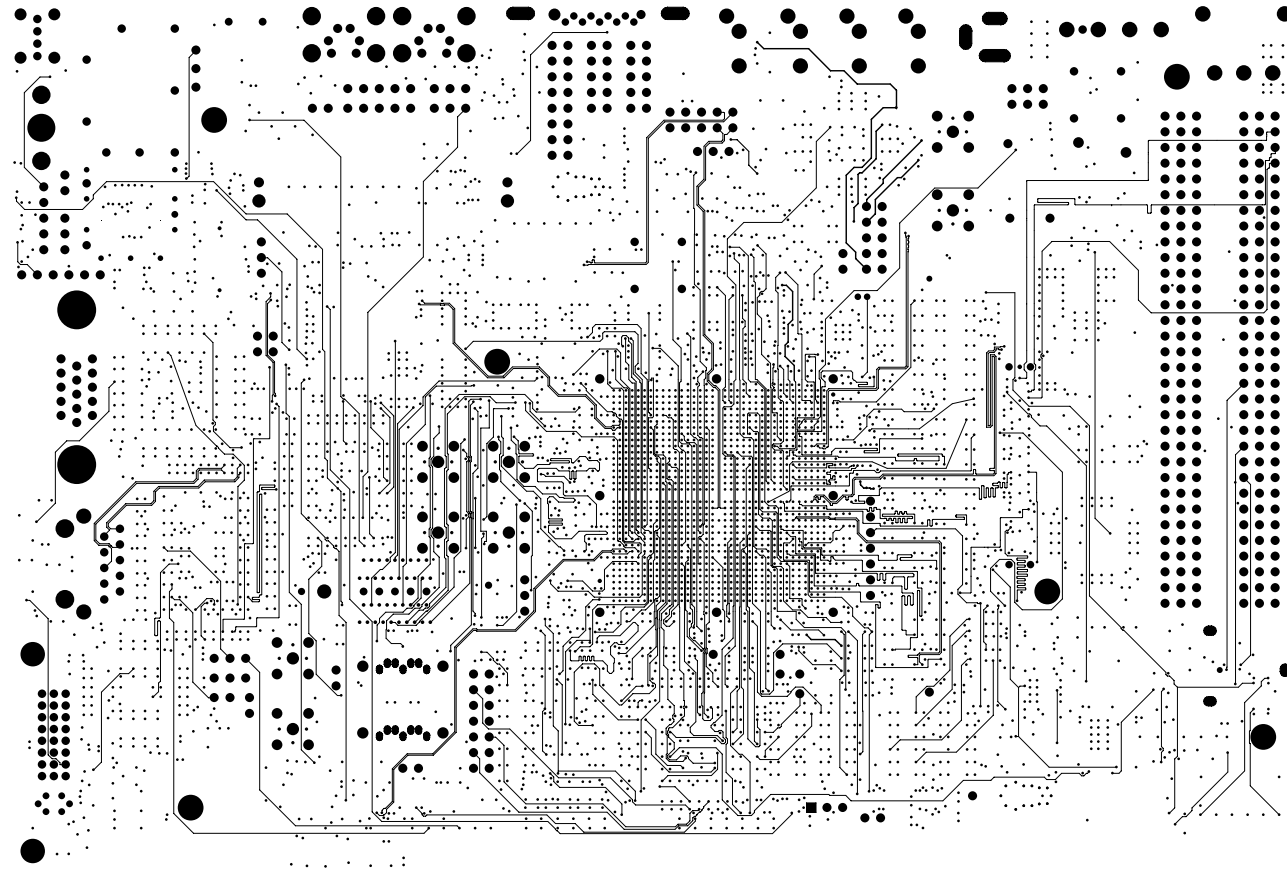
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 05 OF 25 L5_SIG

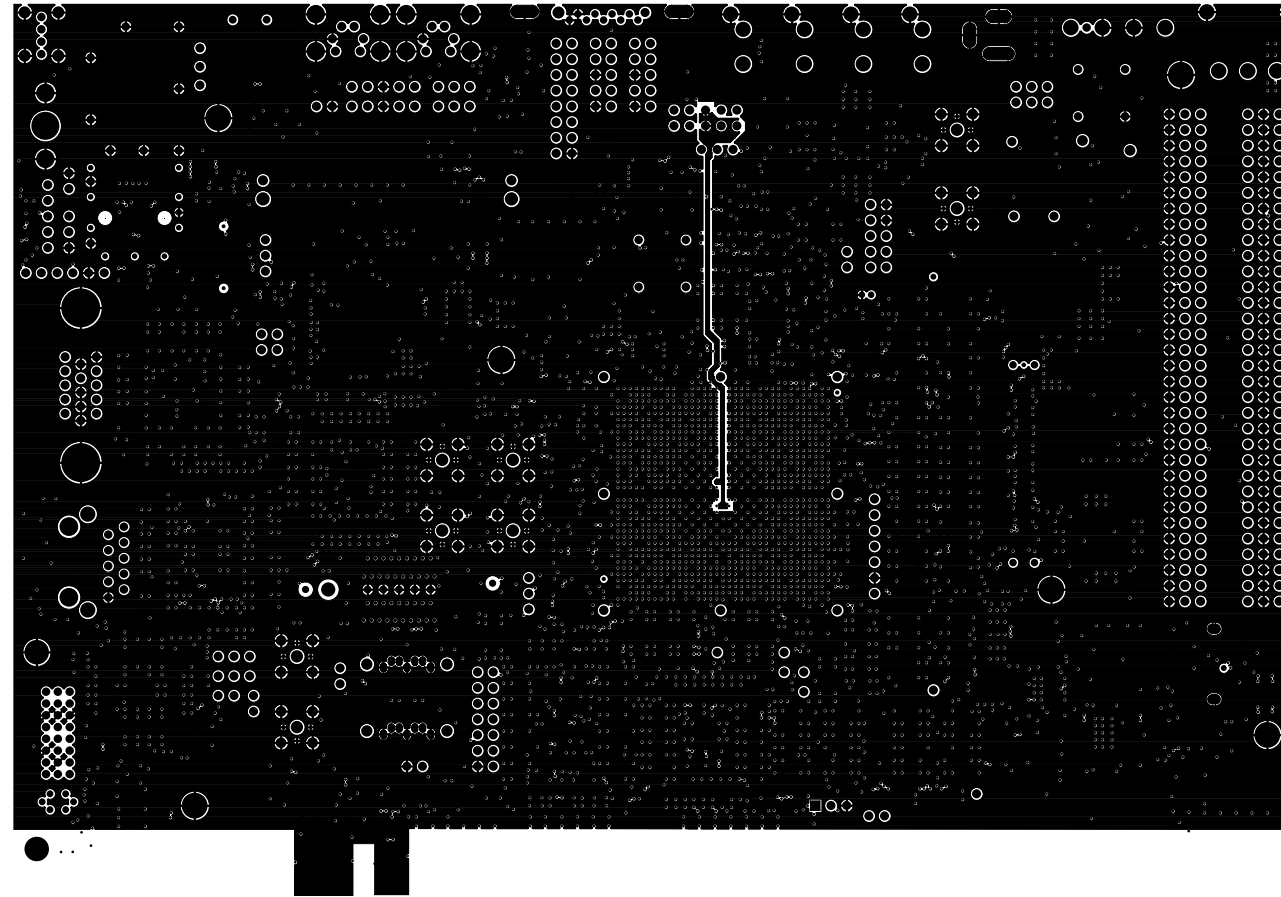


ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 06 OF 25 L6_GND

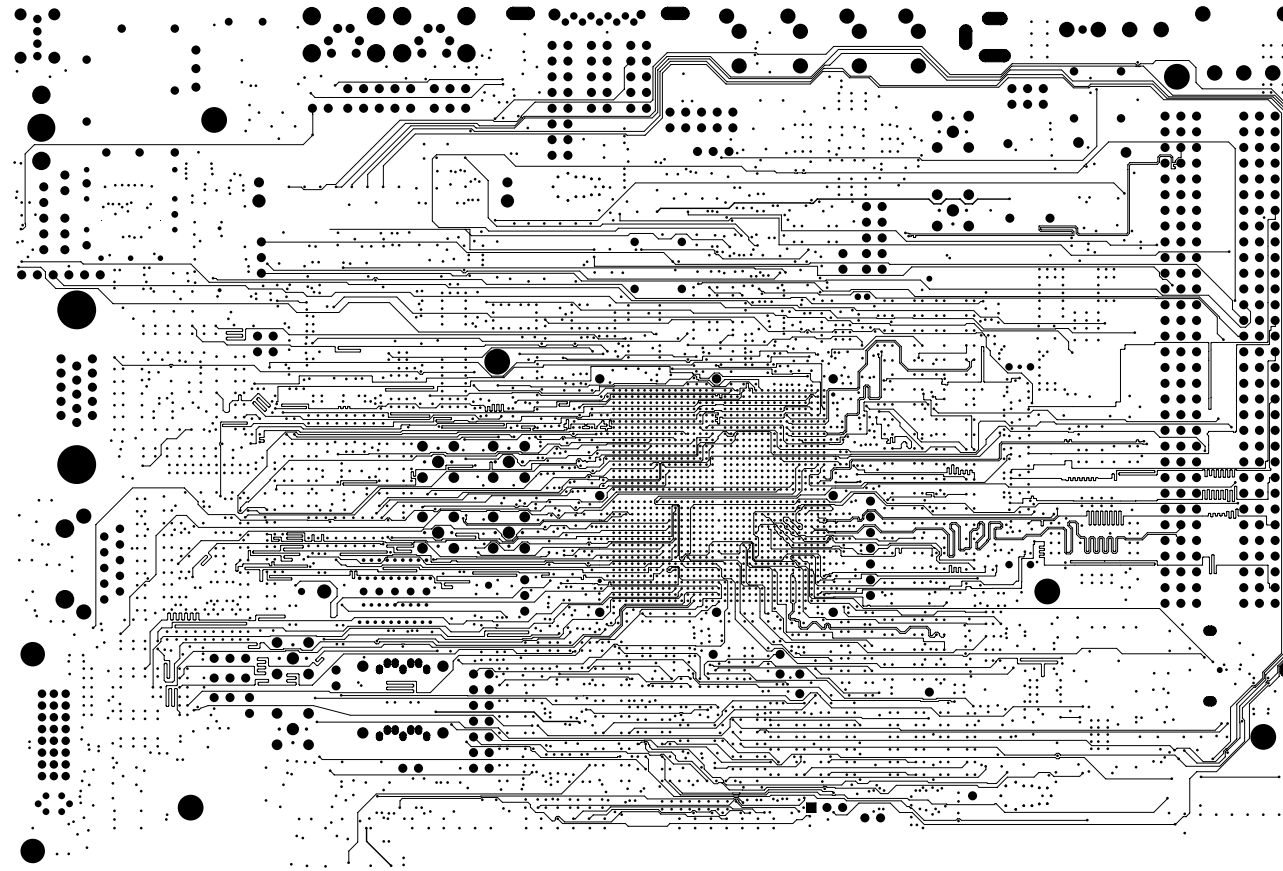


ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 07 OF 25 L7_SIG

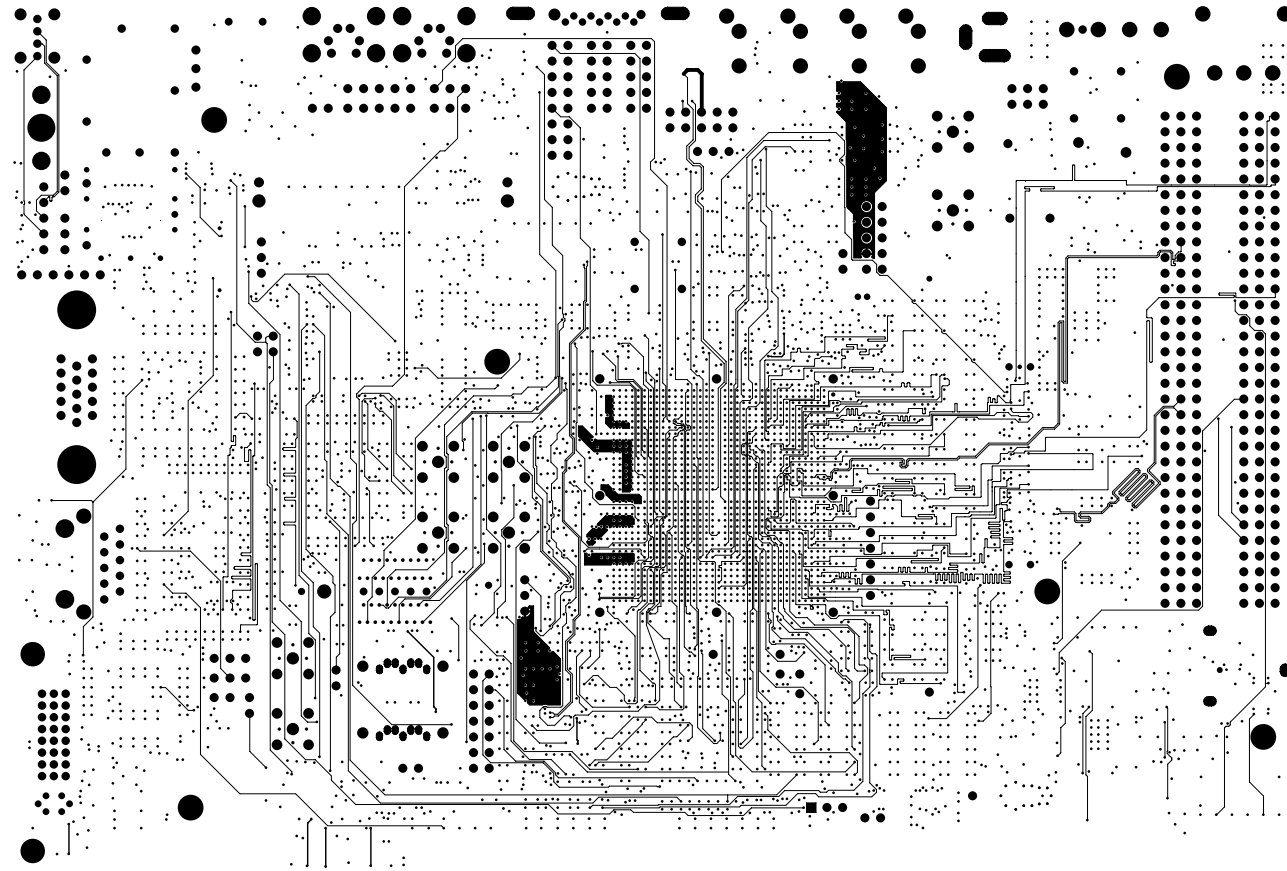




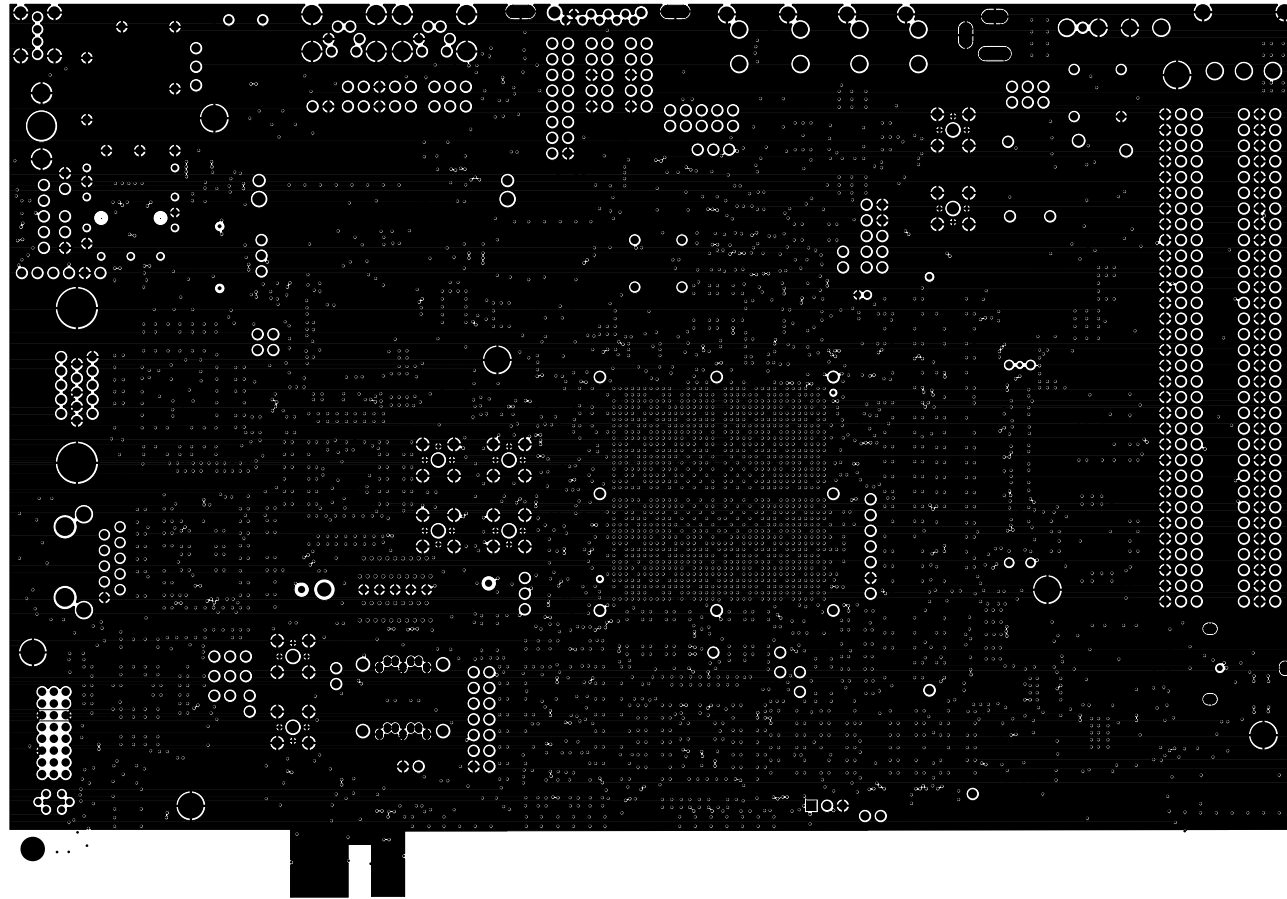
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 09 OF 25 L9_GND



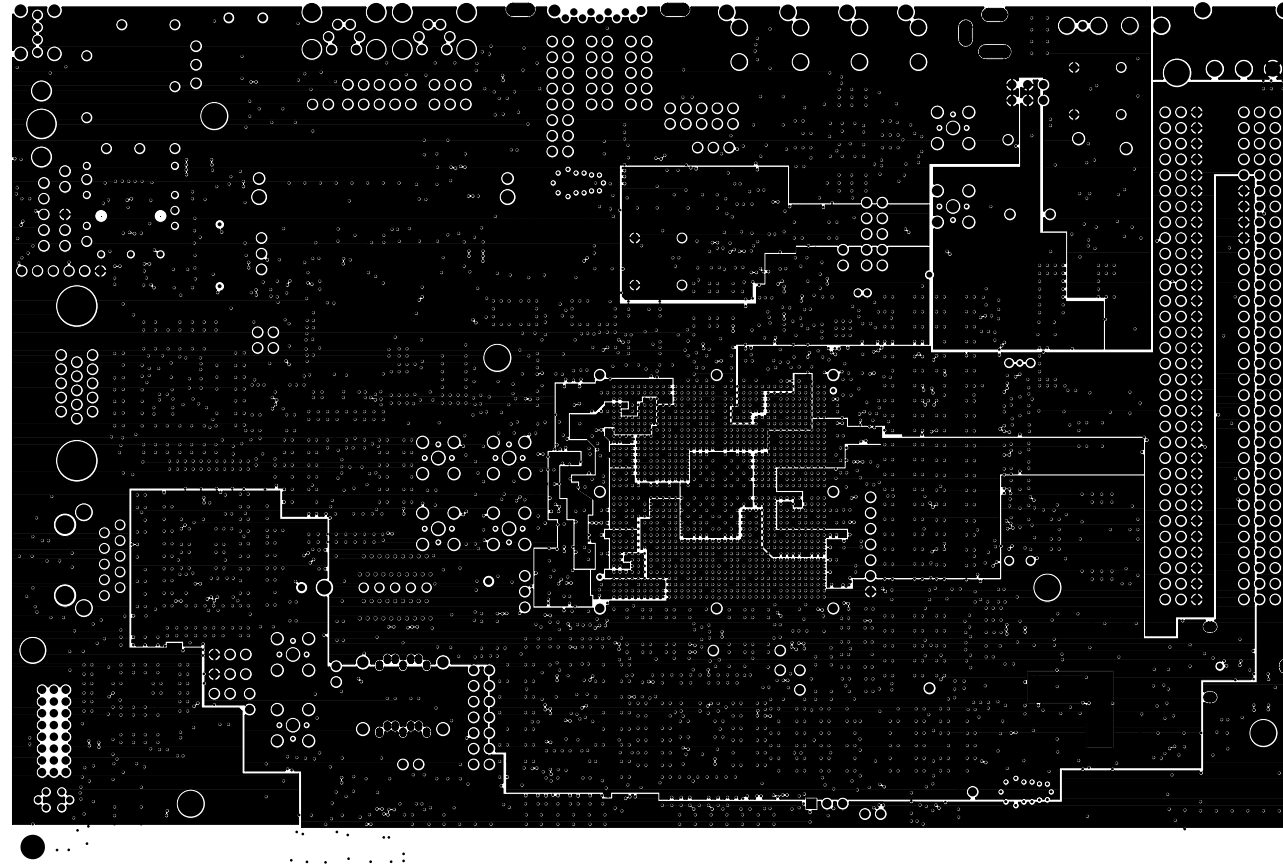
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 10 OF 25 L10_SIG



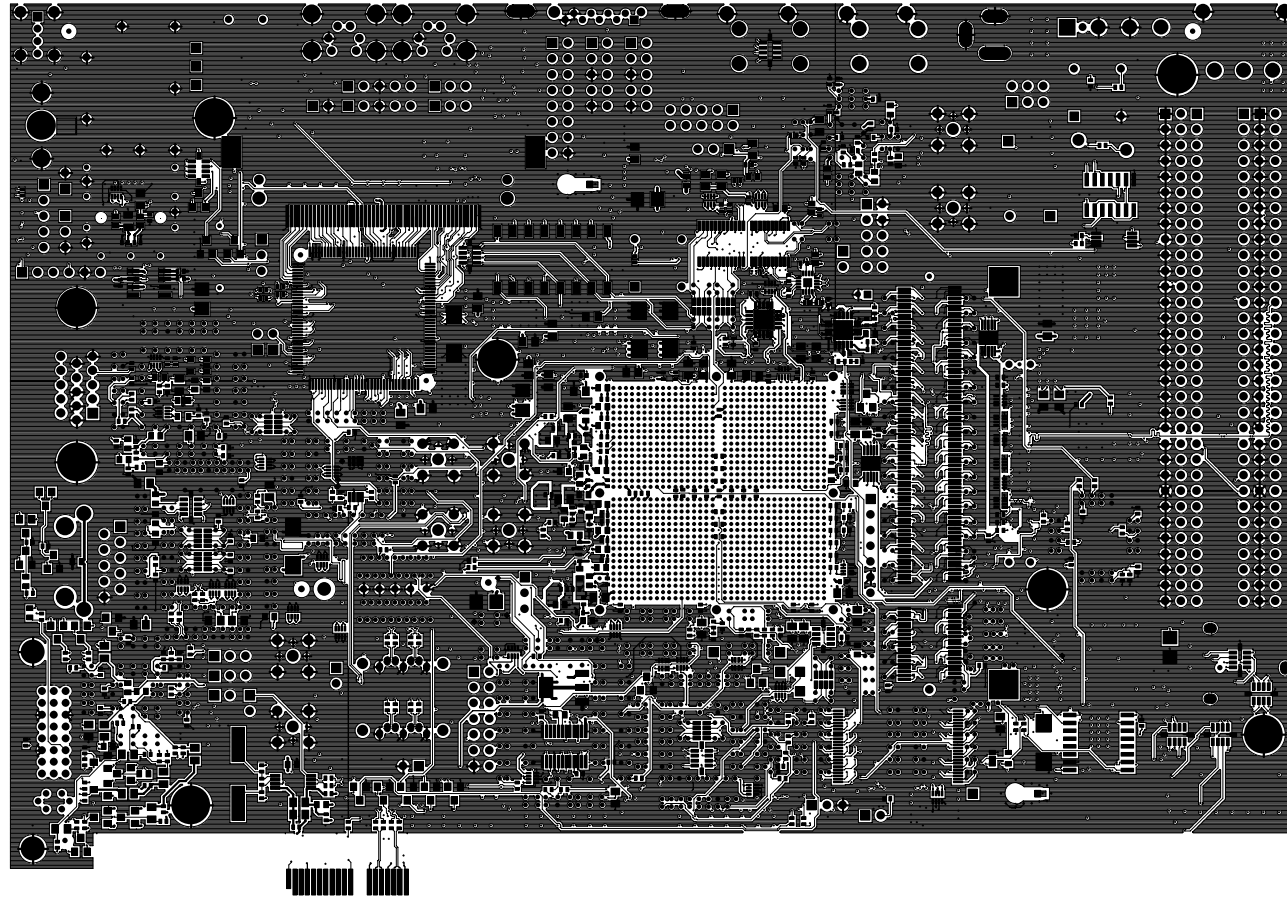
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 11 OF 25 L11_PWR



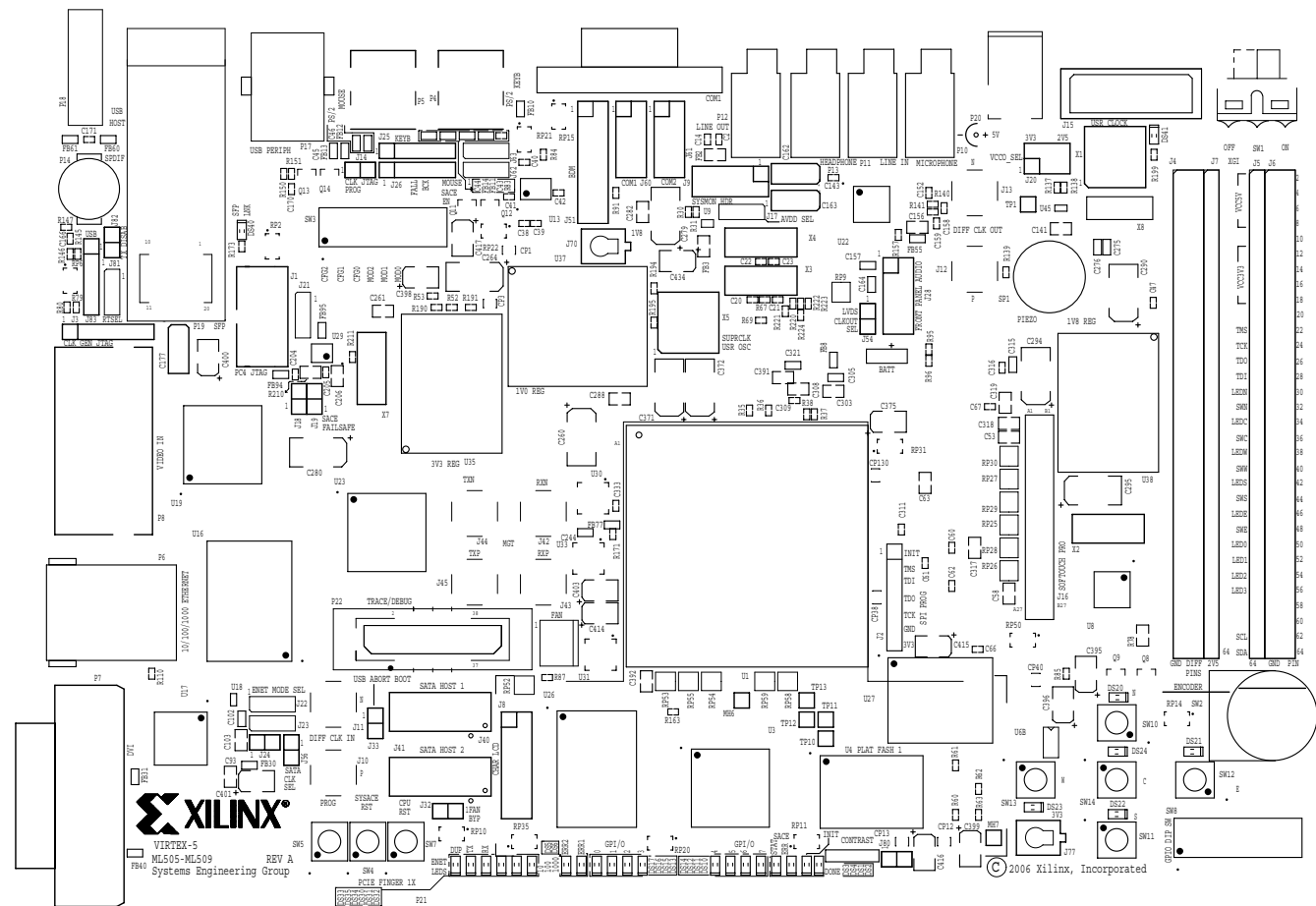
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 12 OF 25 L12_GND



ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 13 OF 25 L13_GND

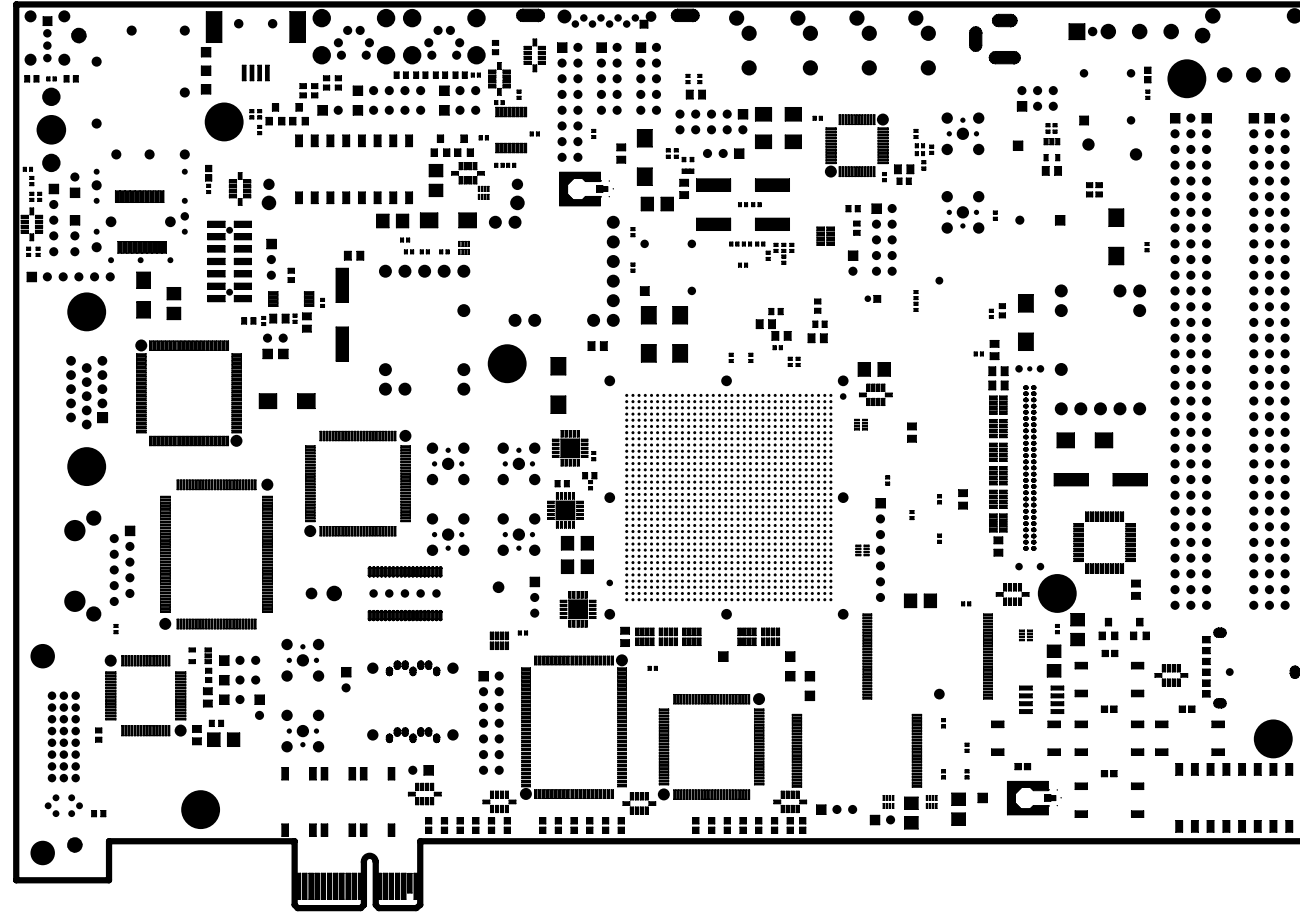


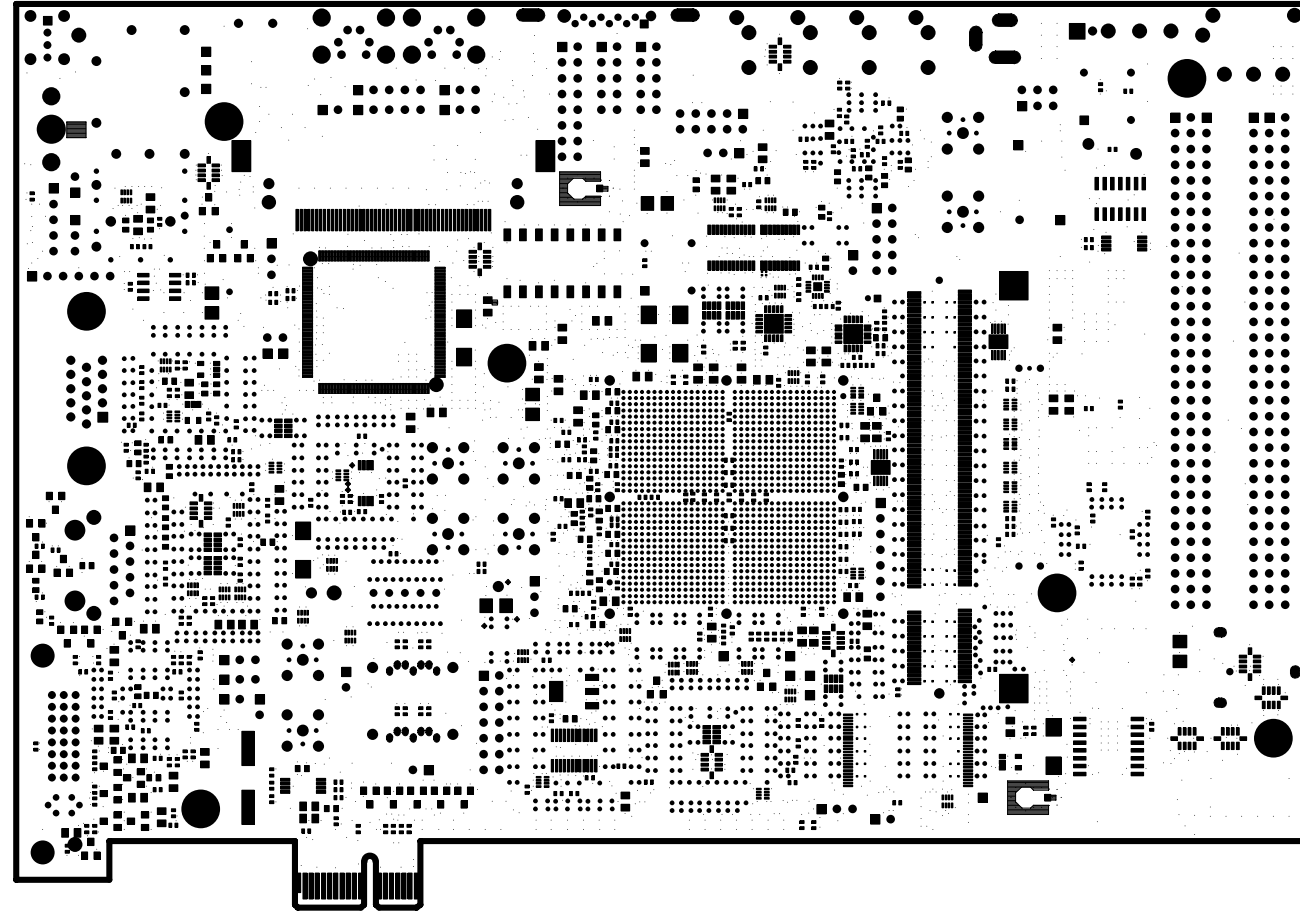
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 14 OF 25 L14_BOTTOM



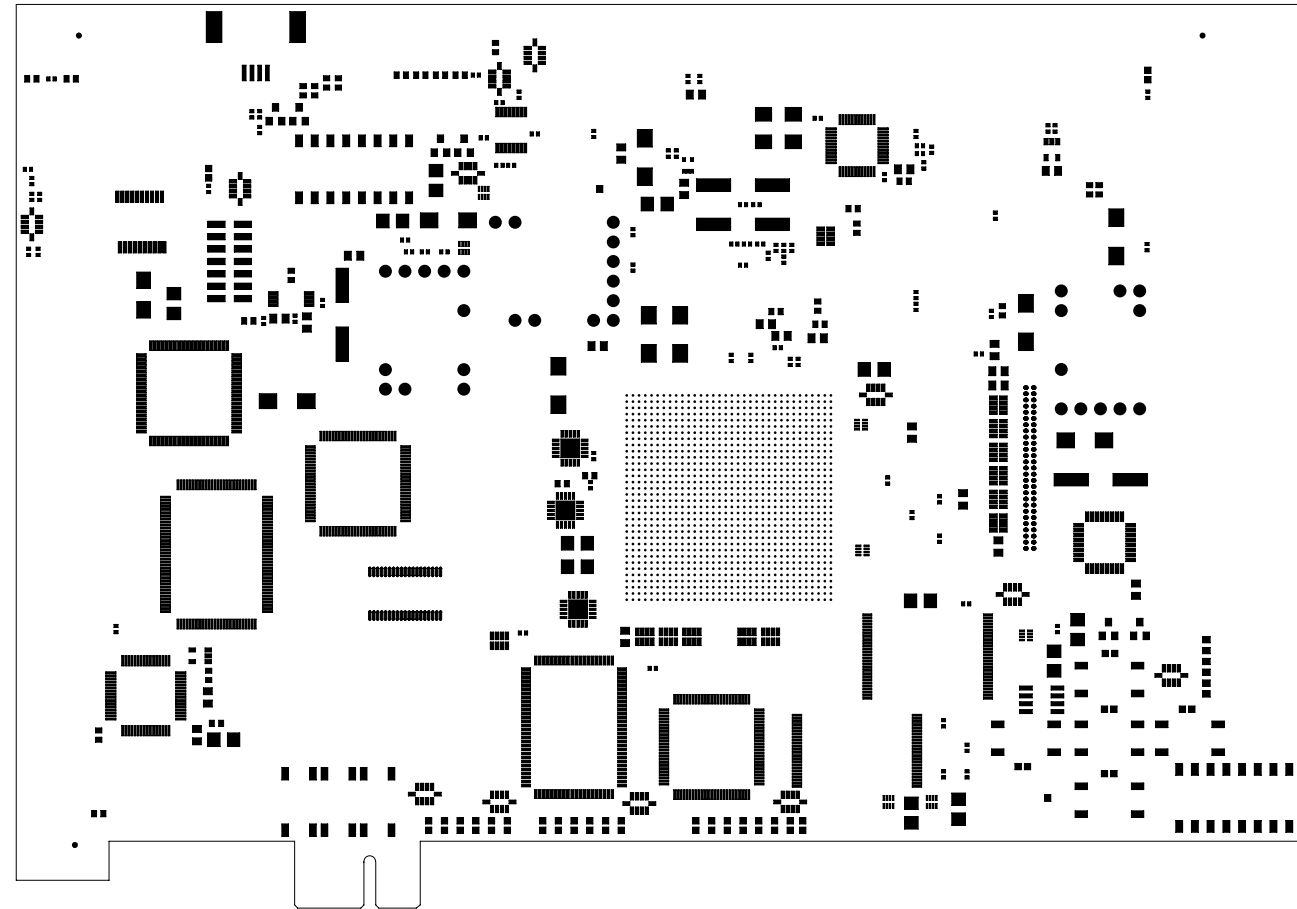


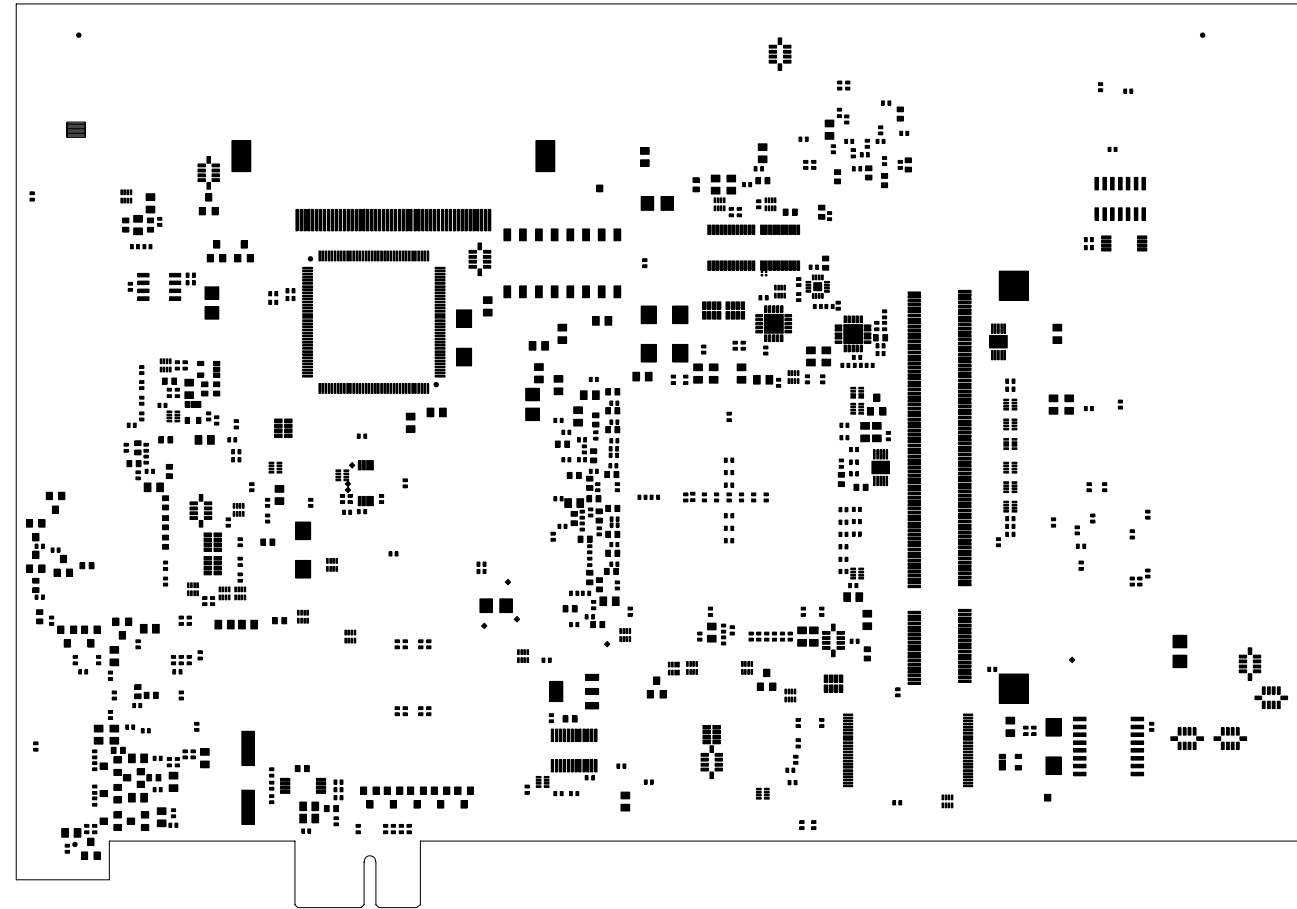
ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 20 OF 25 SILK_SCREEN_BOTTOM

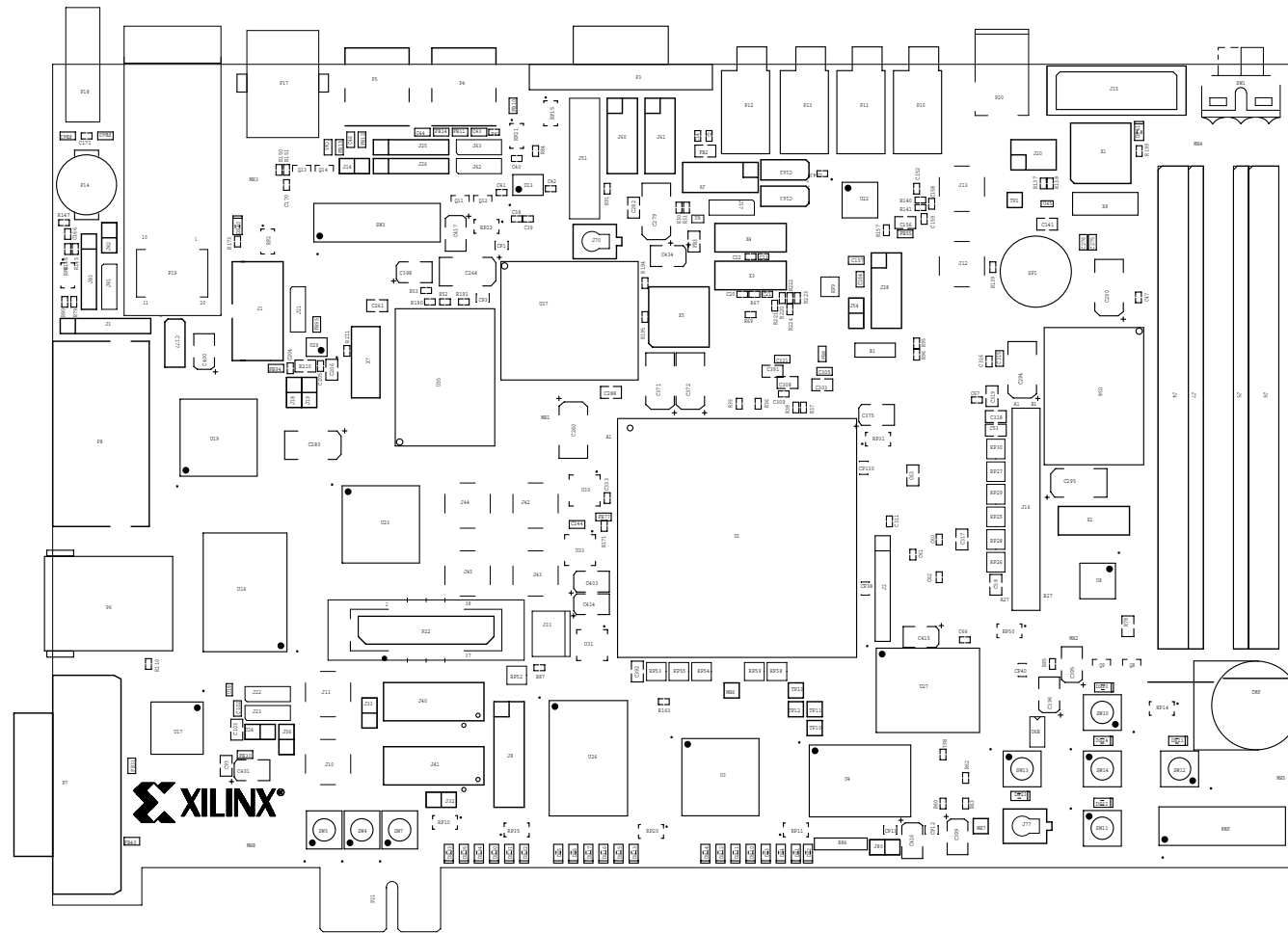


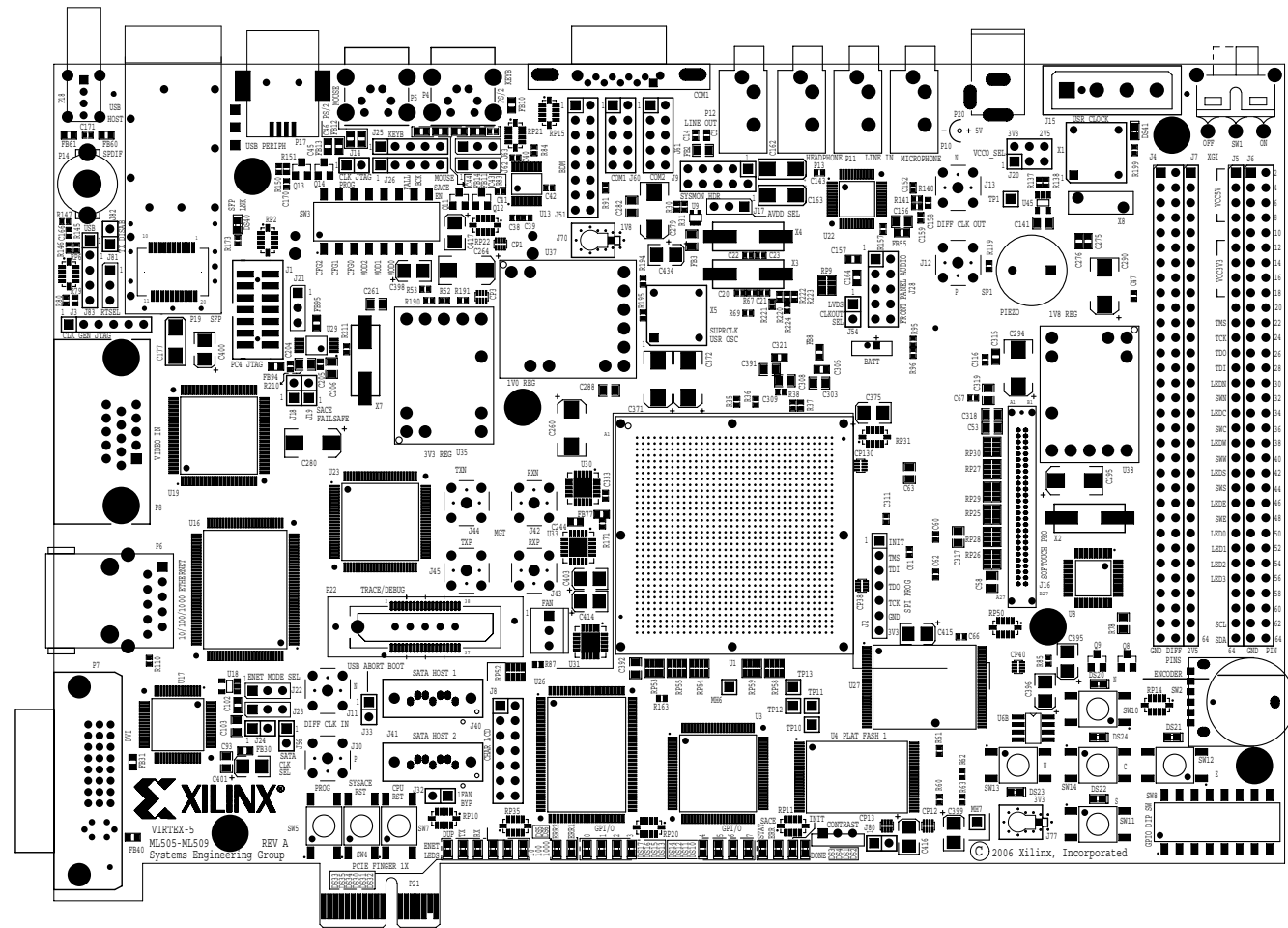


ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 16 OF 25 MASK BOTTOM









ARTWORK, ROHS COMPLIANT, ML505 VIRTEX-5 LX EVALUATION PLATFORM, 1280415
ARTMASTER # 0531630
Designed by Xilinx Oct 04 2006
LAYER: 22 OF 25 ASSY TOP
19 OF 25 SILK-SCREEN TOP

