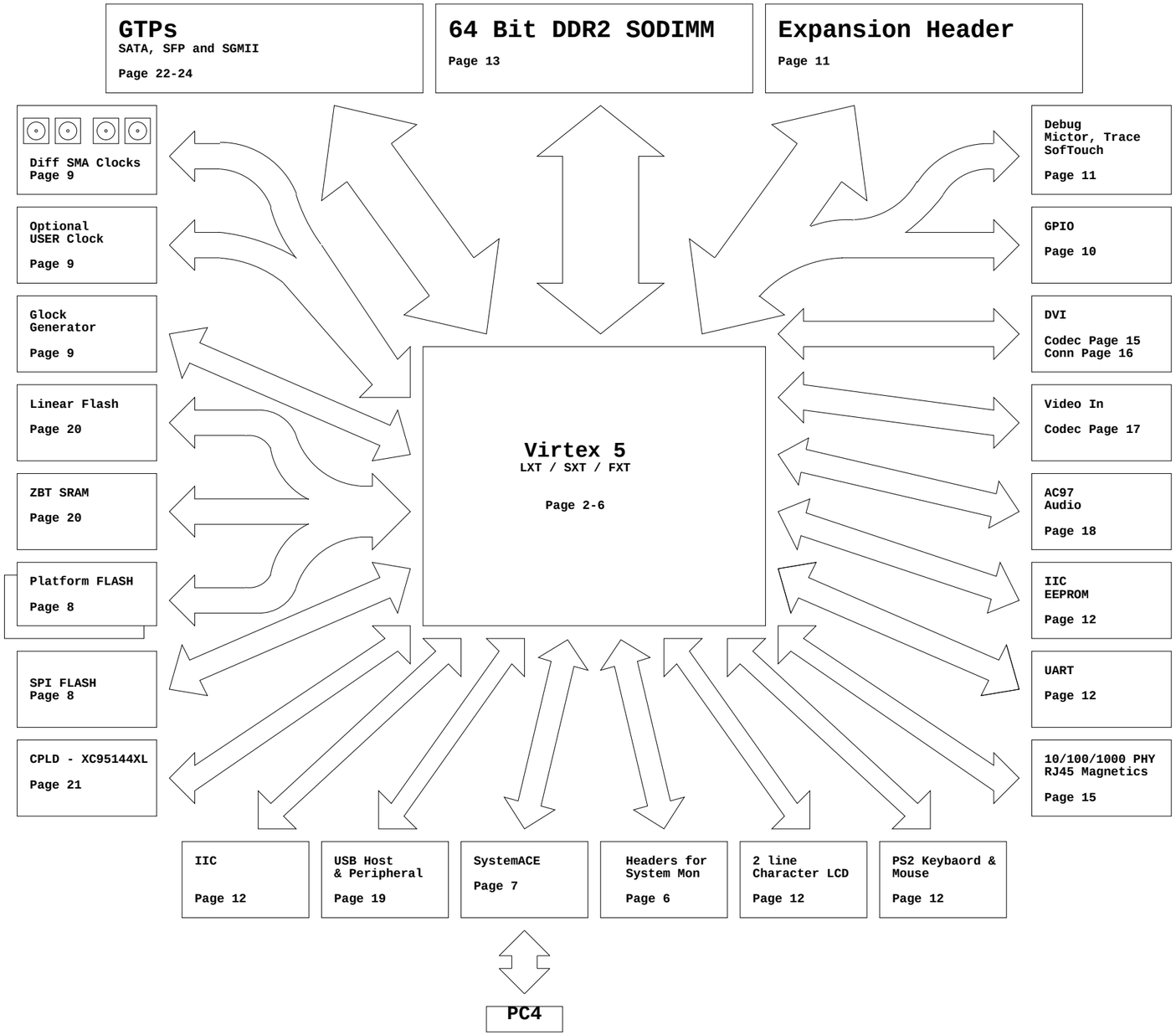
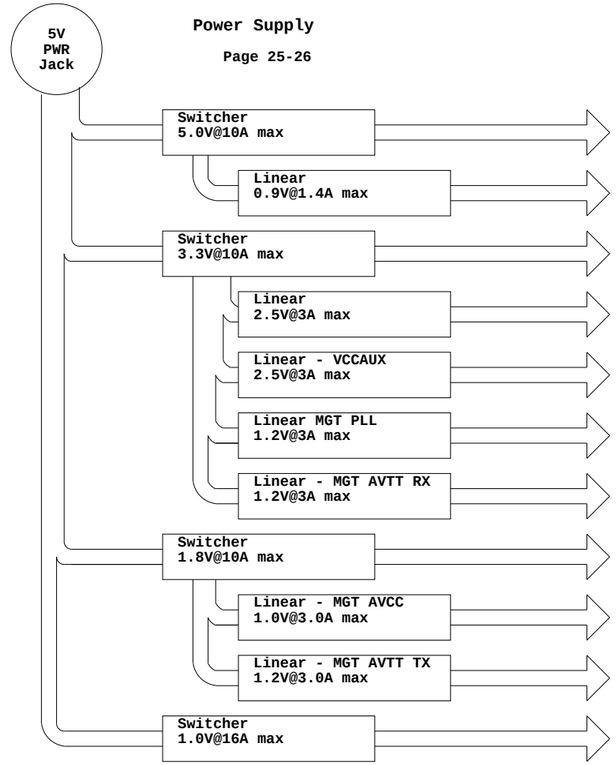
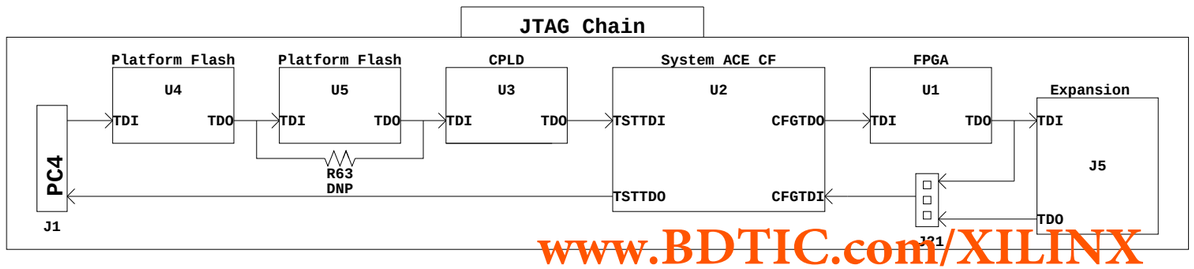
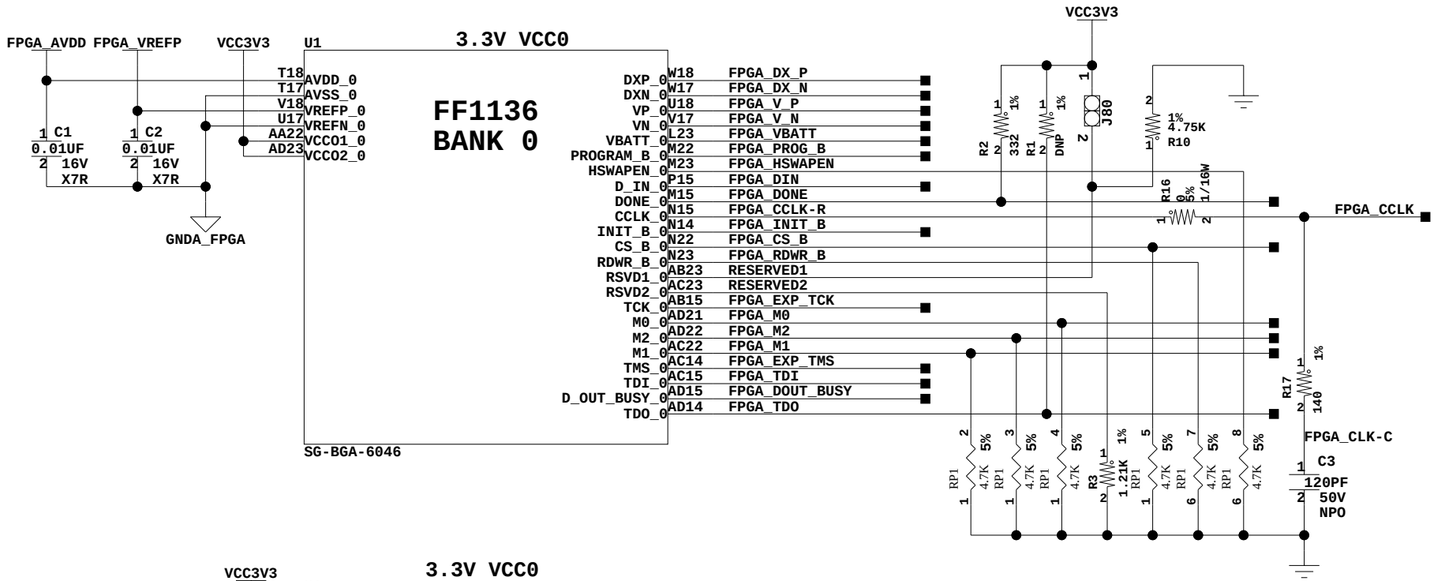


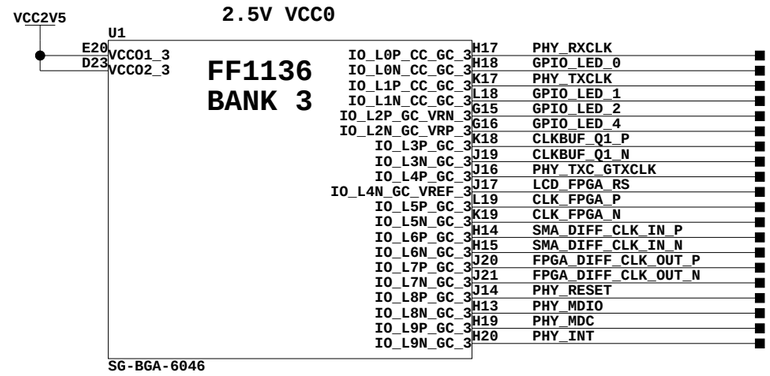


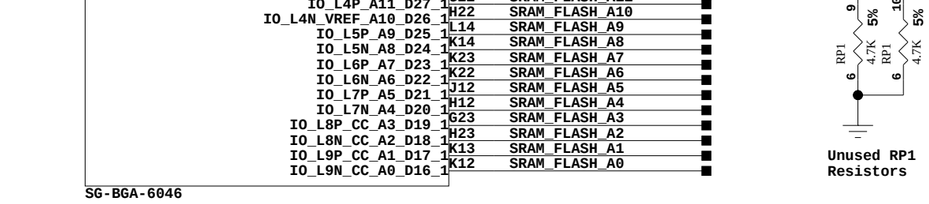


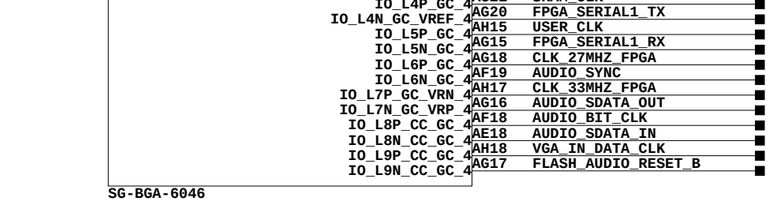
XILINX

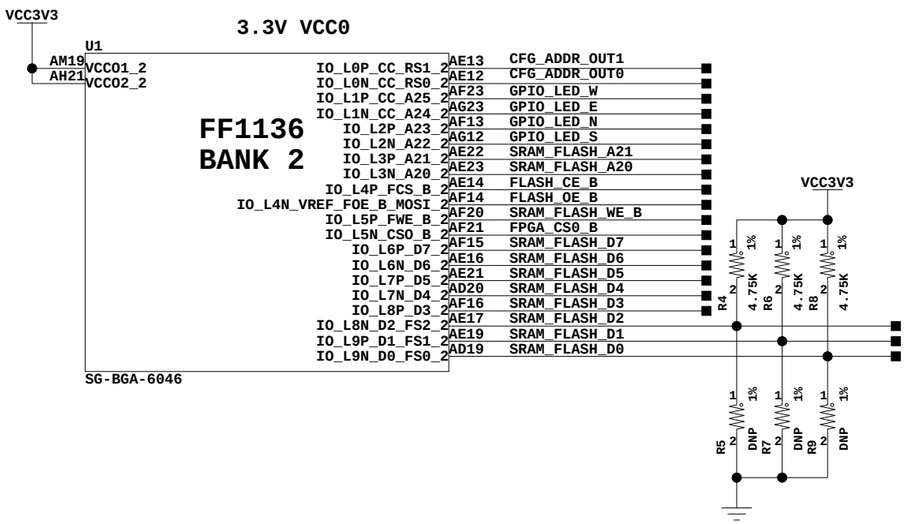
Title:	ML505/6/7 Block Diagram SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	1 of 27	Drawn By	BP





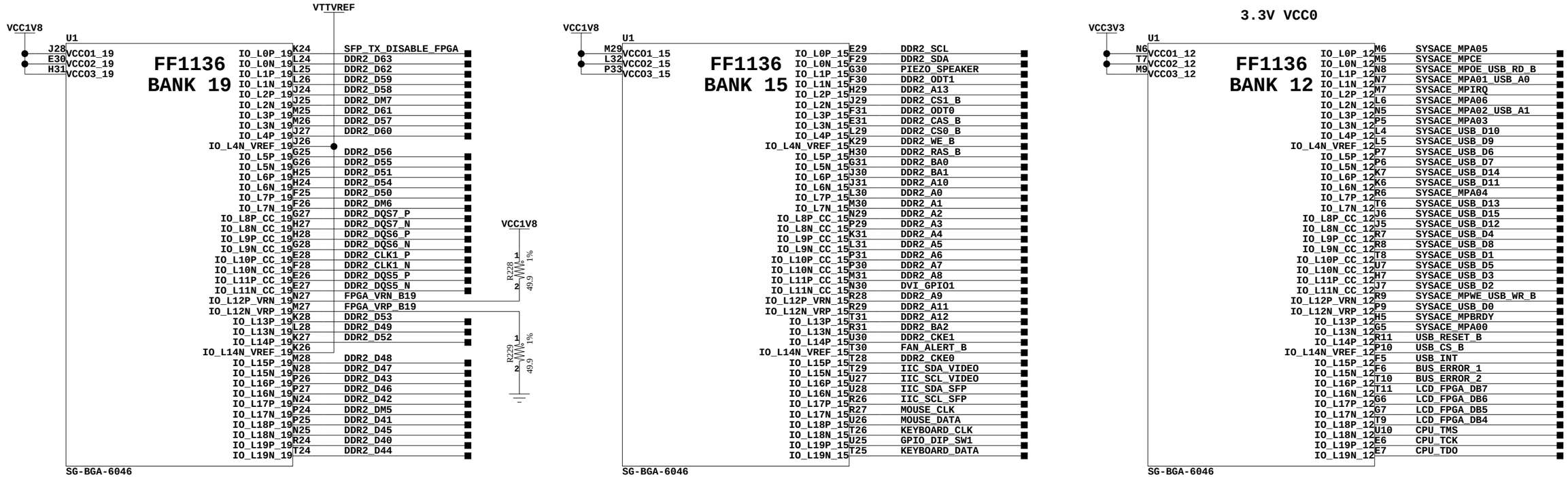






Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs

Title:	FPGA Banks 0,1,2,3,4 Config, FLASH, SRAM, GPIO, CLKs SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	2 of 27	Drawn By	BP



Banks 14,16,18,21
DDR2, PS2, GPIO

XILINX

Title:	FPGA Bank 14, 16, 18, 21DDR2, PS2, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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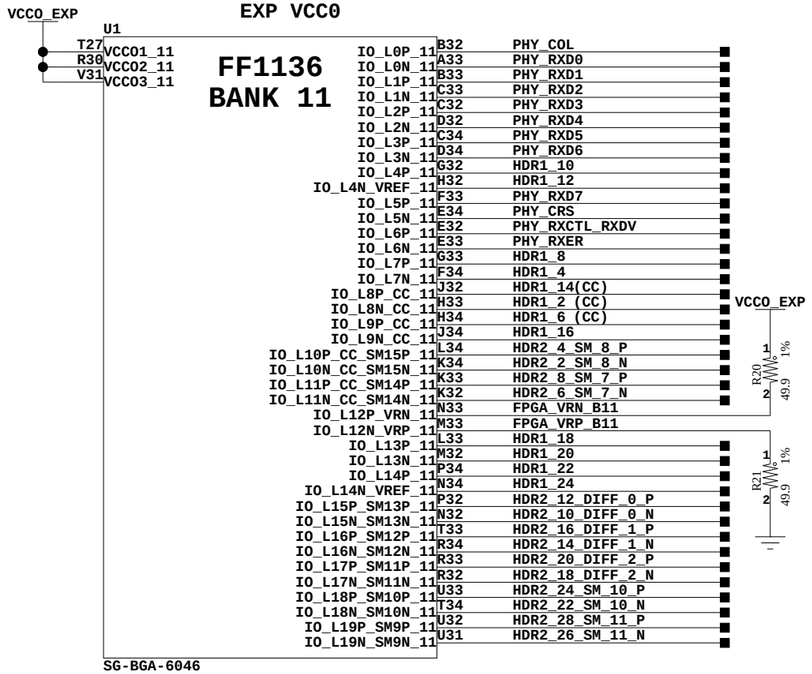

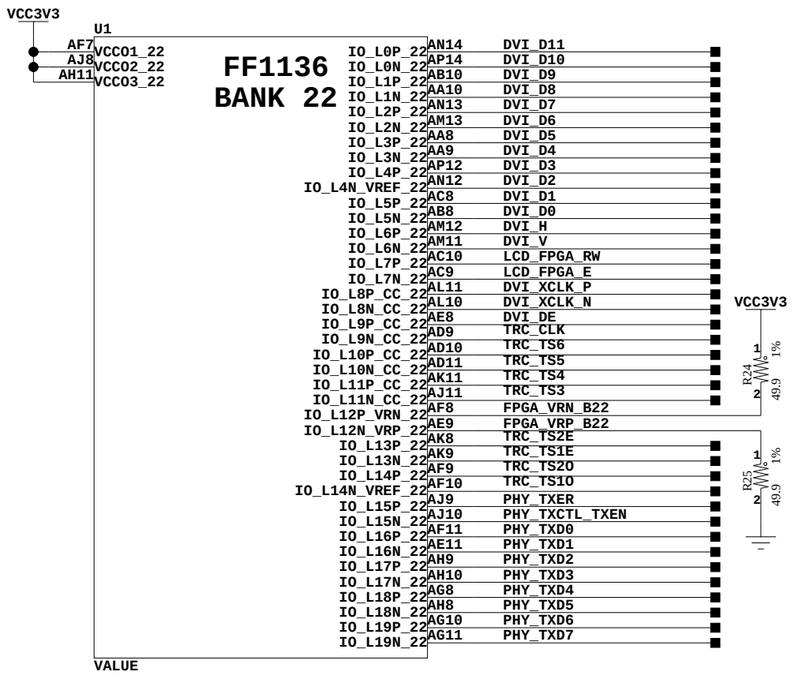

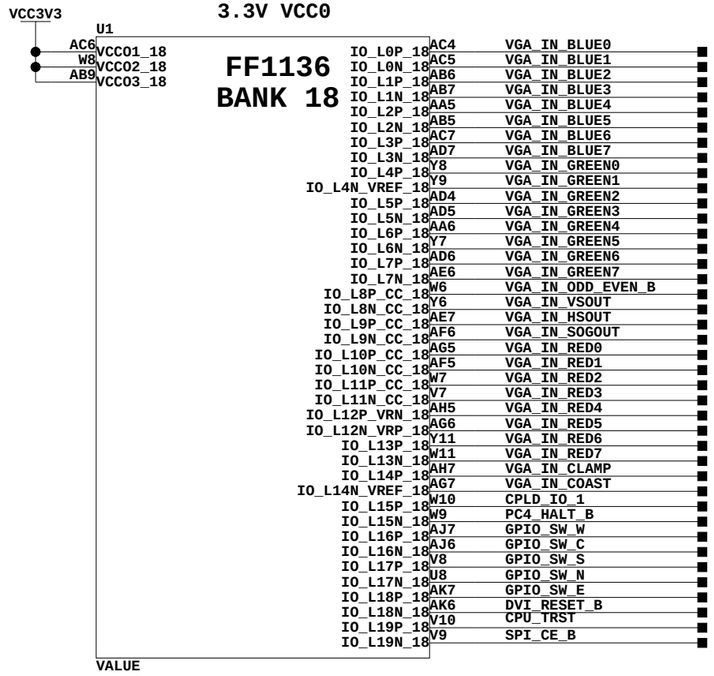

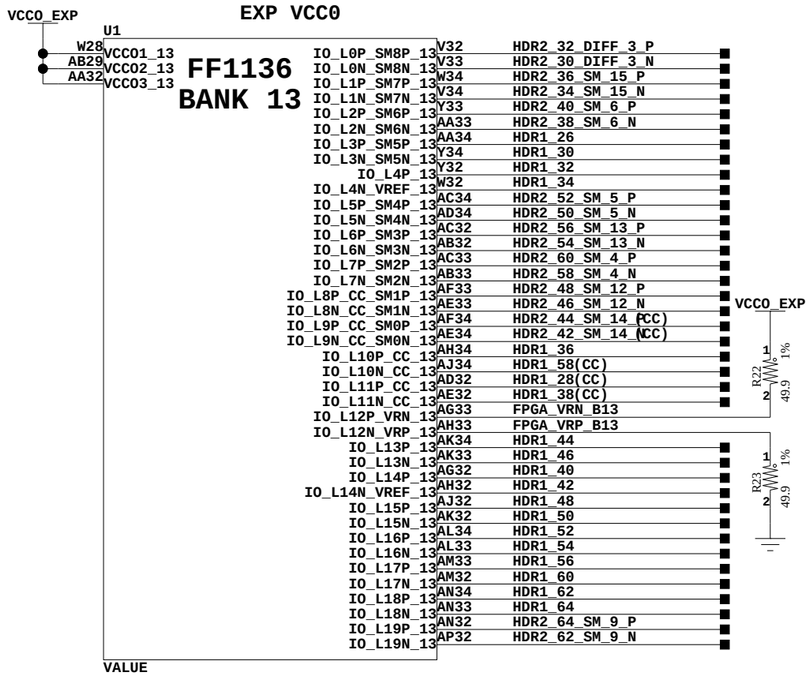

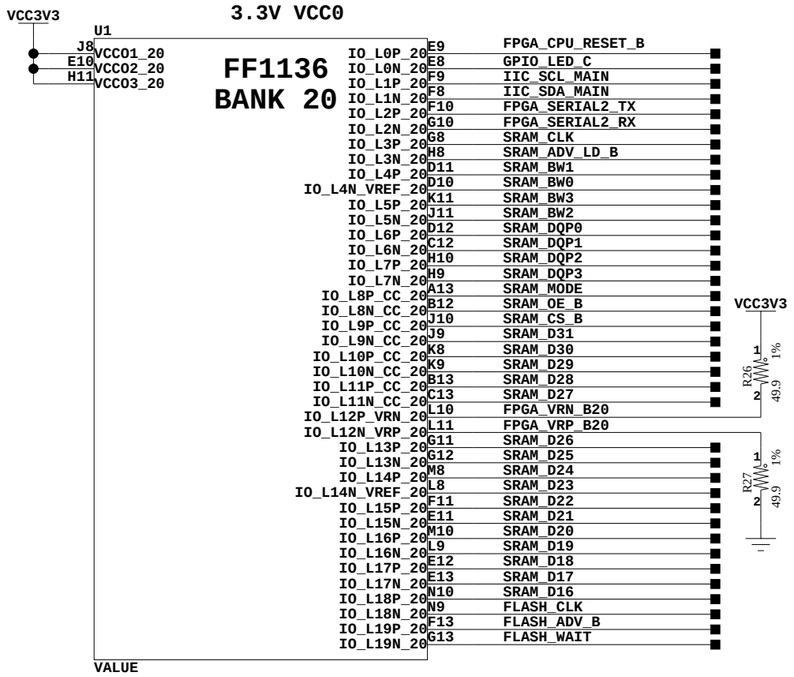

Banks 11,12,13
Sys ACE, XGI, PHY, LCD

XILINX

Title:	Banks 11,12,13 Sys ACE, XGI, PHY, LCD SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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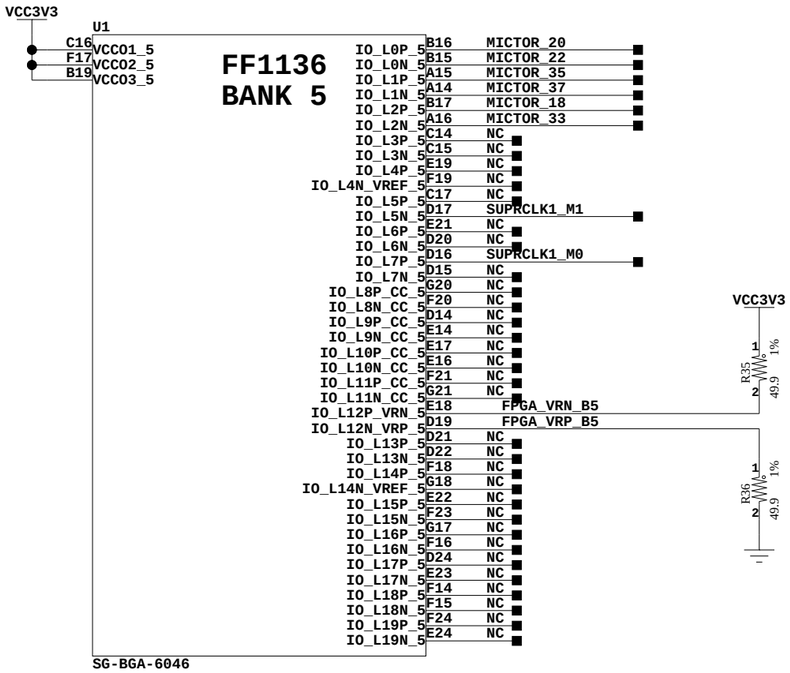
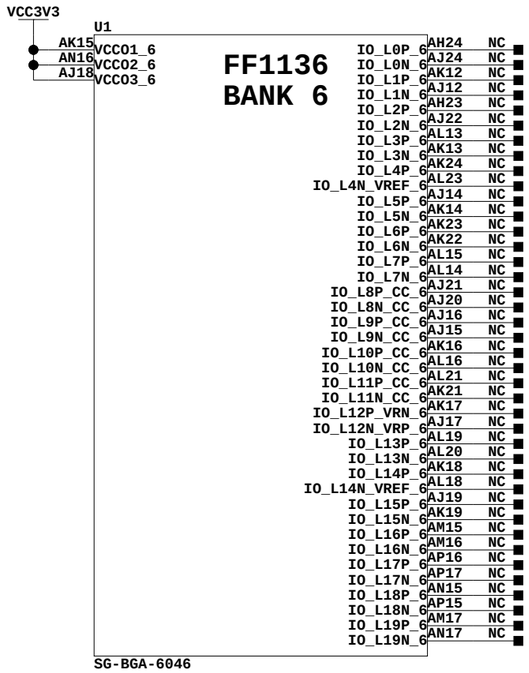
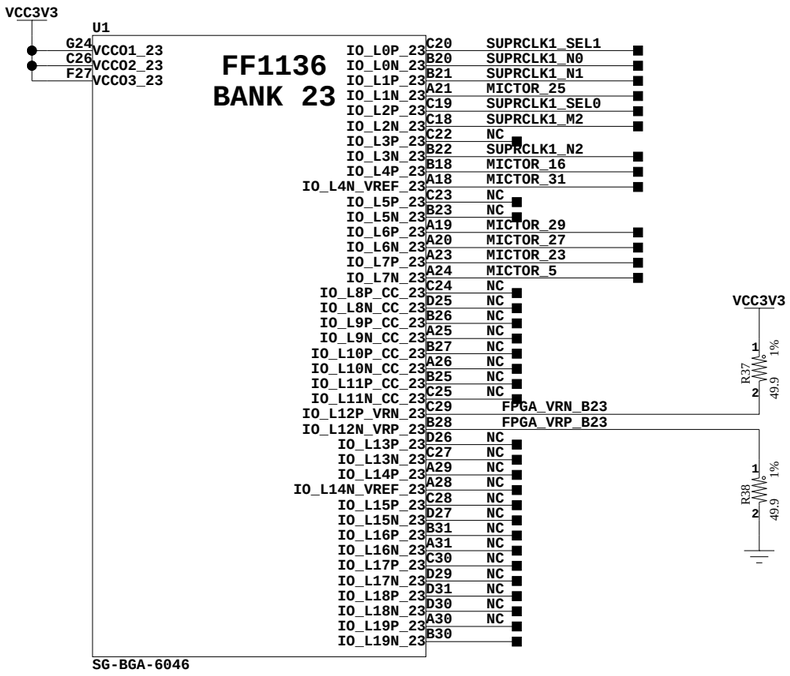
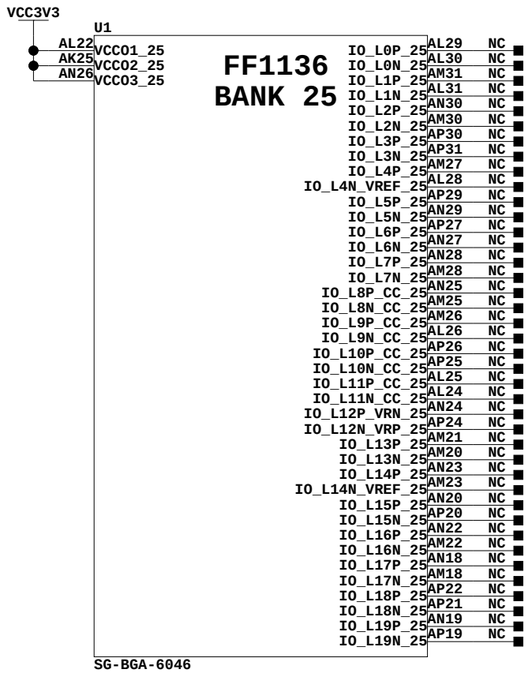
Unused banks on the LX50T and SX50T









Banks 15, 17
VGA, IIC, PHY
SRAM, FLASH, GPIO

Title:	Banks 11,12,13,VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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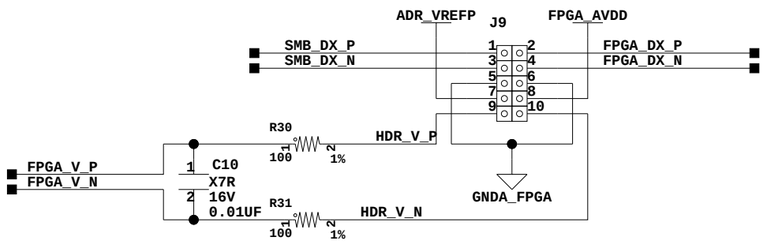
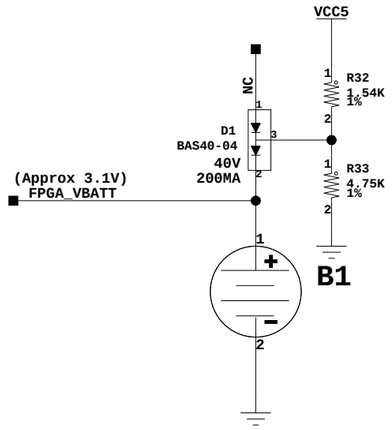
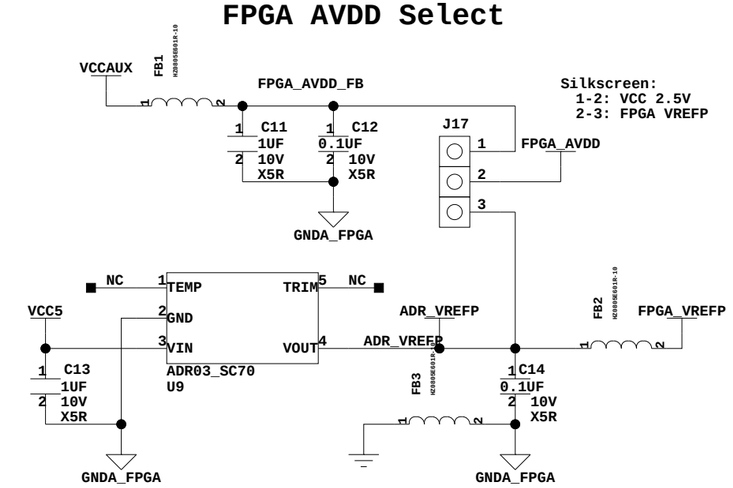
System Monitor Header

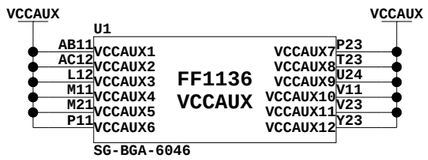


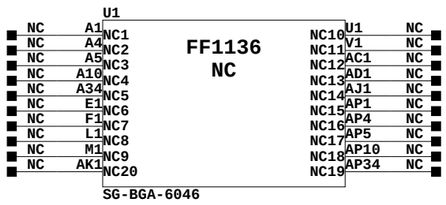
Rechargeable Battery

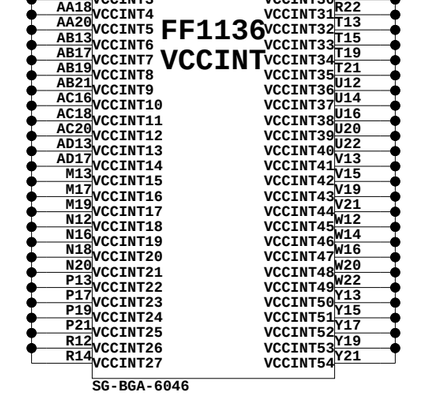


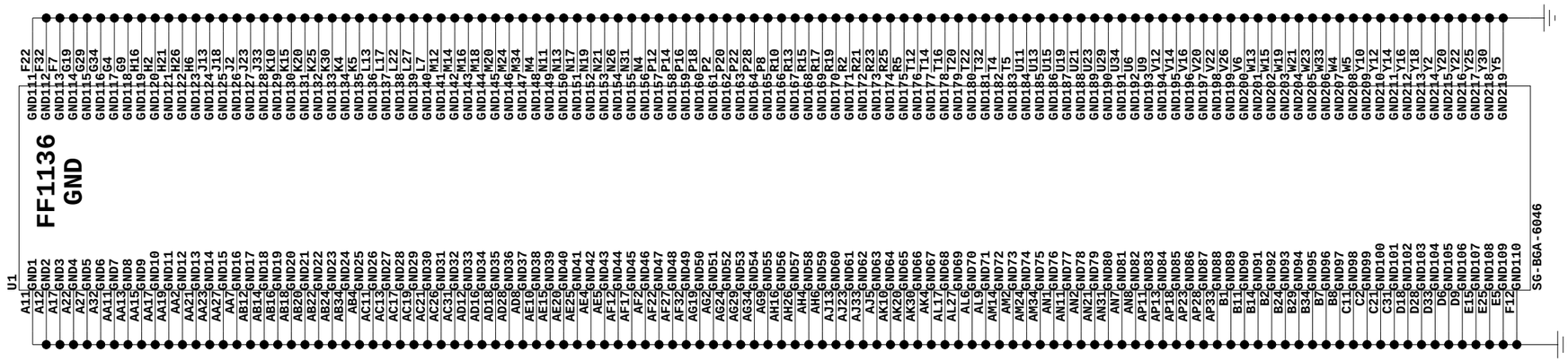
FPGA AVDD Select











Power and Misc FPGA Banks VCCINT, VCCAUX, NCs, GND Battery and System Moniter

Title:	FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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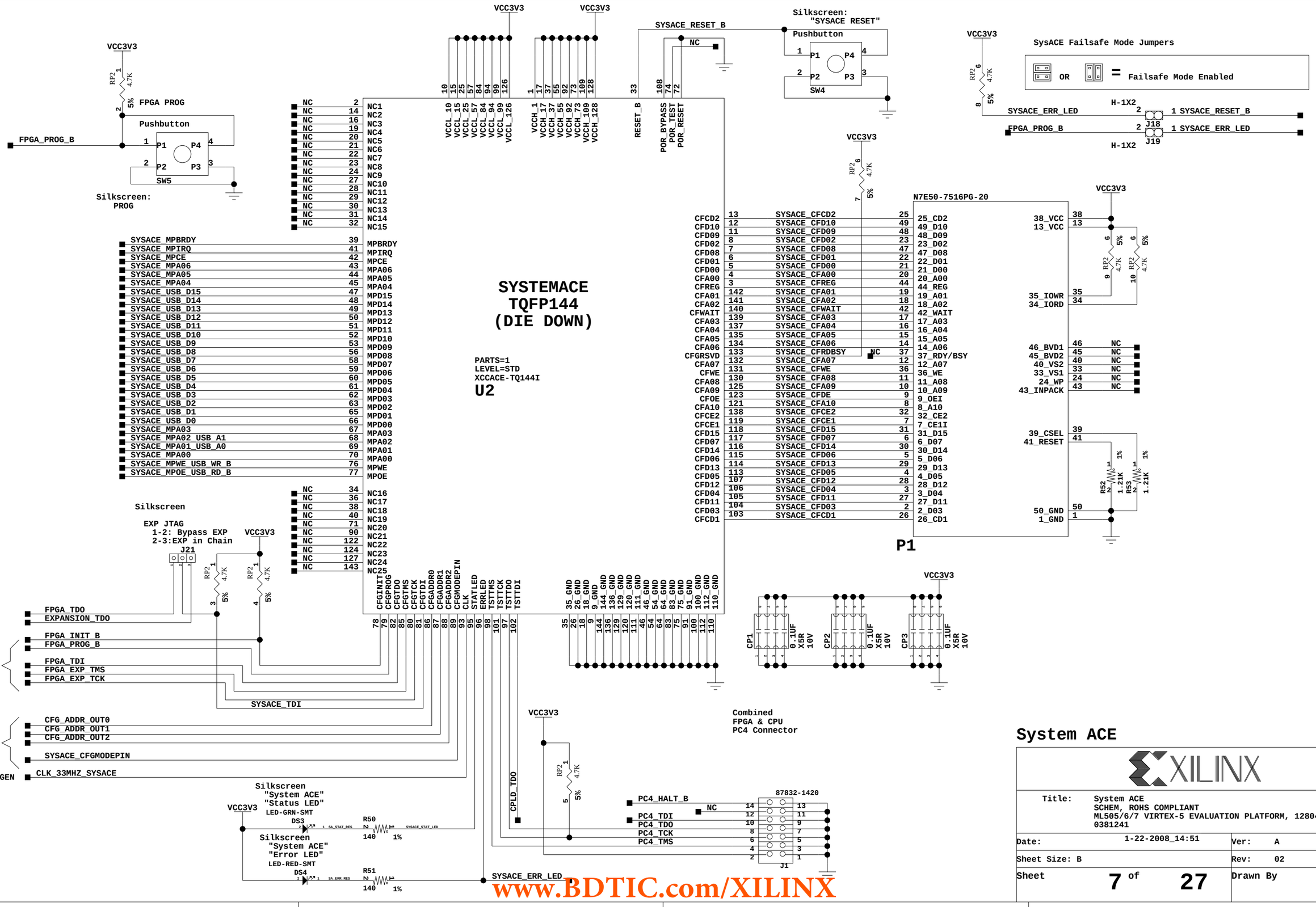

System ACE

Title:	System ACE SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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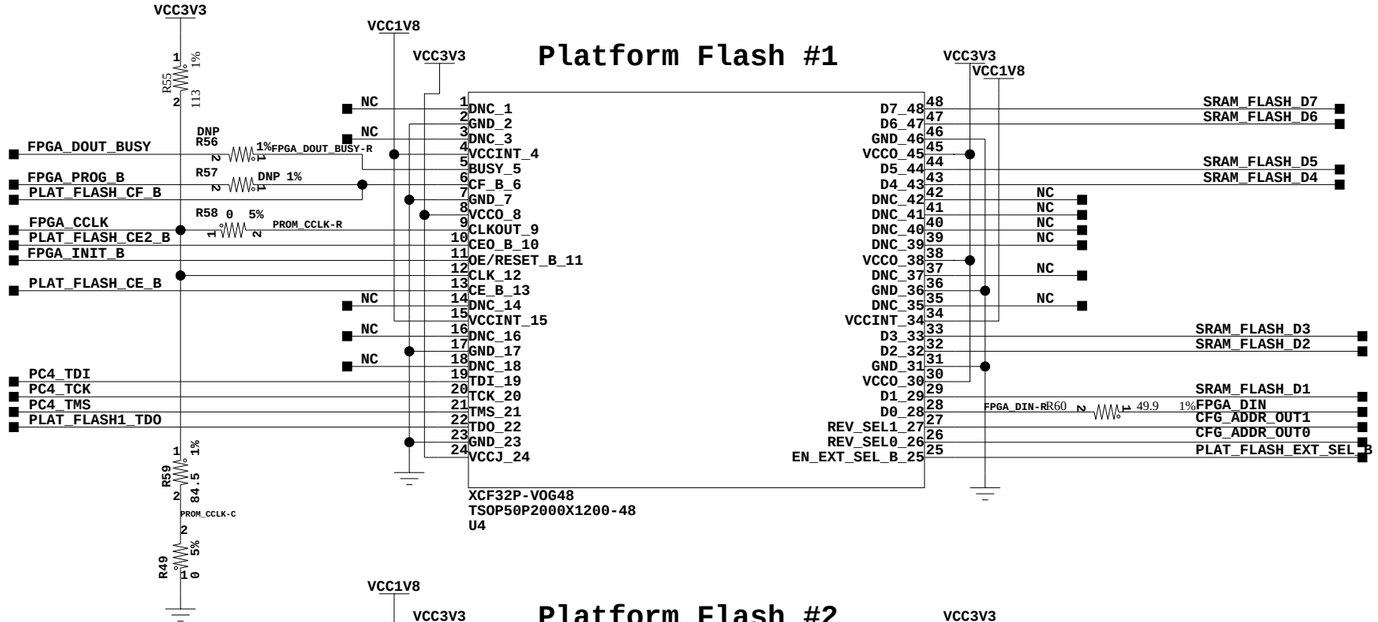
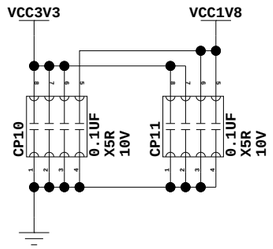
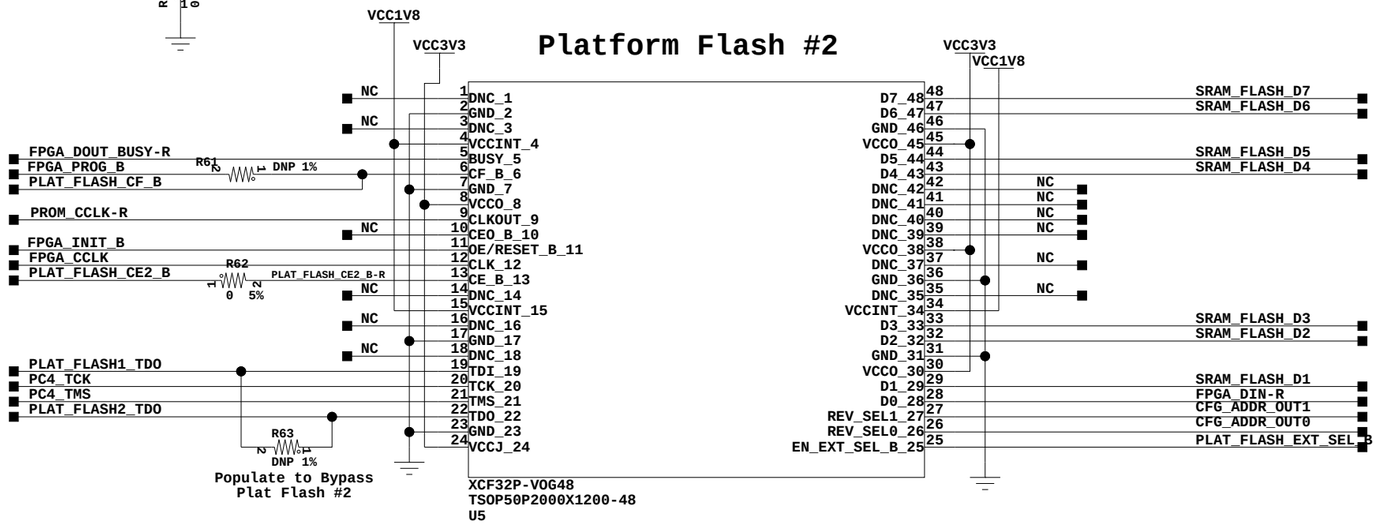
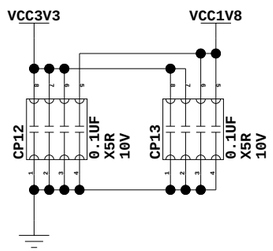
Platform Flash #1



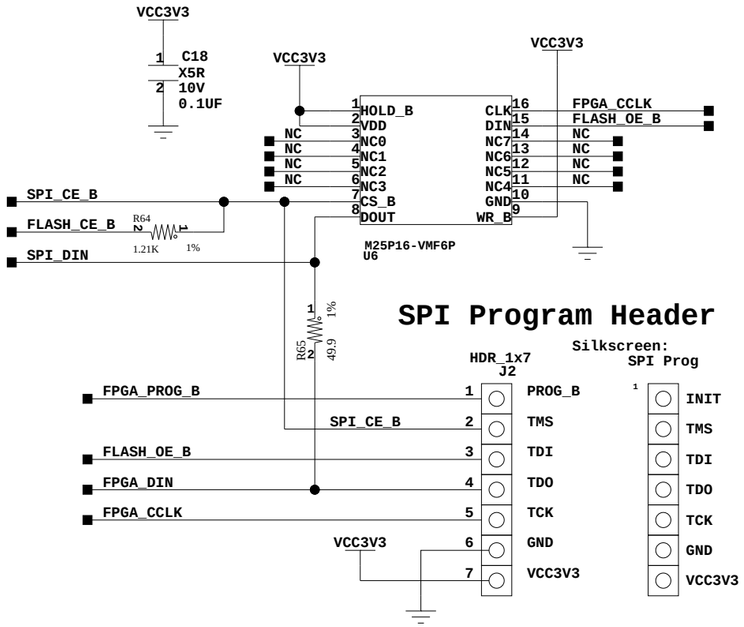


Platform Flash #2

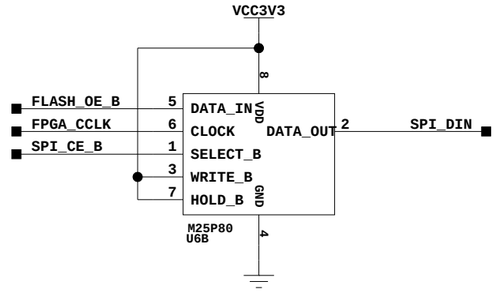




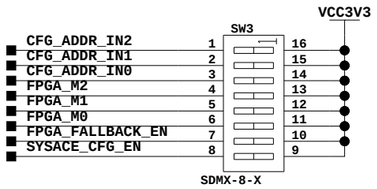
SPI Program Header



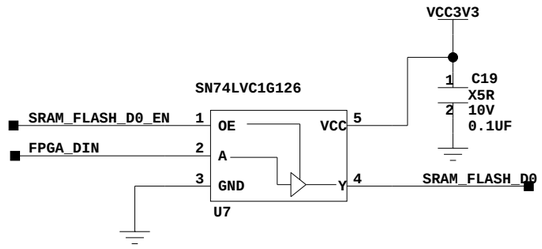
SPI Flash



Silkscreen:
SysACE Config, Mode pins



Config DIP switches



Toggles connection from Plat Flash D0 to SRAM D0

Misc Config
Platform Flash, SPI Flash

Title:	Misc Config,Platform Flash, SPI Flash SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
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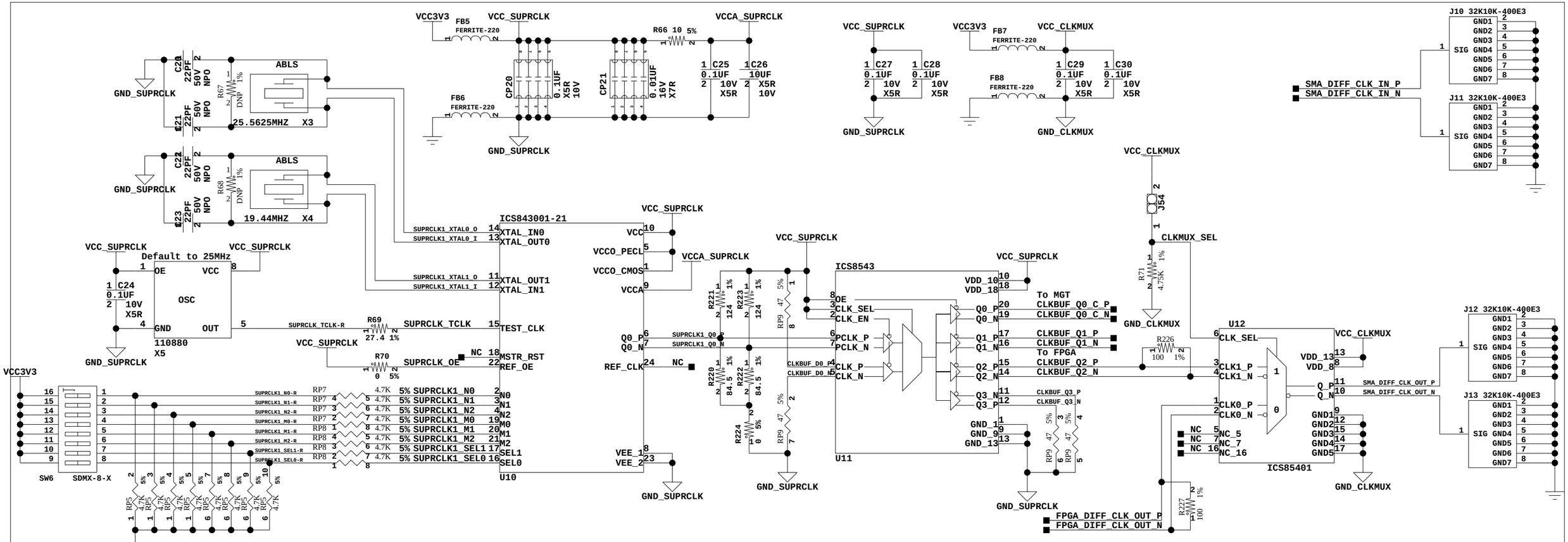
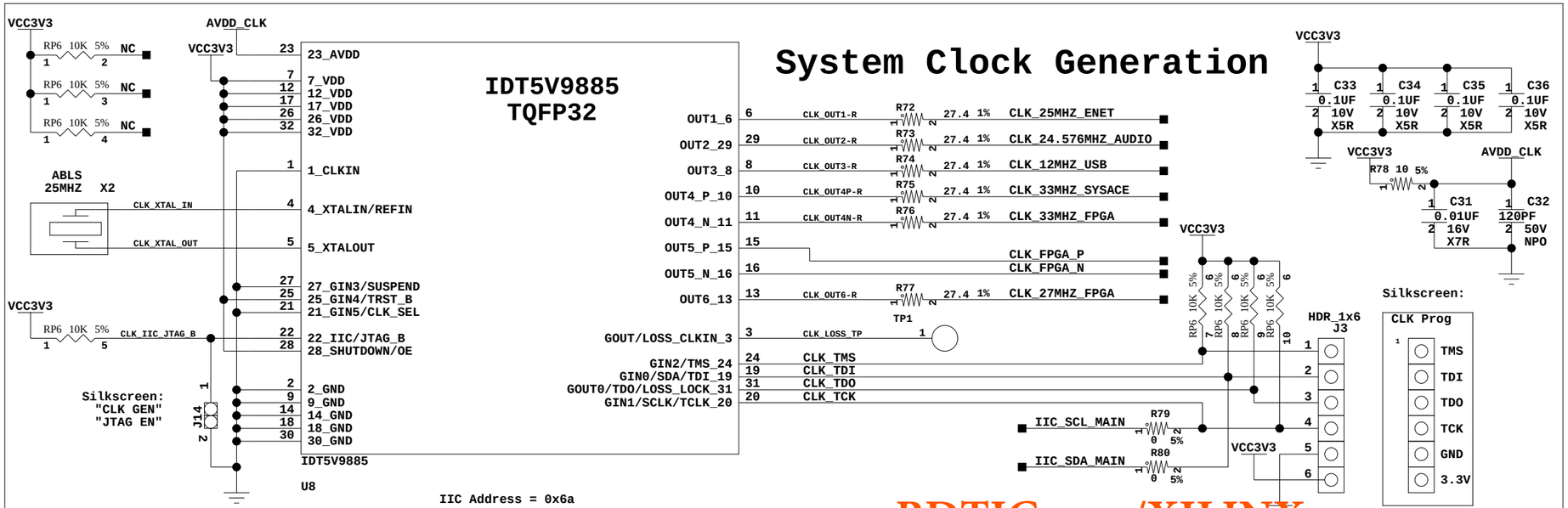
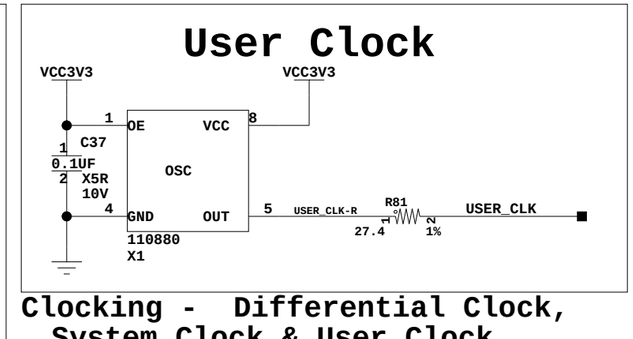
Diff Clocks: SMAs, Generation, MUX and Buffer







Clocking - Differential Clock, System Clock & User Clock

Title:	Differential Clock, System Clock, User Clock SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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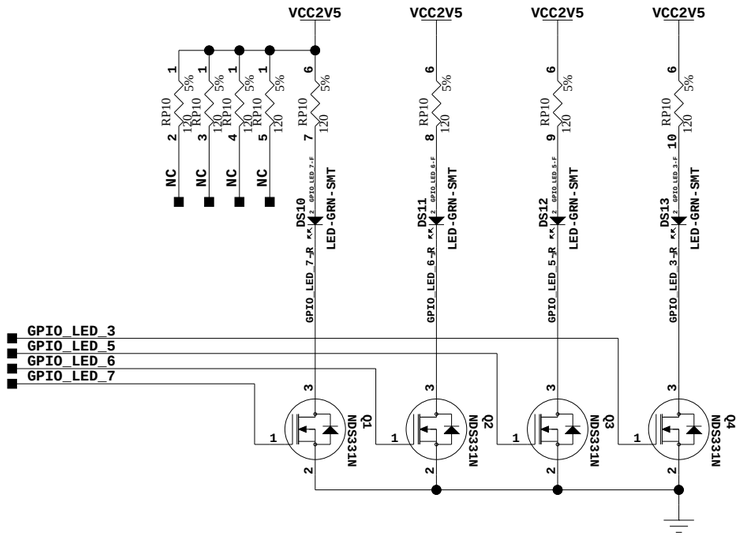
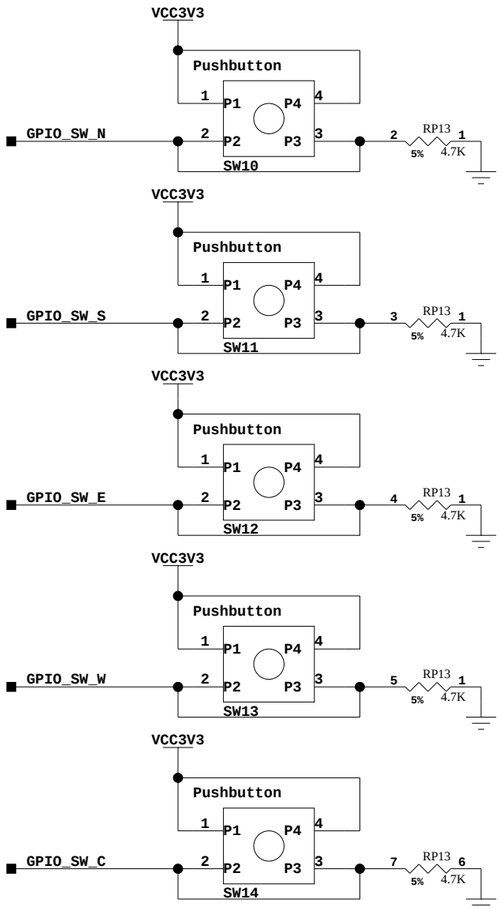
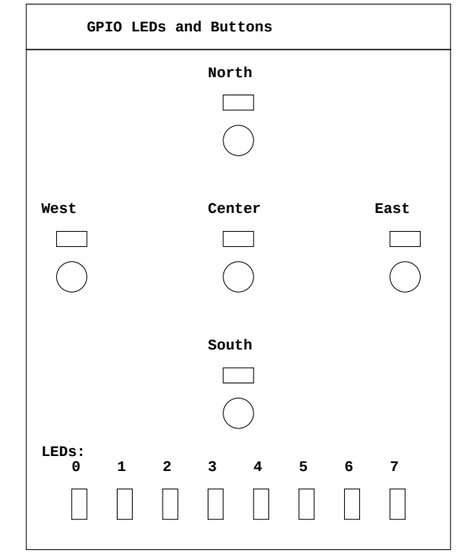
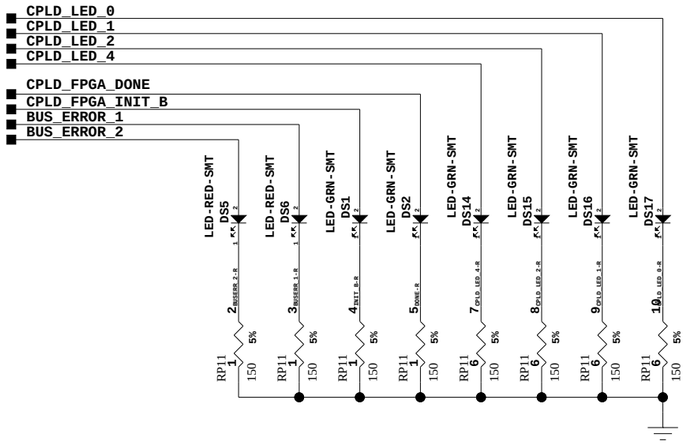
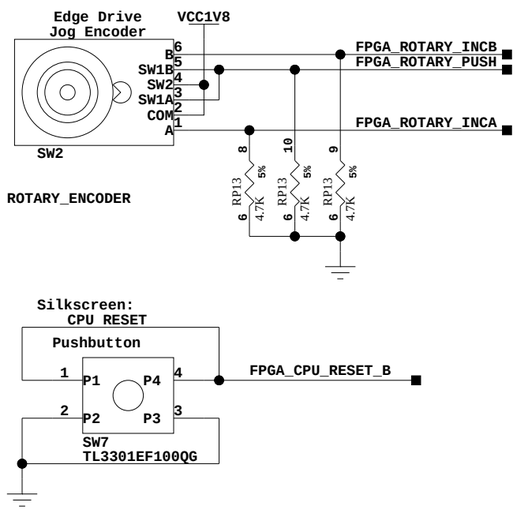


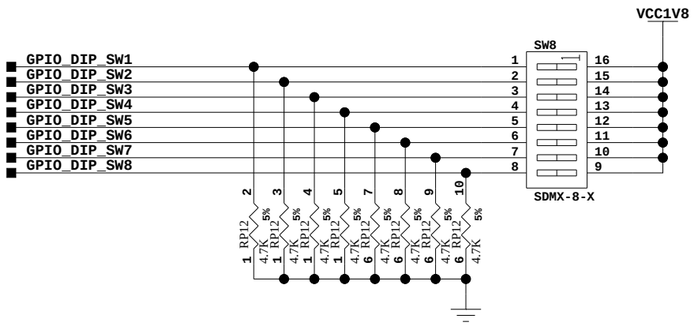


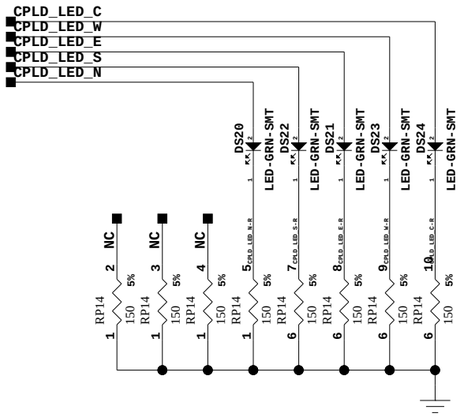


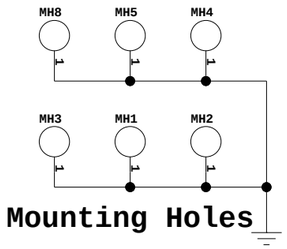




Edge Drive Jog Encoder Switch







Mounting Holes

GPIO - Buttons, LEDs, Switches

XILINX

Title:	GPIO Buttons, LEDs, Switches GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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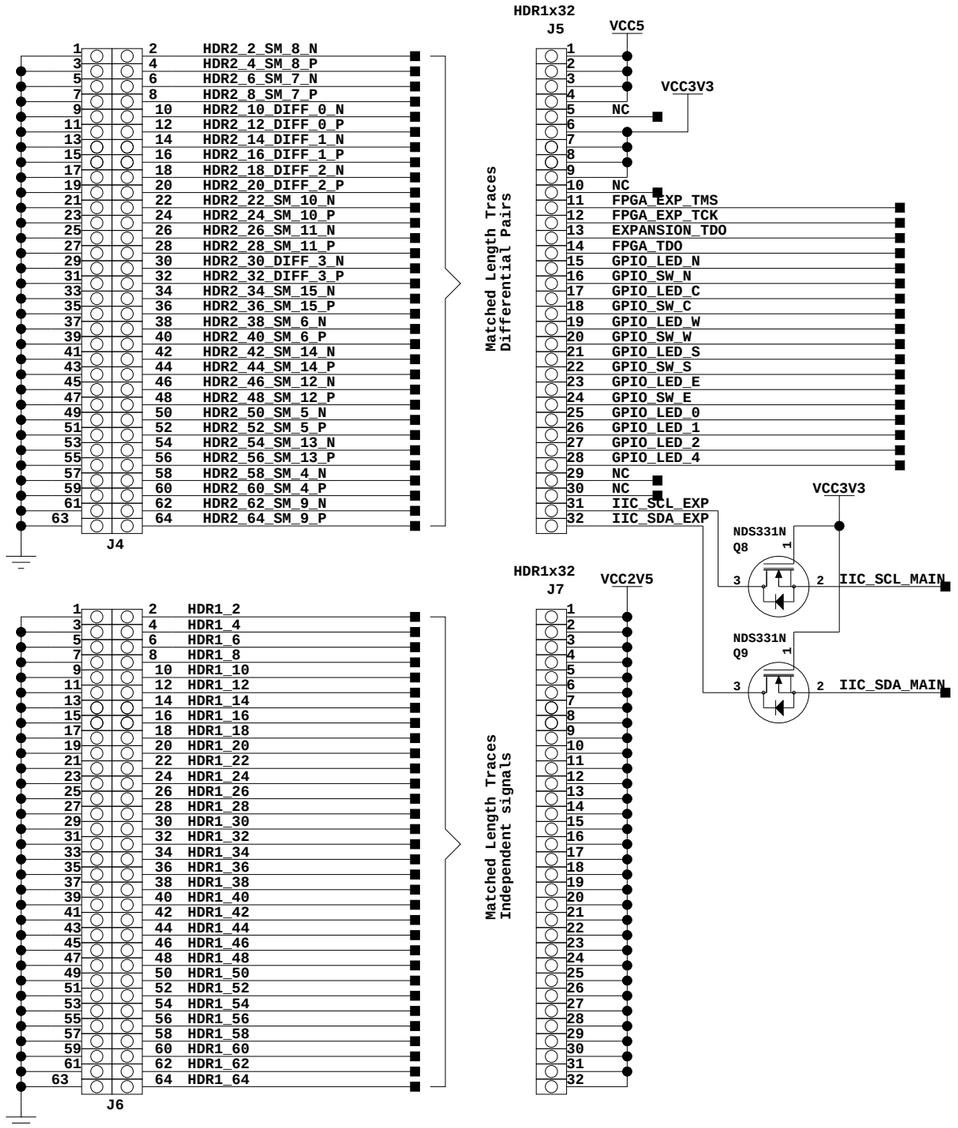
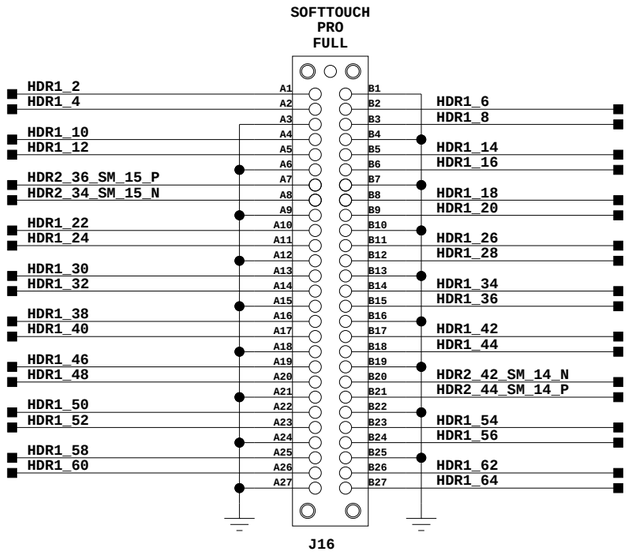
XGI Expansion Interface

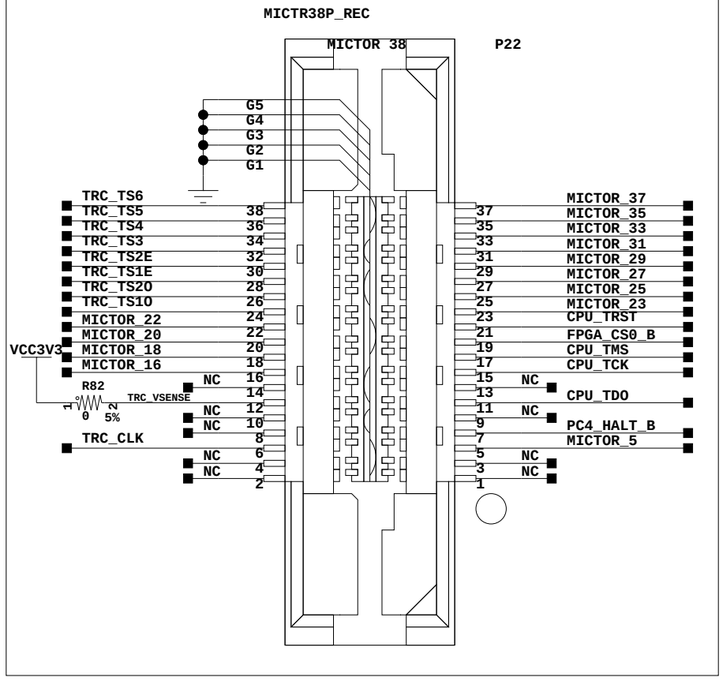


Bank 11/13 Expansion
Connector Voltage
1-3 & 2-4 = 3.3V
3-5 & 4-6 = 2.5V

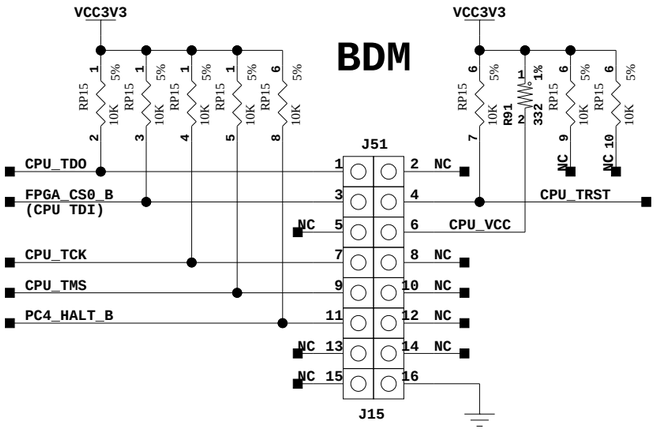
SoftTouch Pro



Mictor



BDM



Mark Pin 1

Pin 14 must be removed.

XGI - Expansion Connector

XILINX

Title:	XGI - Expansion Headers SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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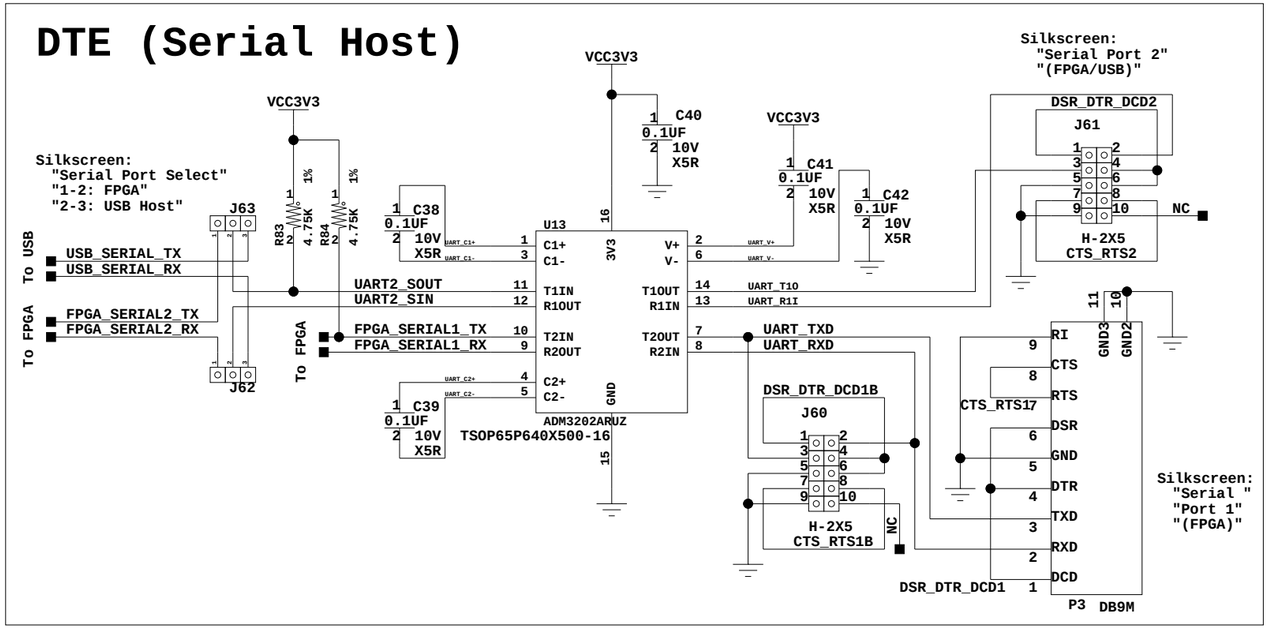
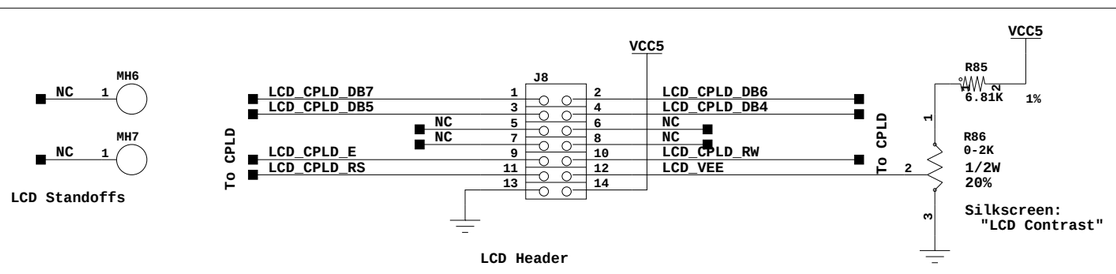
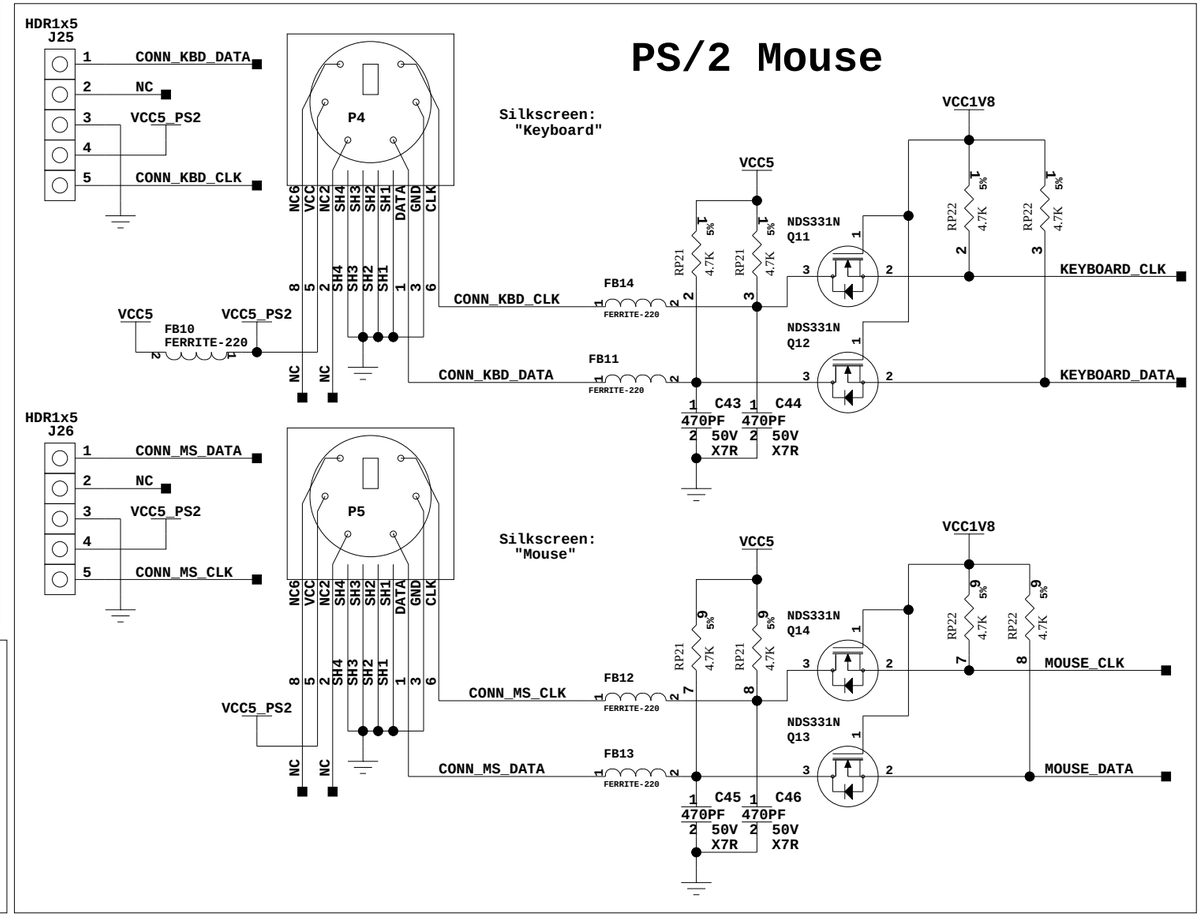
DTE (Serial Host)

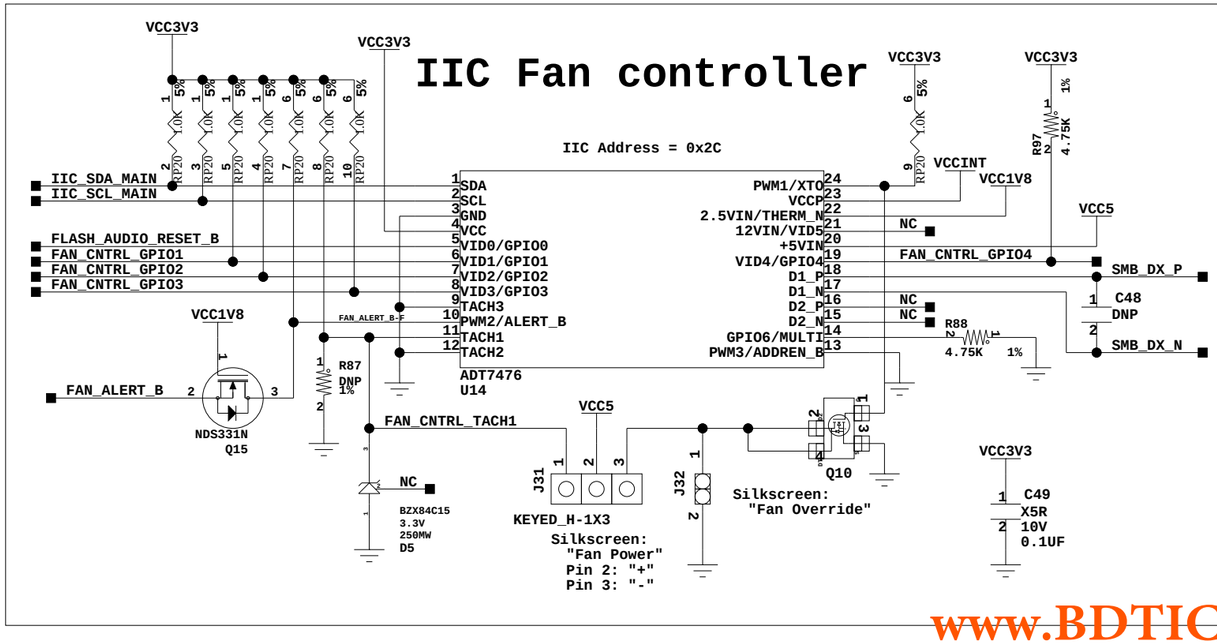




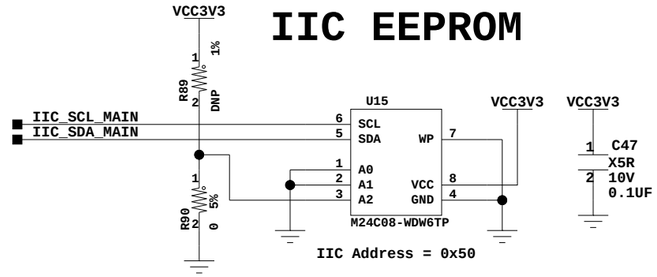
PS/2 Mouse

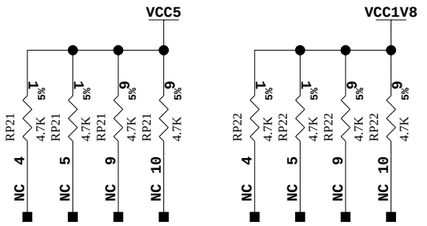


IIC Fan controller



IIC EEPROM





Misc - LCD, PS2, UART, Fan Controller

XILINX

Title:	LCD, PS2, UART, IIC EEPROM, IIC Fan Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:55	Ver:	A
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DDR2 SO-DIMM

Title:	DDR2 SO-DIMM SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date:	1-22-2008_14:51
Ver:	A
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Rev:	02
Sheet	13 of 27
Drawn By	BP

The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

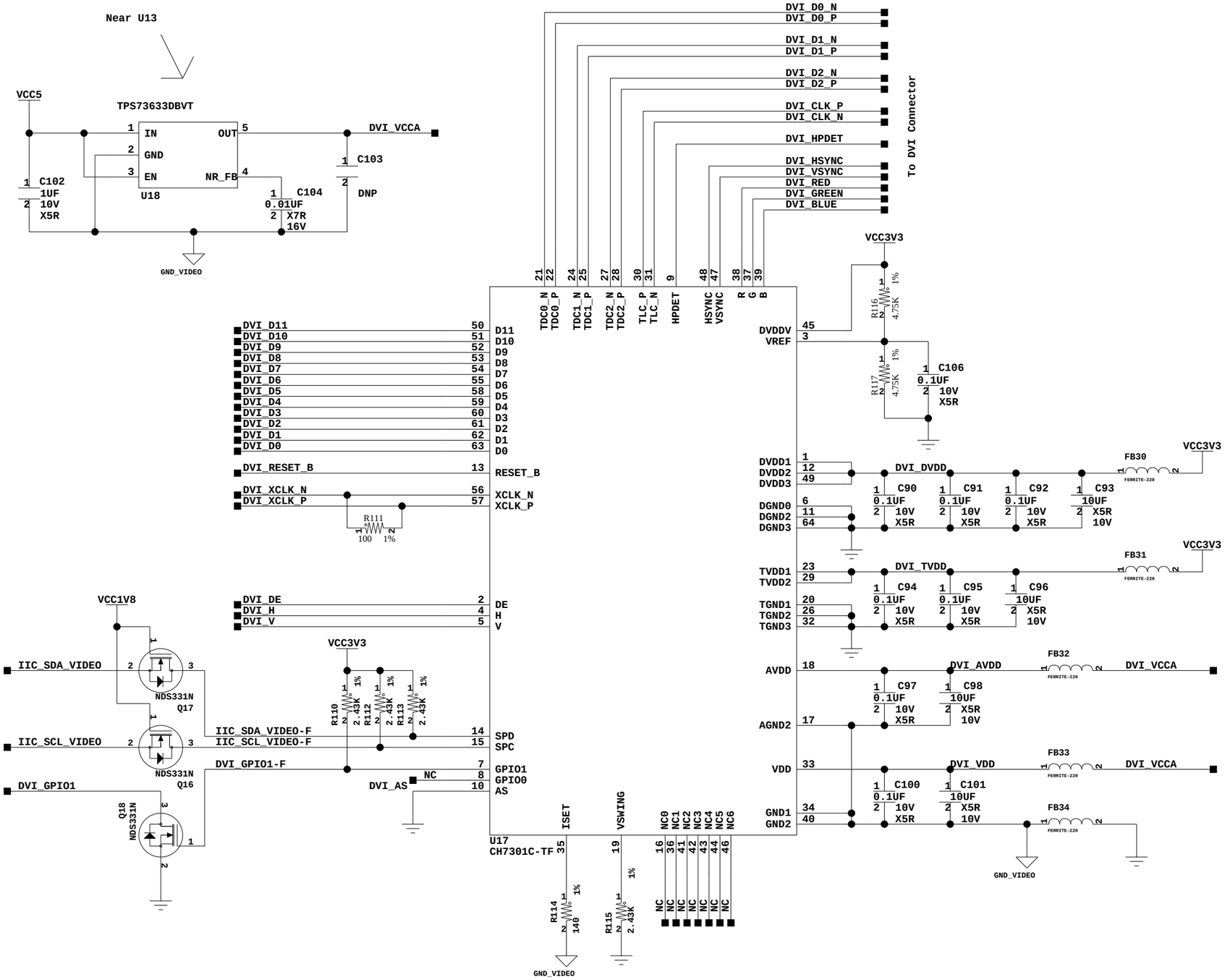
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

J22, J23 pins 1-2: GMII/MII to Cu
J22, J23 pins 2-3: SGMII to Cu, no clk
J22 pins 1-2, J24 ON: RGMII, modified MII in Cu

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date:	1-22-2008_14:51
Ver:	A
Sheet Size: B	
Rev:	02
Sheet	14 of 27
Drawn By	BP

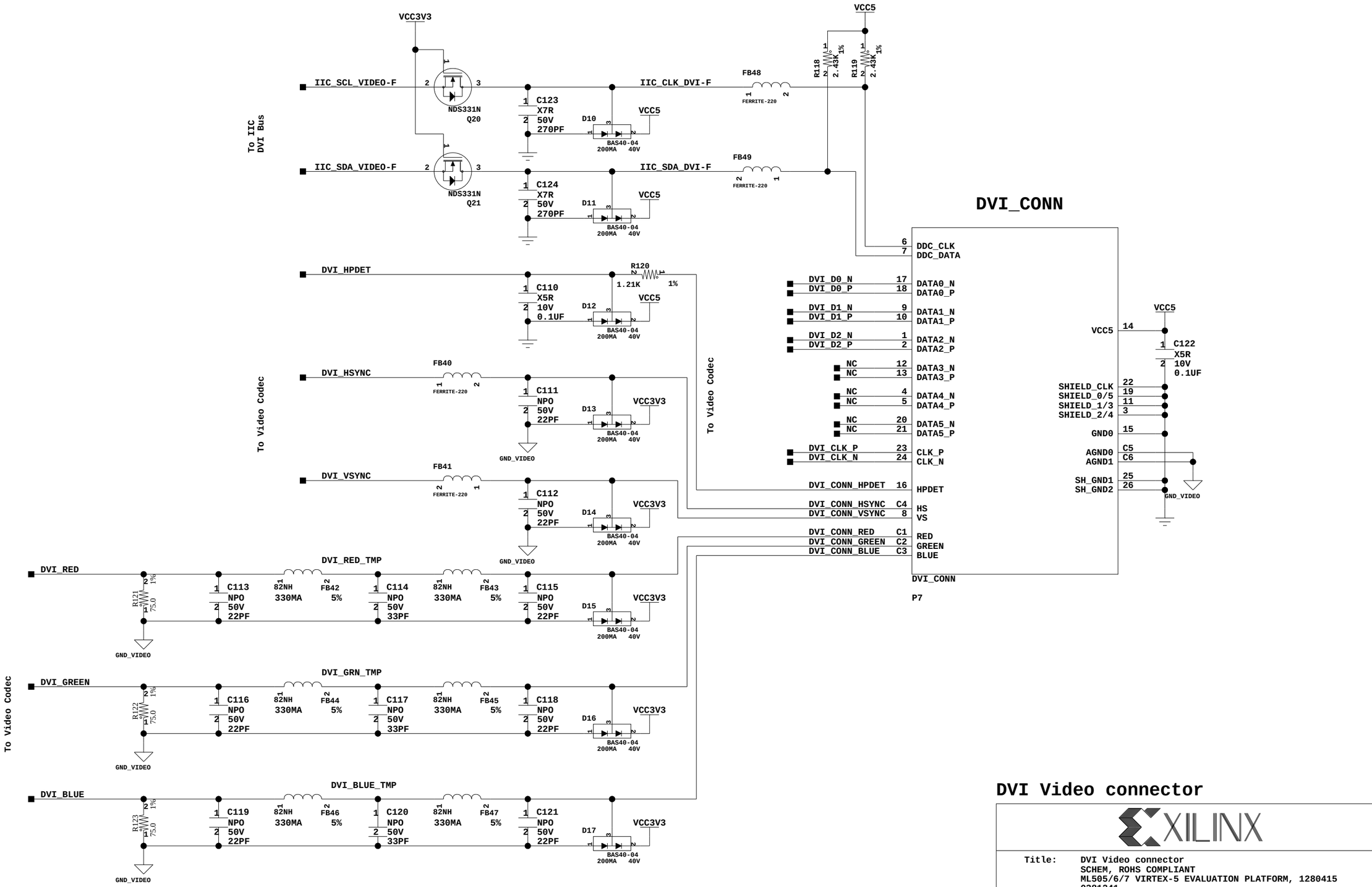


IIC Address = 0x76

VGA Out Codec

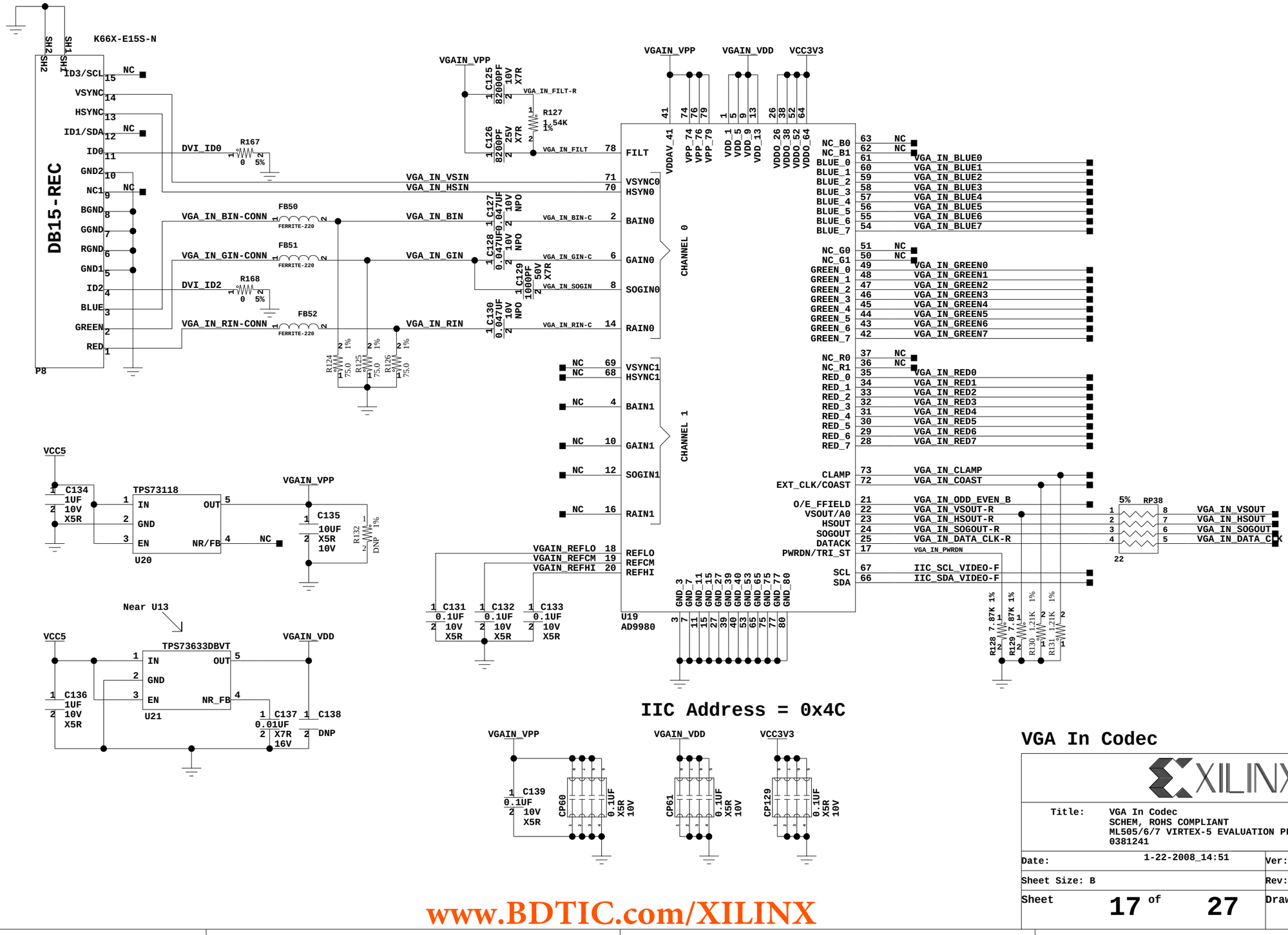
XILINX

Title:	VGA Out Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	15 of 27	Drawn By	BP



DVI Video connector

Title:	DVI Video connector SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	16 of 27	Drawn By	BP



IIC Address = 0x4C

VGA In Codec

XILINX

Title:	VGA In Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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CLK_24.576MHZ_AUDIO
AUDIO_SDATA_OUT
AUDIO_BIT_CLK
AUDIO_SDATA_IN
AUDIO_SYNC
FLASH_AUDIO_RESET_B
PIEZO_SPEAKER

Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat

VCC3V3 SN74LVC1G126 VCC3V3
U45

AUDIO_PHONE

AD1981B
LQFP48

MIC1_IC
MIC2_IC
LINE_IN_L_IC
LINE_IN_R_IC

AUDIO_SPDIF
To CPLD and Back
CPLD_SPDIF_1
CPLD_SPDIF_2
CPLD_SPDIF_3
RCA_SPDIF
Silkscreen: "SPDIF Out"
CON_RCA_TH
RCA_JACK

Silkscreen: "Microphone In"
STEREO_JACK_TH
MIC2_CONN
MIC1_CONN
P10

STEREO_JACK_TH
P11
Silkscreen: "Line In"

AC97
U22
AUDIO_VREF_OUT

VCC5_AUDIO
FB55
FERRITE-220

HP_OUT_R_IC
HP_OUT_L_IC
HP_OUT_R_CONN
HP_OUT_L_CONN
STEREO_JACK_TH
P13
Silkscreen: "Amplified Line Out"

LINE_OUT_R_IC
LINE_OUT_L_IC
LINE_OUT_R_CONN
LINE_OUT_L_CONN
STEREO_JACK_TH
P12
Silkscreen: "Line Out"

MIC2_CONN
MIC1_CONN
LINE_OUT_R_CONN
LINE_OUT_L_CONN
J28
H-2X5

Audio Codec

XILINX

Title:	Audio Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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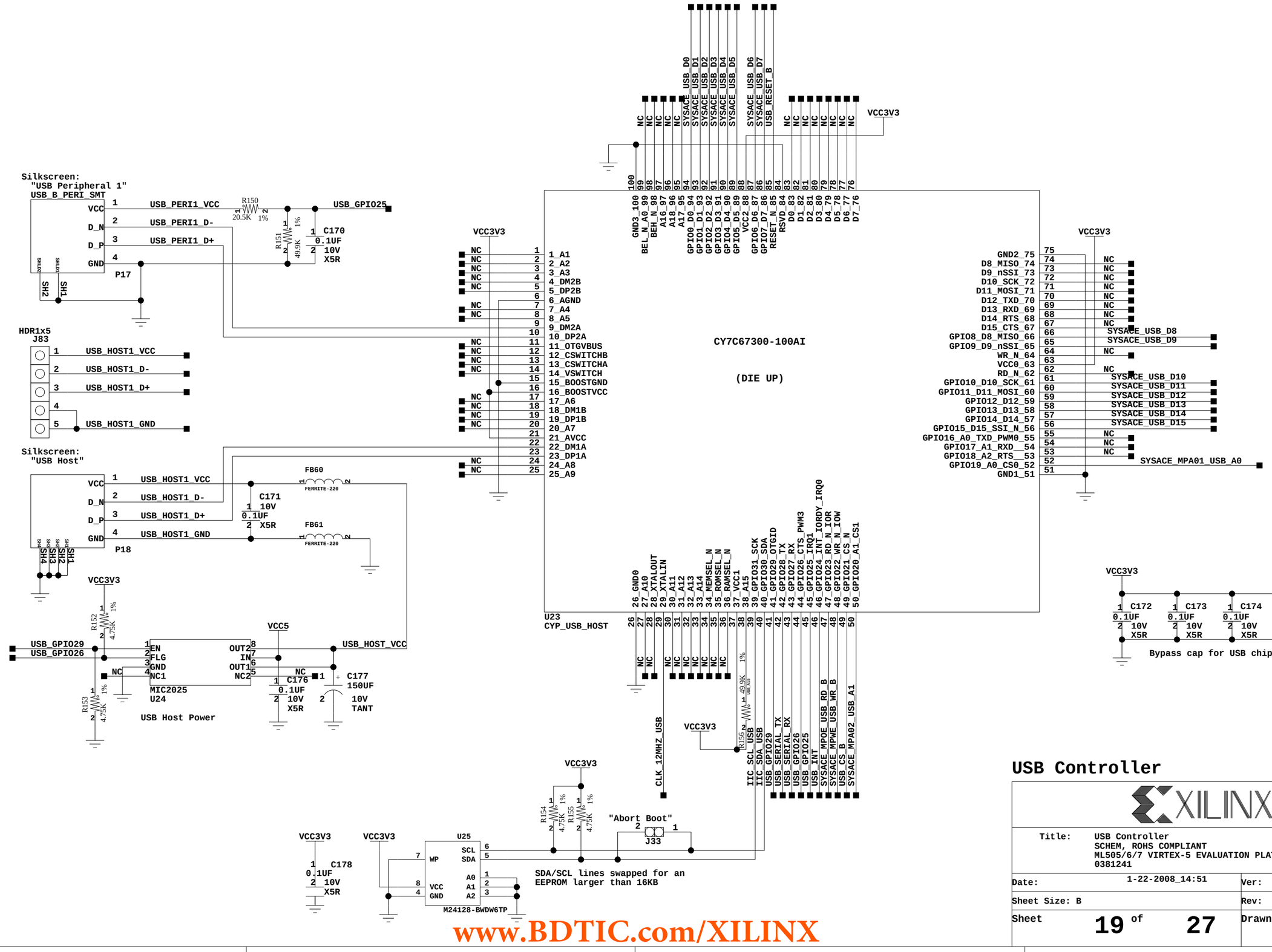

USB Controller

XILINX

Title:	USB Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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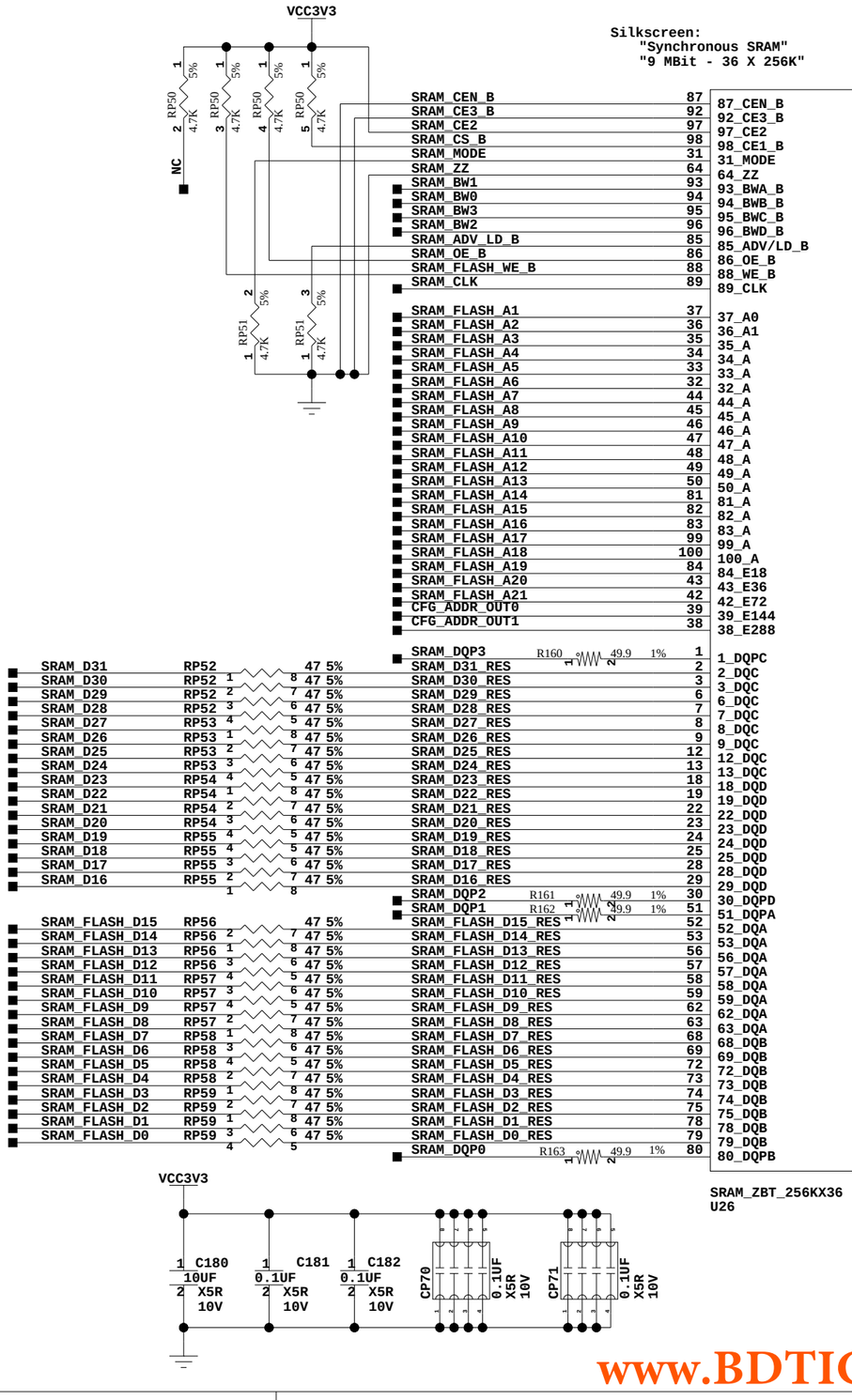
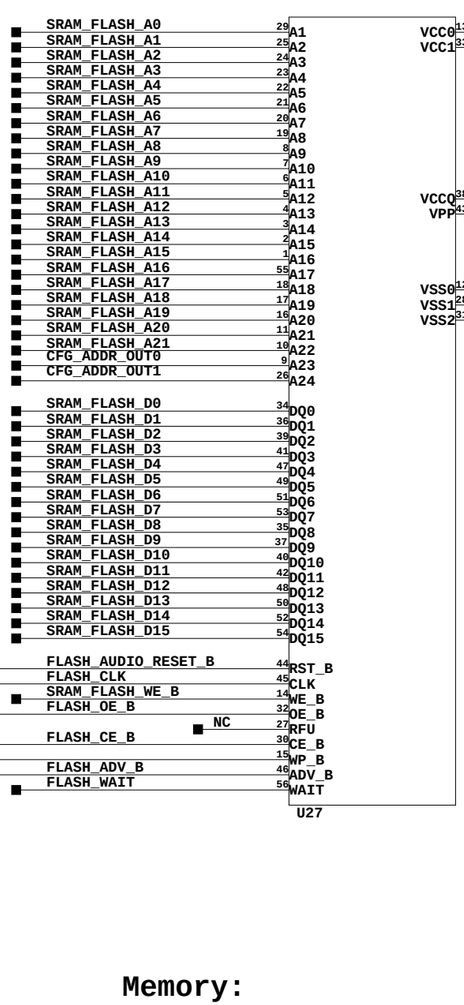
The burst order mode of the SRAM is set to "Linear" by default

Silkscreen:
"Synchronous SRAM"
"9 MBit - 36 X 256K"



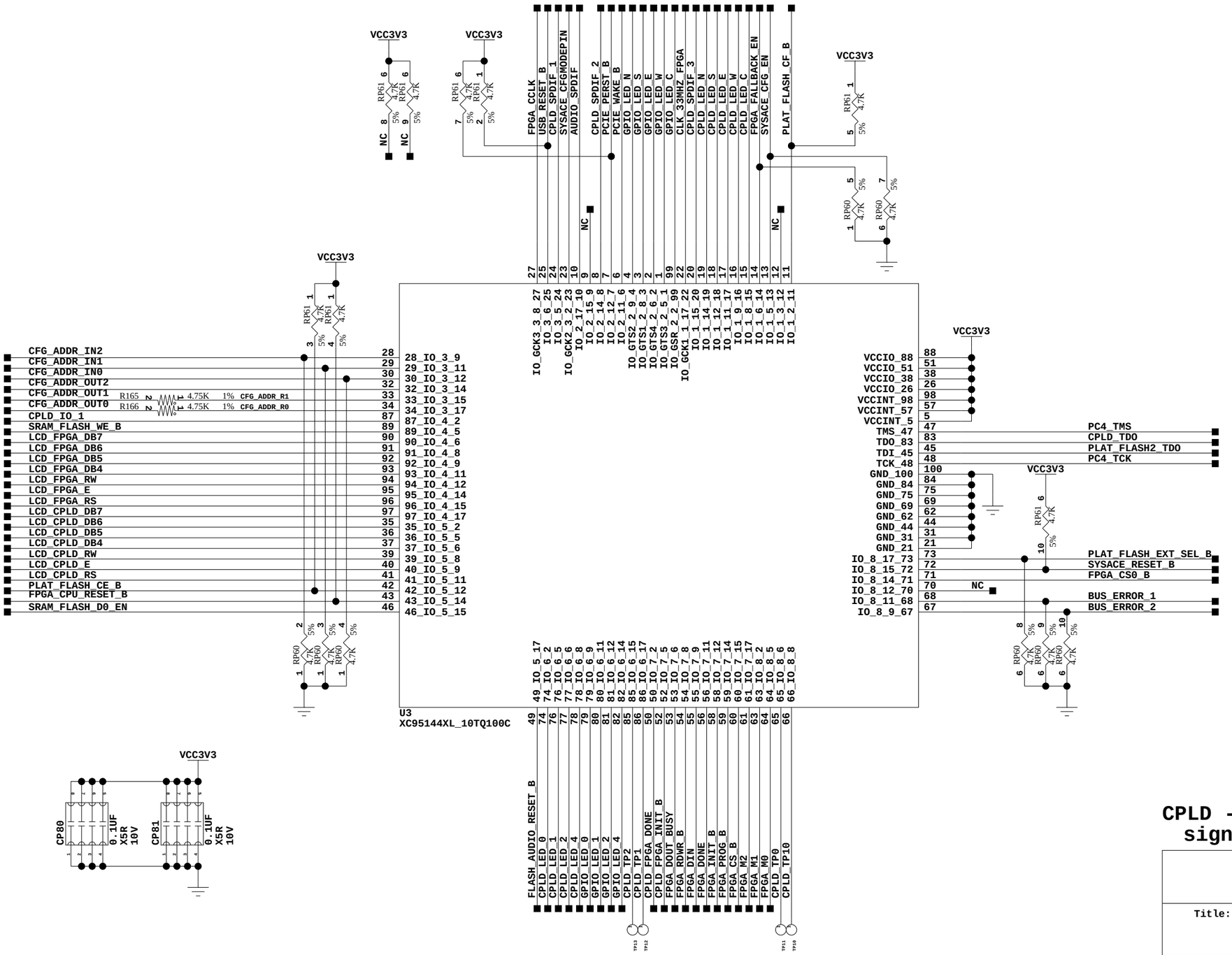
Silkscreen:
"Strata FLASH"
"256 MBit"



Memory:
Synchronous SRAM,
Strata FLASH

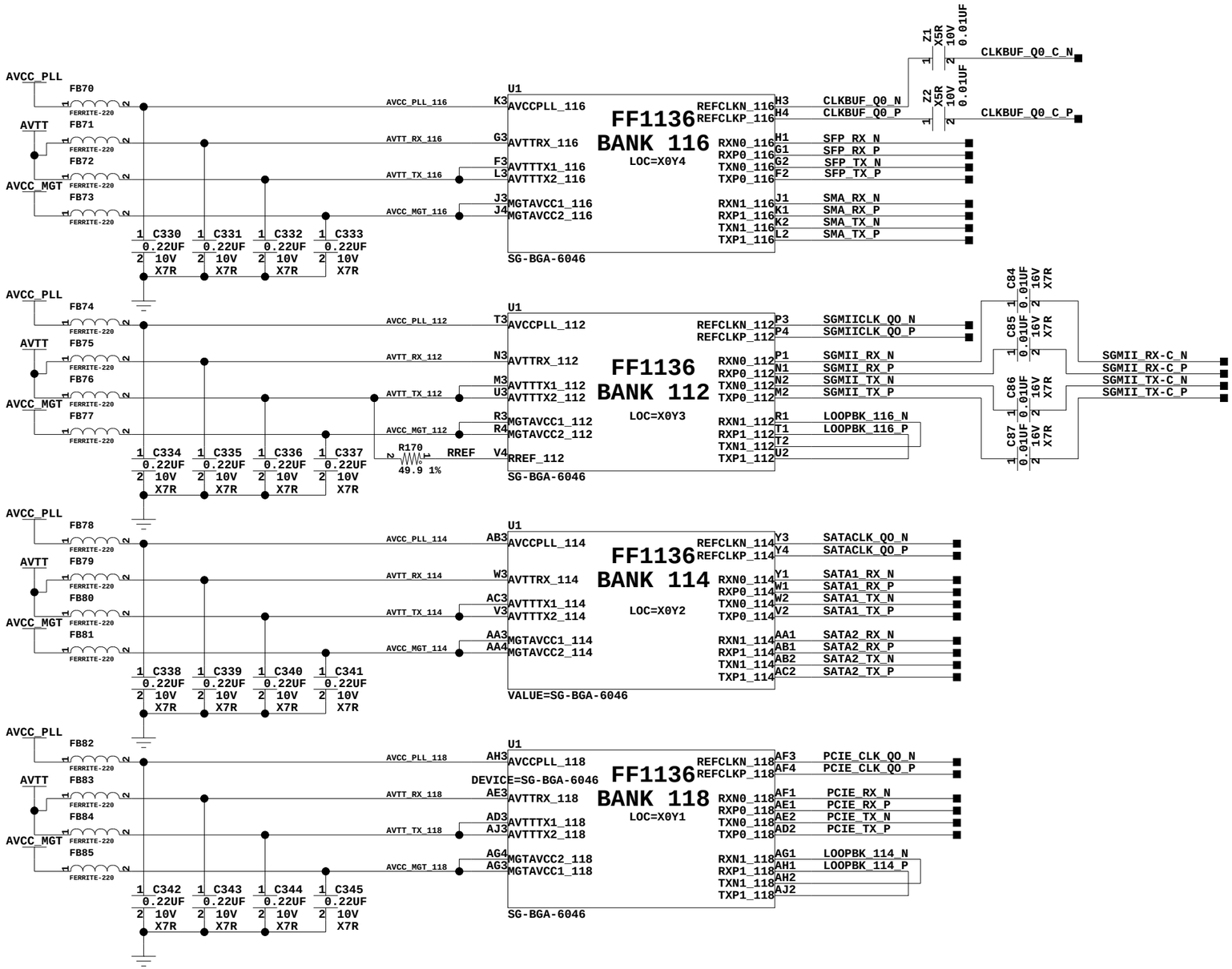
XILINX

Title:	Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	20 of 27	Drawn By	BP



CPLD - Misc signal control

Title:	CPLD - Misc signal control SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
Sheet	21 of 27	Drawn By	BP



Title:	MGT Banks SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241
Date: 1-22-2008_14:55	Ver: A
Sheet Size: B	Rev: 02
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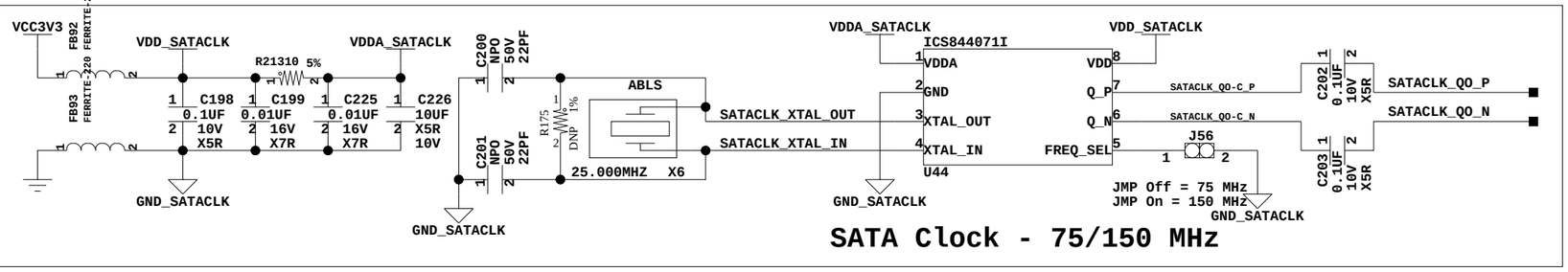
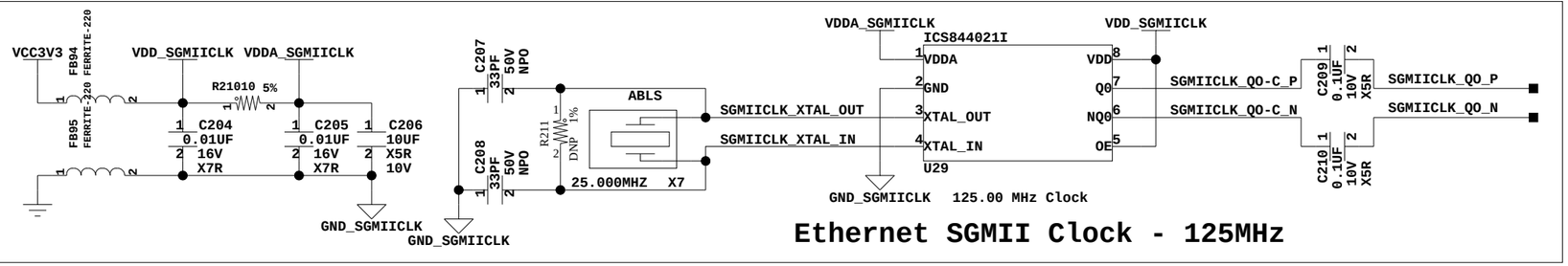
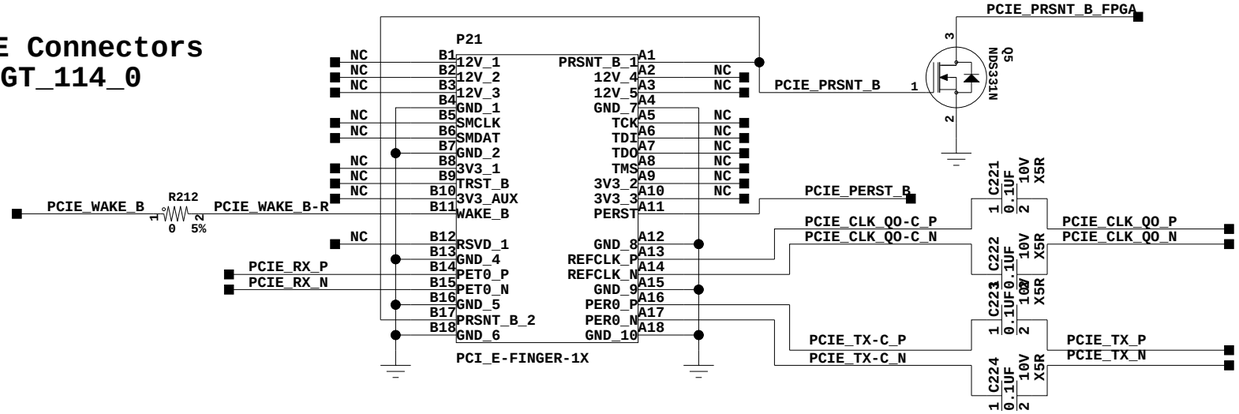


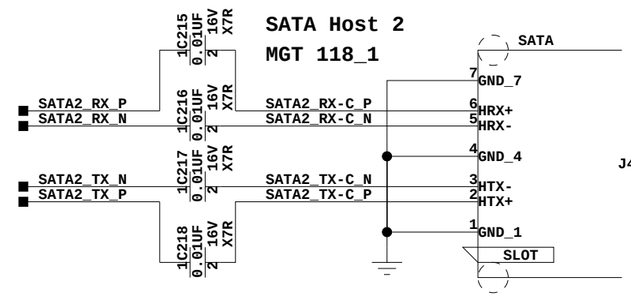
SATA Clock - 75/150 MHz

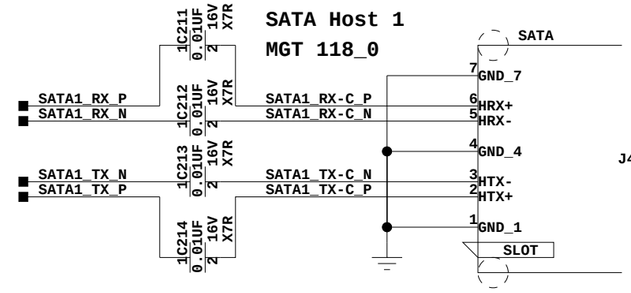


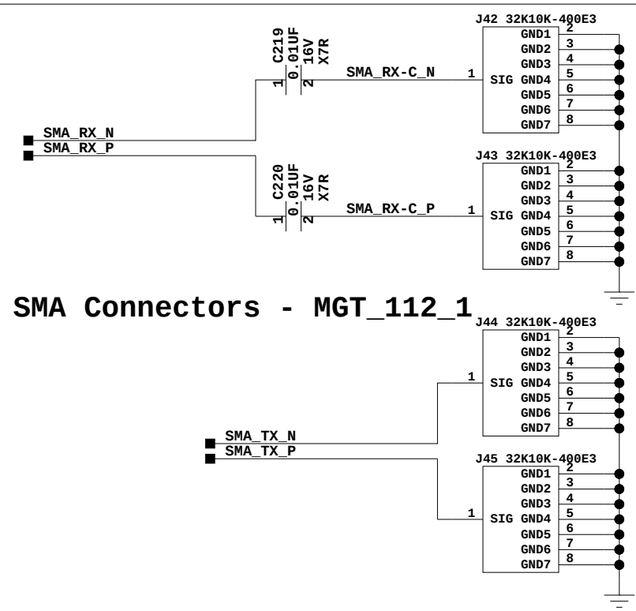
Ethernet SGMII Clock - 125MHz

PCI-E Connectors
MGT_114_0

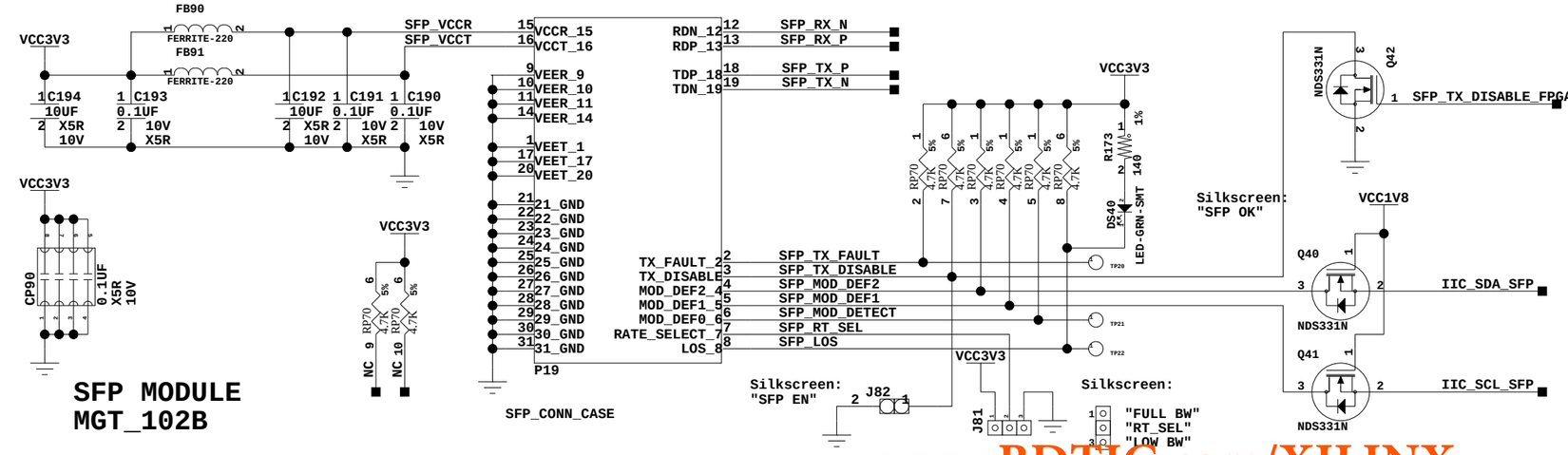








SMA Connectors - MGT_112_1



MGT Clocks and Connectors

Title:	MGT Connectors SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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MGT PLL Regulator

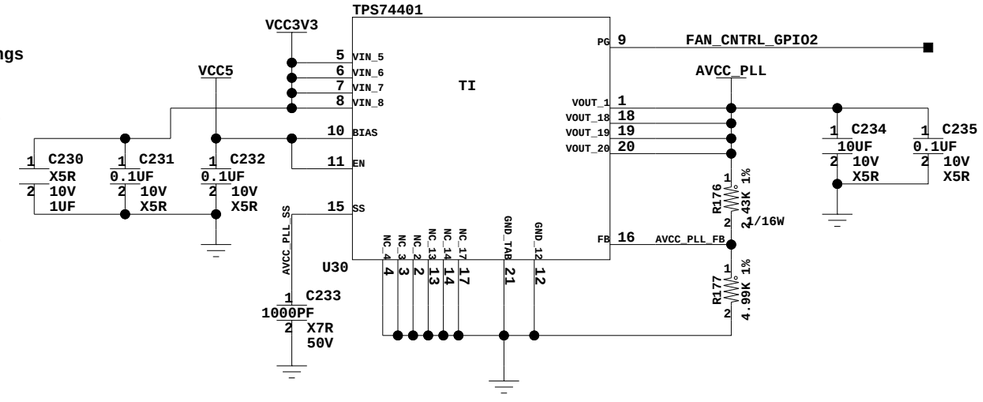
Voltage Output Settings

LXT & SXT (ML505/6)
AVCC_PLL = 1.2V @ 3A

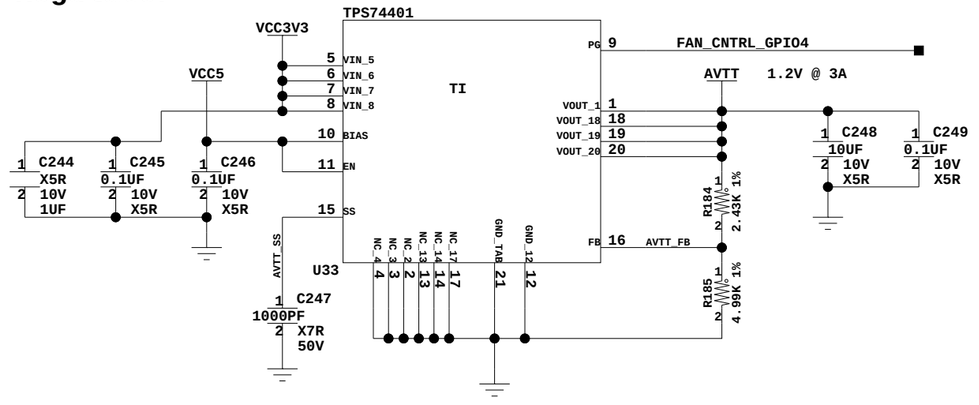
R176 = 2.43K 1%
R177 = 4.99K 1%

FXT Only (ML507)
AVCC_PLL = 1.0V @ 3A

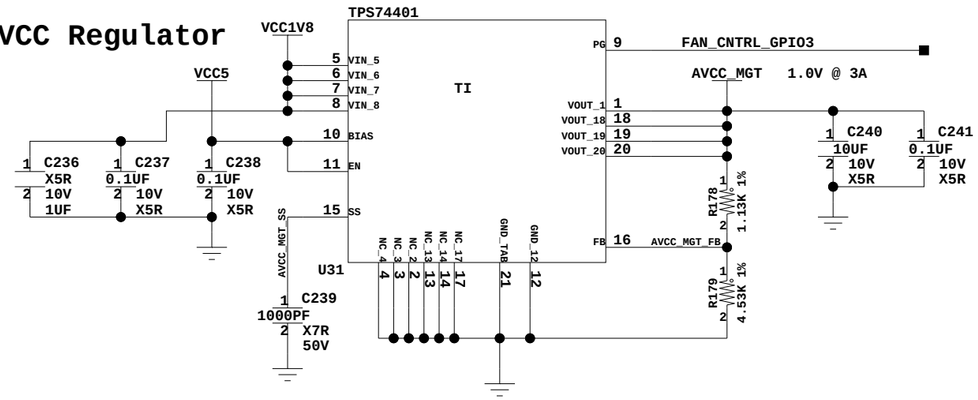
R176 = 1.13K 1%
R177 = 4.53K 1%



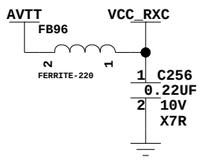
MGT VTT Regulator



MGT AVCC Regulator



MGT RXC Regulator



MGT Power Supplies

XILINX

Title:	MGT Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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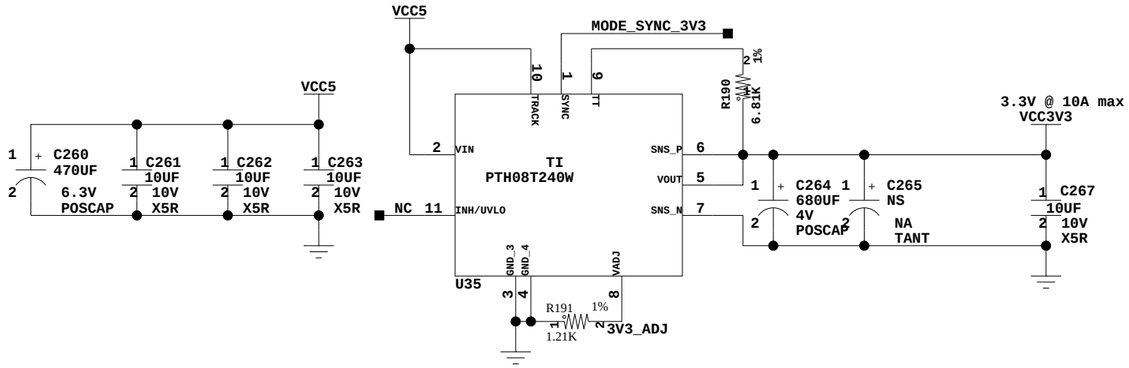
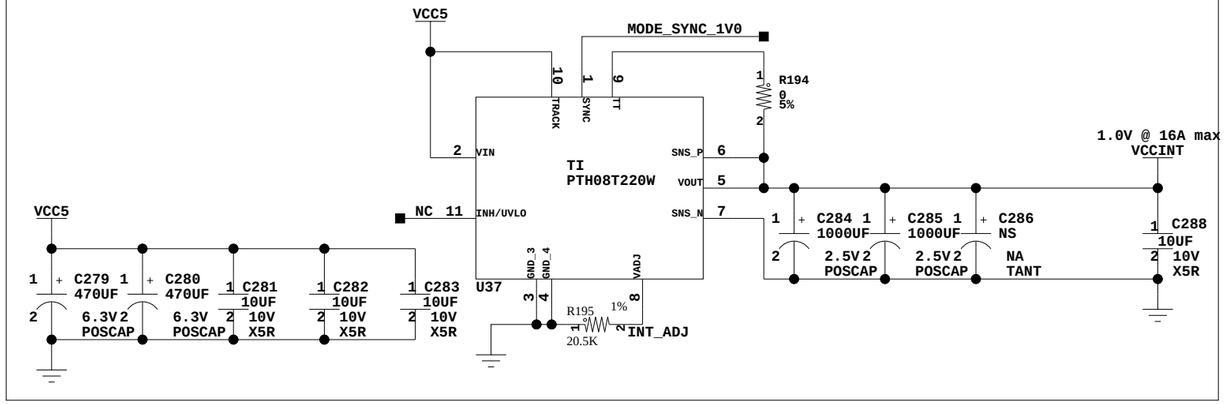
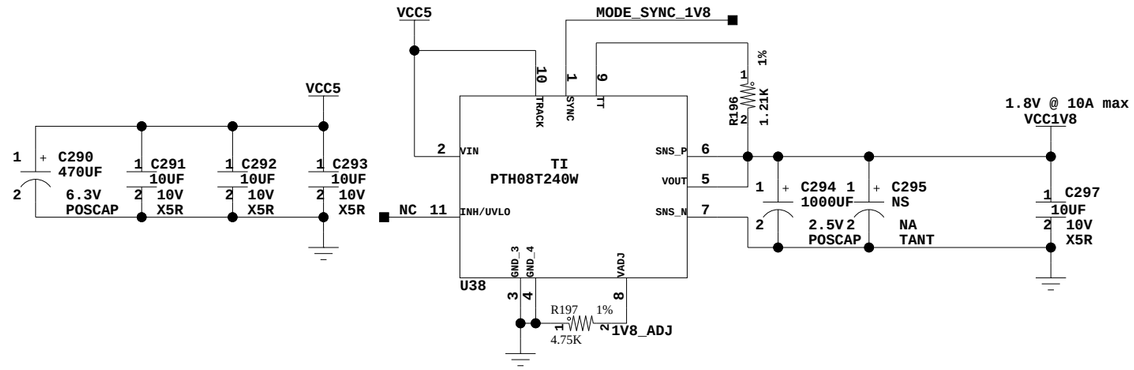
5v to 3.3V Regulator



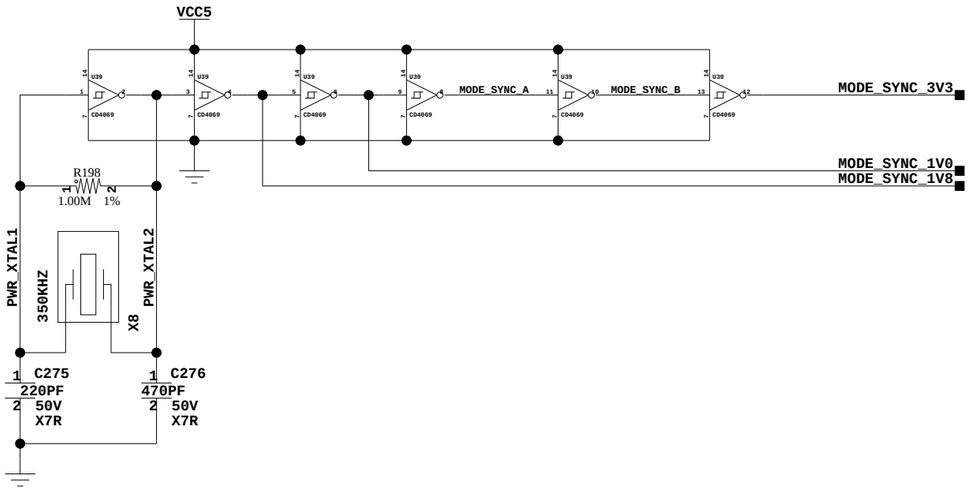
5v to 1.0V Regulator



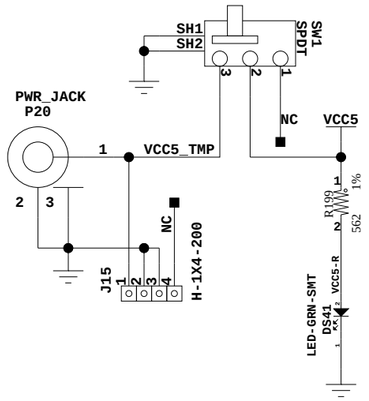
5v to 1.8V Regulator



5V Power Synchronizing Circuit



5V Power - Jack, Switch and LED



5V Power Supplies

XILINX

Title:	Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
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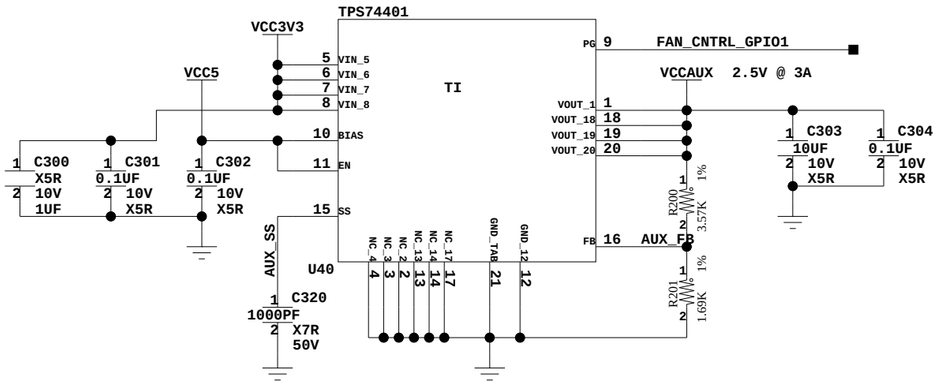
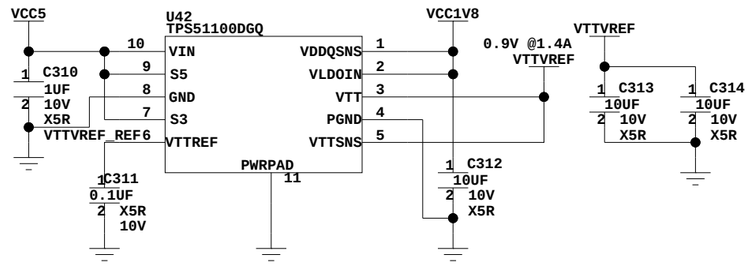
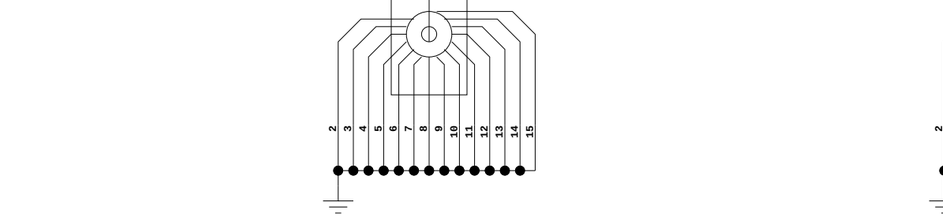
3.3v to 2.5V (VCC AUX) Regulator



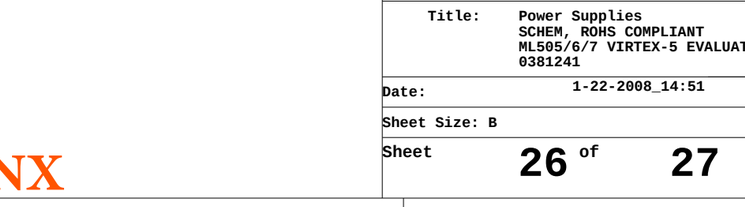
5V to 0.9V (DDR VTT VREF) Regulator

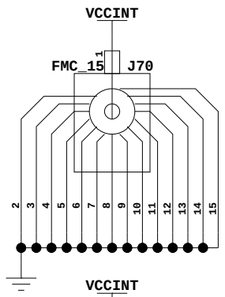


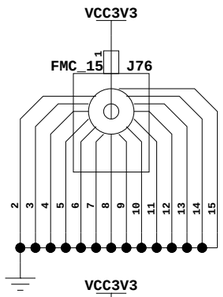
3.3v to 2.5V Regulator

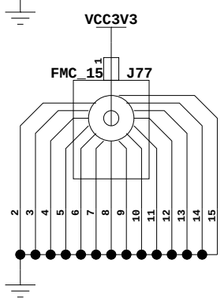


5V to 0.9V (DDR2 VTT DDR) Regulator









5V and 3.3V Power Supplies

XILINX

Title:	Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date:	1-22-2008_14:51	Ver:	A
Sheet Size: B		Rev:	02
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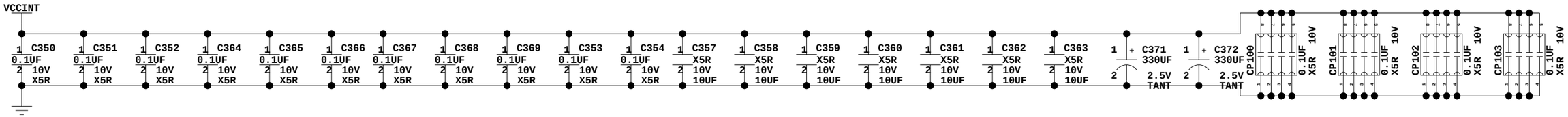
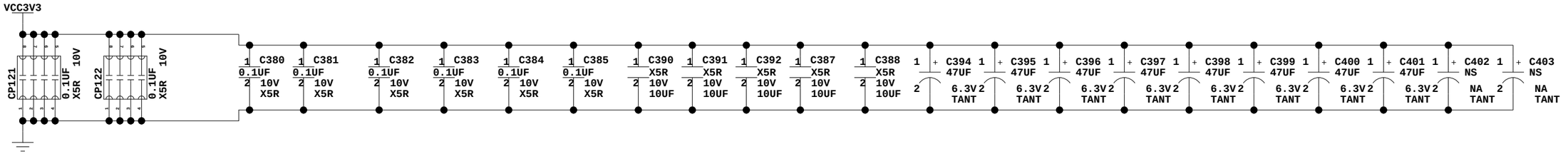
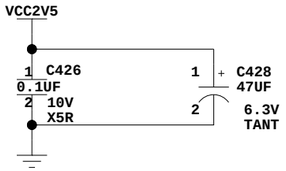
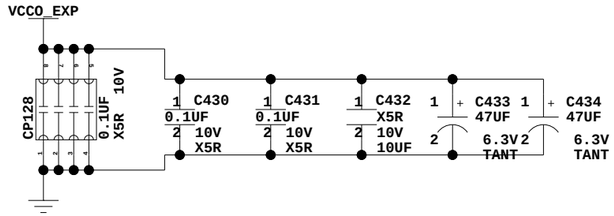
VCCINT Caps

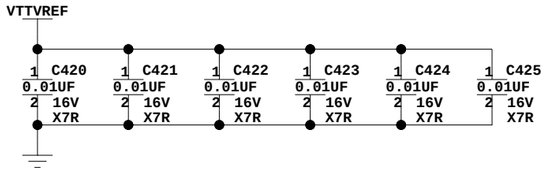


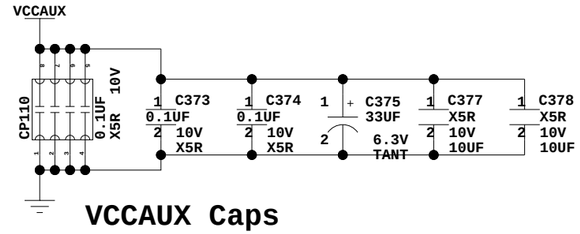
VCCO Caps



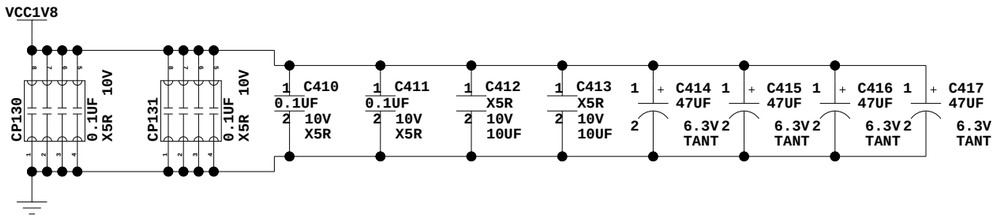








VCCAUX Caps



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Date:	1-22-2008_14:51	Ver:	A
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