38V, 10A DC/DC µModule Regulator with Advanced Input and Load Protection

FEATURES

- **Wide Operating Input Voltage Range: 4.5V to 38V**
- **10A DC Typical, 12A Peak Output Current**
- **Output Range: 0.6V to 6V**
- **±1.5% Maximum Total Output DC Voltage Error**
- **Differential Remote Sense Amplifier for POL Regulation**
- **Internal Temperature, Analog Indicator Output**
- **Overcurrent Foldback and Overtemperature Protection**
- **Current Mode Control/Fast Transient Response**
- **Parallelable for Higher Output Current**
- Selectable Pulse-Skipping Operation
- Soft-Start/Voltage Tracking/Pre-Bias Start-Up
- 15mm × 15mm × 5.01mm BGA Package

Input Protection

- UVLO, Overvoltage Shutdown and Latchoff Thresholds
- N-Channel Overvoltage Power-Interrupt MOSFET Driver
- Surge Stopper Capable with Few External Components

Load Protection

- Robust, Resettable Latchoff Overvoltage Protection
- N-Channel Overvoltage Crowbar Power MOSFET Driver

APPLICATIONS

- Ruggedized Electronics
- Avionics and Industrial Equipment

DESCRIPTION

The LTM®4641 is a switch mode step-down DC/DC µModule® (micromodule) regulator with advanced input and load protection features. Trip detection thresholds for the following faults are customizable: input undervoltage, overtemperature, input overvoltage and output overvoltage. Select fault conditions can be set for latchoff or hysteretic restart response—or disabled. Included in the package are the switching controller and housekeeping ICs, power MOSFETs, inductor, overvoltage drivers, biasing circuitry and supporting components. Operating from input voltages of 4V to 38V (4.5V start-up), the device supports output voltages from 0.6V to 6V, set by an external resistor network remote sensing the point-of-load's voltage.

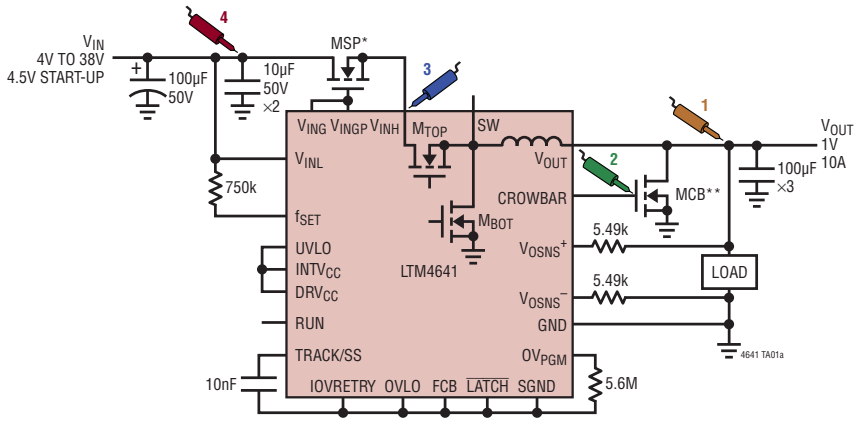
The LTM4641's high efficiency design can deliver up to 10A continuous current with a few input and output capacitors. The regulator's constant on-time current mode control architecture enables high step-down ratios and fast response to transient line and load changes. The LTM4641 is offered in a 15mm × 15mm × 5.01mm RoHS compliant BGA package with Pb-free finish.

LT, LTC, LTM, µModule, Burst Mode, Linear Technology and the Linear logo are registered trademarks and LTpowerCAD is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 5847554, 6100678, 6304066, 6580258, 6677210.

Click to view associated TechClip Videos.

TYPICAL APPLICATION

µModule Regulator with Input Disconnect and Fast Crowbar Output Overvoltage Protection

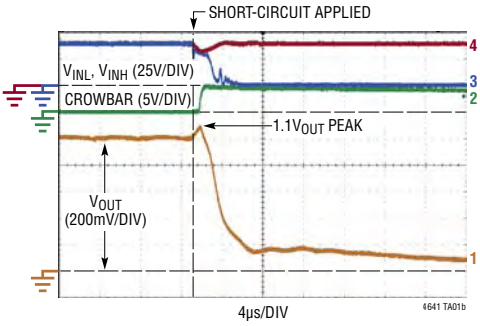


SGND CONNECTS TO GND INTERNAL TO µMODULE REGULATOR

*MSP: (OPTIONAL) SERIES-PASS OVERVOLTAGE POWER INTERRUPT MOSFET, NXP PSMN014-60LS

**MCB: (OPTIONAL) OUTPUT OVERVOLTAGE CROWBAR MOSFET, NXP PH2625L

1V Load Protected from M_{TOP} Short-Circuit at $38V_{IN}$



TESTED AT WORST-CASE CONDITION: NO LOAD

TABLE OF CONTENTS

Features 1
Applications 1
Typical Application 1
Description 1
Absolute Maximum Ratings 3
Order Information 3
Pin Configuration 3
Electrical Characteristics 4
Typical Performance Characteristics 8
Pin Functions 10
Simplified Block Diagram 15
Decoupling Requirements 15
Operation 16
Introduction 16
Motivation 16
Power µModule Regulator Reliability 16
Overview 16
Applications Information—Power Supply Features . 17
Power (V_{INH}) and Bias (V_{INL}) Input Pins 17
Switching Frequency (On Time) Selection and Voltage Dropout Criteria (Achievable V_{IN}-to-V_{OUT} Step-Down Ratios) 18
Setting the Output Voltage; the Differential Remote Sense Amplifier 21
Input Capacitors 23
Output Capacitors and Loop Stability/Loop Compensation 23
Pulse-Skipping Mode vs Forced Continuous Mode 24
Soft-Start, Rail-Tracking and Start-Up Into Pre-Bias 24
$INTV_{CC}$ and DRV_{CC} 27
$1V_{REF}$ 28
TEMP, OTBH and Overtemperature Protection 28
Input Monitoring Pins: UVLO, IOVRETRY, OVLO 29
Applications Information—Input Protection Features 29
Start-Up/Shutdown and Run Enable; Power-On Reset and Timeout Delay Time 31
Applications Information—Load Protection Features 32
Overcurrent Foldback Protection 32
Power Good Indicator and Latching Output Overvoltage Protection 32
Power-Interrupt MOSFET (MSP), CROWBAR Pin and Output CROWBAR MOSFET (MCB) 33
Fast Output Overvoltage Comparator Threshold 34
The Switching Node: SW Pin 35
Applications Information—EMI Performance 35
Applications Information—Multimodule Parallel Operation 36
Applications Information—Thermal Considerations and Output Current Derating 38
Thermal Considerations and Output Current Derating 38
Applications Information—Output Capacitance Table 45
Applications Information—Safety and Layout Guidance 46
Safety Considerations 46
Layout Checklist/Example 46
Typical Applications 48
Appendices 56
Appendix A. Functional Block Diagram and Features Quick Reference Guide 56
Appendix B. Start-Up/Shutdown State Diagram 57
Appendix C. Switching Frequency Considerations and Usage of R_{fSET} 58
Appendix D. Remote Sensing in Harsh Environments 59
Appendix E. Inspiration For Pulse-Skipping Mode Operation 60
Appendix F. Adjusting the Fast Output Overvoltage Comparator Threshold 60
Package Description 63
Package Photo 63
Package Description 64
Revision History 65
Typical Application 66
Related Parts 66

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages

- V_{INL}, V_{INH}, SW, f_{SET} ..... –0.3V to 40V
- V_{OUT} ..... –0.3V to 9.2V
- V_{ING} ..... –0.3V to V_{INH} + 20V
- $INTV_{CC}$, DRV_{CC}, RUN, TRACK/SS, PGOOD, CROWBAR, HYST ..... –0.3V to 6V
- FCB, TMR ..... -0.3V to $INTV_{CC}$ + 0.3V
- COMP ..... –0.3V to 2.7V
- V_{OSNS}^+, V_{ORB}^+ ..... –0.6V to 9.7V
- V_{OSNS}^-, V_{ORB}^- ..... V_{OSNS}^+ – 2.7V to V_{OSNS}^+ + 0.3V
- $\overline{OTBH}$, UVLO, IOVRETRY, OVLO, $\overline{LATCH}$ ..... –0.3V to 7.5V
- TEMP, OV_{PGM} ..... –0.3V to 1.5V

Terminal Currents

- $INTV_{CC}$ (Continuous) ..... –30mA
- $INTV_{CC}$ (Continuous; CROWBAR Sourcing 15mA) ..... –15mA
- CROWBAR (Continuous) ..... –15mA
- V_{INGP} (Continuous) ..... –50mA to 15mA
- $1V_{REF}$ (Continuous) ..... –1mA to 1mA

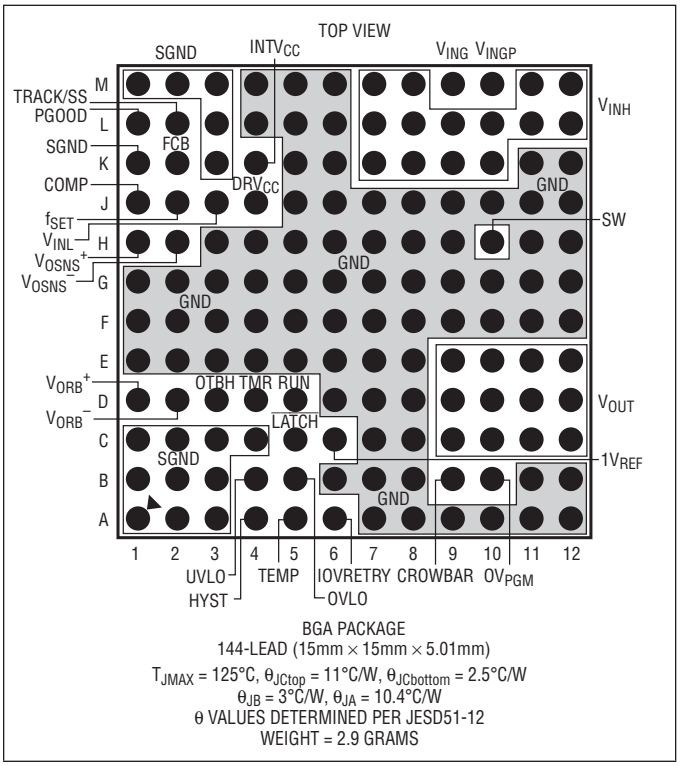
Internal Operating Temperature Range (Note 2)

- E- and I-Grades ..... –40°C to 125°C
- MP-Grade ..... –55°C to 125°C

Storage Temperature Range ..... –55°C to 125°C

Peak Package Body Temperature (SMT Reflow) ... 245°C

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (15mm × 15mm × 5.01mm)
T_{JMAX} = 125°C, θ_{JCtop} = 11°C/W, $\theta_{JCbottom}$ = 2.5°C/W
θ_{JB} = 3°C/W, θ_{JA} = 10.4°C/W
θ VALUES DETERMINED PER JESD51-12
WEIGHT = 2.9 GRAMS

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE (Note 2)
LTM4641EY#PBF	LTM4641EY#PBF	LTM4641Y	144-Lead (15mm × 15mm × 5.01mm) BGA	–40°C to 125°C
LTM4641IY#PBF	LTM4641IY#PBF	LTM4641Y	144-Lead (15mm × 15mm × 5.01mm) BGA	–40°C to 125°C
LTM4641MPY#PBF	LTM4641MPY#PBF	LTM4641Y	144-Lead (15mm × 15mm × 5.01mm) BGA	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		38	V
V_{OUT}	Output Voltage Range	Use R_{SET1A} = R_{SET1B} ≤ 8.2kΩ. R_{fSET} Values Recommended in Table 1	●	0.6		6	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load, and Prior to UVLO	4.5V ≤ V_{IN} ≤ 38V, 0A ≤ I_{OUT} ≤ 10A V_{IN} = 4V (Ramped Down from 4.5V), I_{OUT} = 0A	● ●	1.773 1.773	1.800 1.800	1.827 1.827	V V
Input Specifications							
$V_{RUN(ON,OFF)}$	RUN On/Off Threshold	Run Rising, Turn On Run Falling, Turn Off	● ●	 0.8	1.25 1.15	2	V V
$I_{RUN(ON)}$	RUN Pull-Up Current	V_{RUN} = 0V V_{RUN} = 3.3V	● ●	–580 –220	–520 –165	–460 –110	µA µA
$I_{RUN(OFF)}$	RUN Pull-Down Current, Switching Inhibited	V_{RUN} = 3.3V, UVLO = 0V (M_{HYST} On)			1		nA
$V_{INL(UVLO)}$	V_{INL} Undervoltage Lockout	V_{INL} Rising V_{INL} Falling Hysteresis	● ● ●	 3.5 300	4.2 3.8 400	4.5 4	V V mV
$I_{INRUSH(VINH)}$	Input Inrush Current Through V_{INH}, at Start-Up	C_{SS} = Open			230		mA
$I_{Q(VINH)}$	Power Stage Bias Current (I_{VINH}) at No Load	I_{OUT} = 0A and: FCB ≥ 0.84V (Pulse-Skipping Mode) FCB ≤ 0.76V (Forced Continuous Mode) Shutdown, RUN = 0			 8 29 0.2		 mA mA mA
$I_{Q(VINL)}$	Control Bias Current (I_{VINL})	$INTV_{CC}$ Connected to DRV_{CC} and: V_{IN} = 28V, I_{OUT} = 0A V_{IN} = 28V, I_{OUT} = 10A V_{IN} = 28V, Shutdown, RUN = 0			 14.5 15.5 5		 mA mA mA
$I_{S(VINH)}$	Power Stage Input Current (I_{VINH}) at Full Load	I_{OUT} = 10A and: V_{IN} = 4.5V V_{IN} = 28V V_{IN} = 38V			 4.65 790 590		 A mA mA
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	(Note 3)	●	0		10	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	V_{IN} from 4.5V to 38V, I_{OUT} = 0A	●		0.02	0.15	%
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	I_{OUT} from 0A to 10A (Note 3)	●		0.04	0.15	%
$V_{OUT(AC)}$	Output Voltage Ripple Amplitude	I_{OUT} = 0A			16		mV_{P-P}
f_S	Output Voltage Ripple Frequency	I_{OUT} = 0A I_{OUT} = 10A			290 330		kHz kHz
$V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A			10		mV
t_{START}	V_{IN}-to-V_{OUT} Start-Up Time	RUN Electrically Open Circuit, Time Between Application of V_{IN} to V_{OUT} Becoming Regulated, OV_{PGM} = 1.5V, C_{TMR} = C_{SS} = Open			3		ms
$t_{RUN(ON-DELAY)}$	RUN-to-V_{OUT} Turn-On Response Time	V_{IN} Established, (TMR-Set POR Time Expired) Time Between RUN Releasing from GND to PGOOD Going Logic High, C_{SS} = Open, OV_{PGM} = 1.5V			175	400	µs
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load Step	I_{OUT} from 0A to 5A at 5A/µs I_{OUT} from 5A to 0A at 5A/µs			40 40		mV mV
$t_{SETTLE(LS)}$	Settling Time for Dynamic Load Step	I_{OUT} from 0A to 5A at 5A/µs I_{OUT} from 5A to 0A at 5A/µs			20 20		µs µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUT(PK)}$	Output Current Limit	5.1kΩ Pull-Up from PGOOD to 5V Source, I_{OUT} Ramped Up Until V_{OUT} Below PGOOD Lower Threshold, PGOOD Pulls Logic Low			24		A
$I_{VINH(IOUT_SHORT)}$	Power Stage Input Current During Output Short Circuit	V_{OUT} Electrically Shorted to GND			45		mA
Control Section							
V_{FB}	Differential Feedback Voltage from V_{OSNS}^+ to V_{OSNS}^-	I_{OUT} = 0A	●	591	600	609	mV
$I_{TRACK/SS}$	TRACK/SS Pull-Up Current	$V_{TRACK/SS}$ = 0V		–0.45	–1		µA
V_{FCB}	FCB Threshold			0.76	0.8	0.84	V
I_{FCB}	FCB Pin Current	V_{FCB} = 0.8V			0	±1	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			43	75	ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			220	300	ns
$V_{OSNS(DM)}$	Remote Sense Pin-Pair Differential Mode Input Range	Valid Differential V_{OSNS}^+ -to- V_{OSNS}^- Range (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)	●	0		2.7	V
$V_{OSNS(CM)}$	Remote Sense Pin-Pair Common Mode Input Range	Valid V_{OSNS}^- Common Mode Range Valid V_{OSNS}^+ Common Mode Range (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)	● ●	–0.3		 3	V V
$R_{IN(VOSNS+)}$	Input Resistance	V_{OSNS}^+ to GND		16318	16400	16482	Ω
$INTV_{CC}$, DRV_{CC}, $1V_{REF}$							
V_{INTVCC}	Internal V_{CC} Voltage	6V ≤ V_{IN} ≤ 38V, $INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V	●	5.1	5.3	5.4	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	$INTV_{CC}$ Load Regulation	RUN = 0V, $INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V and: I_{INTVCC} Varied from 0mA to –20mA I_{INTVCC} Varied from 0mA to –30mA			 –0.7 –1	 ±2 ±3	 % %
$V_{INTVCC(LOWLINE)}$	$INTV_{CC}$ Voltage at Low Line	V_{IN} = 4.5V, R_{SET1A} = R_{SET1B} = 0Ω (~0.6V_{OUT}, R_{fSET} Value Recommended in Table 1)	●	4.2	4.3		V
$DRV_{CC(UVLO)}$	DRV_{CC} Undervoltage Lockout	DRV_{CC} Rising DRV_{CC} Falling	● ●	3.9 3.2	4.05 3.35	4.2 3.5	V V
I_{DRVCC}	DRV_{CC} Current	$INTV_{CC}$ Not Connected to DRV_{CC}, DRV_{CC} = 5.3V, R_{SET1A}, R_{SET1B} and R_{SET2} Setting V_{OUT} to: 1.8V_{OUT}, R_{fSET} = 2MΩ, 0A ≤ I_{OUT} ≤ 10A 6.0V_{OUT}, R_{fSET} = Open, 0A ≤ I_{OUT} ≤ 10A (Use R_{SET1A} = R_{SET1B} ≤ 8.2k)			 11 20	 18 27	 mA mA
$V_{1VREF(DC)}$	$1V_{REF}$ DC Voltage Regulation	I_{1VREF} = 0mA I_{1VREF} = ±1mA	● ●	0.985 0.980	1.000 1.000	1.015 1.020	V V
PGOOD Output							
$V_{PGOOD(TH)}$	Power Good Window, Logic State Transition Thresholds	Ramping Differential V_{OSNS}^+ – V_{OSNS}^- Voltage: Up, PGOOD Goes Logic Low → High Up, PGOOD Goes Logic High → Low Down, PGOOD Goes Logic Low → High Down, PGOOD Goes Logic High → Low		 533 645 621 525	 556 660 644 540	 579 675 667 555	 mV mV mV mV
$V_{PGOOD(HYST)}$	Hysteresis	Differential V_{OSNS}^+ – V_{OSNS}^- Voltage Returning		8	16	24	mV
$V_{PGOOD(VOL)}$	Logic-Low Output Voltage	I_{PGOOD} = 5mA	●		75	400	mV
$t_{PGOOD(DELAY)}$	PGOOD Logic-Low Blanking Time	Delay Between Differential V_{OSNS}^+ – V_{OSNS}^- Voltage Exiting PGOOD Valid Window to PGOOD Going Logic Low (Note 4)			12		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Interrupt MOSFET Drive							
V_{VING}	Gate Drive Voltage for Power-Interrupt MOSFET, MSP	V_{IN} = 4.5V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 28V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 38V, 0A ≤ I_{OUT} ≤ 10A, V_{ING} Sourcing 1µA V_{IN} = 4V (Ramped Down from 4.5V), I_{OUT} = 0A, V_{ING} Sourcing 1µA	● ● ● ●	11.5 35 45 10.5	13.3 38.4 48.4 11.5	15.5 41 51.5 14.2	V V V V
$I_{VING(UP)}$	V_{ING} Pull-Up Current	V_{ING} Tied to V_{INGP}, and: V_{IN} = 4.5V, V_{ING} Pulled to 6.5V V_{IN} = 28V, V_{ING} Pulled to 30V	 ● ●	 350 425	 475 550	 600 675	 µA µA
$I_{VING_DOWN(CROWBAR\ ACTIVE,CROWBAR\ INACTIVE)}$	V_{ING} Pull-Down Current	V_{ING} Tied to V_{INGP}, Pulled to 33V, and: RUN Pulled to 0V (CROWBAR Inactive) OV_{PGM} Pulled to 0V (CROWBAR Active)	 ● ●	 3 24	 20 27	 30 30	 mA mA
$t_{VING(OVP_DELAY)}$	V_{ING} OVP Pull-Down Delay	OV_{PGM} Driven from 650mV to 550mV, V_{ING} Discharge Response Time	●		1.3	2.6	µs
$I_{VINGP(LEAK)}$	Zener Diode Leakage Current	V_{INGP} Driven to (V_{INH} + 10V)			1		nA
$V_{INGP(CLAMP)}$	Zener Diode Breakdown Voltage	V_{INGP}-to-V_{INH} Differential Voltage; I_{VINGP} = 5mA			15		V
Fault Pins and Functions							
V_{OVPGM}	Default Output Overvoltage Program Setting	OV_{PGM} Electrically Open Circuit	●	650	666	680	mV
$I_{OVPGM(UP)}$	OV_{PGM} Pull-Up Current	OV_{PGM} = 0V	●	–2.07	–2	–1.91	µA
$I_{OVPGM(DOWN)}$	OV_{PGM} Pull-Down Current	OV_{PGM} = 1V	●	0.945	1	1.06	µA
OVP_{TH}	Output Overvoltage Protection Inception Threshold	Ramping Up Differential V_{OSNS}^+-to-V_{OSNS}^- Voltage Until CROWBAR Outputs Logic High	●	647	666	683	mV
OVP_{ERR}	Output Overvoltage Protection Inception Error	Difference Between OVP_{TH} and V_{OVPGM} (OVP_{TH}-V_{OVPGM})	●	–12	0	12	mV
$t_{CROWBAR(OVP_DELAY)}$	CROWBAR Response Time	OVP_{GM} Driven from 650mV to 550mV	●		400	500	ns
$V_{CROWBAR(OH)}$	CROWBAR Output, Active High Voltage	OVP_{GM} Pulled to 0V and: $I_{CROWBAR}$ = –100µA, I_{INTVCC} = –20mA $I_{CROWBAR}$ = –4mA, I_{INTVCC} = –20mA	 ● ●	 4.3 4.2	 4.65 4.55	 5 4.9	 V V
$V_{CROWBAR(OL)}$	CROWBAR Output, Passive Low Voltage	$I_{CROWBAR}$ = 1µA	●		260	500	mV
$V_{CROWBAR(OVERSHOOT)}$	CROWBAR Peak Voltage Overshoot at V_{INL} Start-Up and Shutdown	V_{INL} Ramped Up from/Down to 0V	●		550	900	mV
$V_{CROWBAR(TH)}$	CROWBAR Latchoff Threshold	CROWBAR Ramped Up Until HYST Goes Logic Low	●	1.4	1.5	1.6	V
V_{TEMP}	TEMP Voltage	RUN = 0V, T_A = 25°C RUN = 0V, T_A = 125°C (See Figure 10 for Reference)		950	980 585	1010	mV mV
$OT_{TH(INCEPTION)}$	TEMP Overtemperature Inception Threshold	Ramping TEMP Downward Until HYST Outputs Logic Low	●	428	438	448	mV
$OT_{TH(RECOVER)}$	TEMP Overtemperature Recovery Threshold	Ramping TEMP Upward Until HYST Outputs Logic High	●	501	514	527	mV
$UVOV_{TH}$	UVLO/OVLO/IOVRETRY Undervoltage/Overvoltage Inception Thresholds	Ramping UVLO, OVLO or IOVRETRY Positive Until HYST Toggles Its State	●	488	500	512	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{INH} = V_{INL} = 28V, per the typical application shown in Figure 45, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{UVOVD}	UVLO/OVLO/IOVRETRY/ TEMP Response Time	±50mV Overdrive (All Pins) ±5mV Overdrive, UVLO/OVLO/IOVRETRY Pins Only (Note 4)	● 	 50	25 125	100 500	µs µs
I_{UVOV}	Input Current of UVLO, OVLO and IOVRETRY	UVLO = 0.55V or OVLO = 0.45V or IOVRETRY = 0.45V	●			±30	nA
$V_{HOUSEKEEPING(UVLO)}$	Housekeeping Circuitry UVLO	Voltage on $INTV_{CC}$, $INTV_{CC}$ Rising (Note 4) Hysteresis, $INTV_{CC}$ Returning (Note 4)	 	1.9 5	2 25	2.1 50	V mV
$V_{HYST(SWITCHING\ ON)}$	HYST Voltage (M_{HYST} Off, RUN Logic High)	RUN Electrically Open Circuit RUN = 1.8V	● ●	4.9 1.85	5.1 2.1	5.25 2.35	V V
$V_{HYST(SWITCHING\ OFF,\ RUN)}$	HYST Voltage (M_{HYST} Off, RUN Logic Low)	RUN = 0V	●	170	350	480	mV
$V_{HYST(SWITCHING\ OFF,\ FAULT)}$	HYST Voltage, Switching Action Inhibited (M_{HYST} On)	UVLO < $UVOV_{TH}$ or OVLO > $UVOV_{TH}$ or IOVRETRY > $UVOV_{TH}$ or TEMP < $OT_{TH(INCEPTION)}$ or CROWBAR > $V_{CROWBAR(TH)}$ or DRV_{CC} < $DRVCC_{UVLO(FALLING)}$ (See Figures 62, 63)	●		30	65	mV
TMR_{UOTO}	Timeout and Power-On Reset Period	C_{TMR} = 1nF, Time from Fault Clearing to HYST Being Released by Internal Circuitry	●	5	9	14	ms
$V_{LATCH(IH)}$	$\overline{LATCH}$ Clear Threshold Input High		●	1.2			V
$V_{LATCH(IL)}$	$\overline{LATCH}$ Clear Threshold Input Low		●			0.8	V
$I_{\overline{LATCH}}$	$\overline{LATCH}$ Input Current	$V_{\overline{LATCH}}$ = 7.5V	●			±1	µA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 0V	●	–1.2	–2.1	–2.8	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1.6V	●	1.2	2.1	2.8	µA
$V_{TMR(DIS)}$	Timer Disable Voltage	Referenced to $INTV_{CC}$	●	–180	–270		mV
$OTBH_{VIL}$	OTBH Low Level Input Voltage		●			0.4	V
$OTBH_{VZ}$	OTBH Pin Voltage When Left Electrically Open Circuit	–10µA ≤ I_{OTBH} ≤ 10µA	●	0.6	0.9	1.2	V
$I_{OTBH(MAX)}$	Maximum OTBH Current	OTBH Electrically Shorted to SGND	●			30	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

The LTM4641 SW absolute maximum rating of 40V is verified in ATE by regulating V_{OUT} while at $40V_{IN}$, in a controlled manner guaranteed to not affect device reliability or lifetime. Static testing of SW leakage current at $40V_{IN}$ is performed at control IC wafer level only.

Note 2: The LTM4641 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4641E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4641I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTM4641MP is tested and guaranteed over the full –55°C to 125°C operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

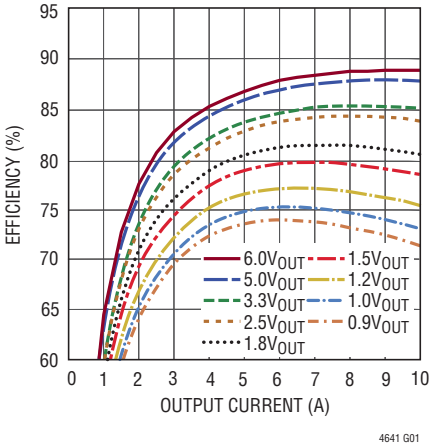
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level only.

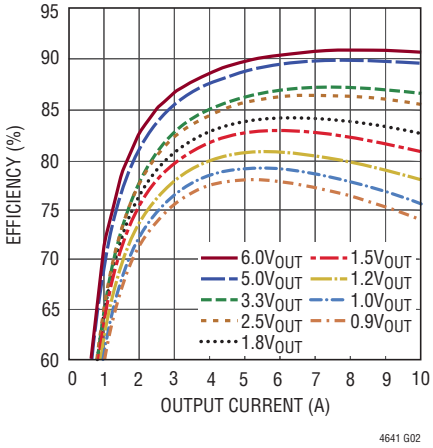
TYPICAL PERFORMANCE CHARACTERISTICS

(Figure 45 circuit with R_{fSET} per Table 1 and R_{SET1A}, R_{SET1B} and R_{SET2} per Table 2, unless otherwise noted)

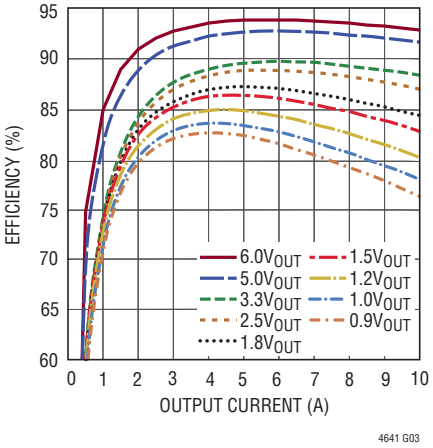
Efficiency vs Load Current at $36V_{IN}$



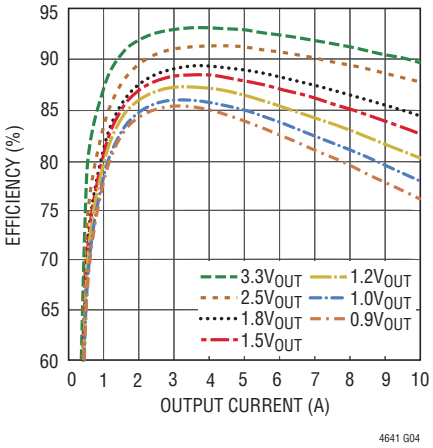
Efficiency vs Load Current at $24V_{IN}$



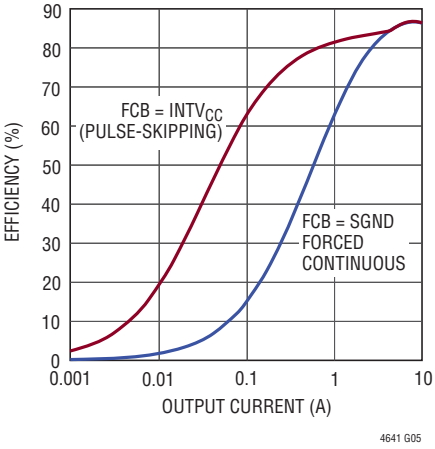
Efficiency vs Load Current at $12V_{IN}$



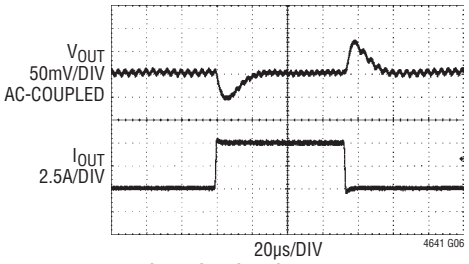
Efficiency vs Load Current at $6V_{IN}$



Pulse-Skipping vs Forced Continuous Mode Efficiency, $28V_{IN}$ to $3.3V_{OUT}$

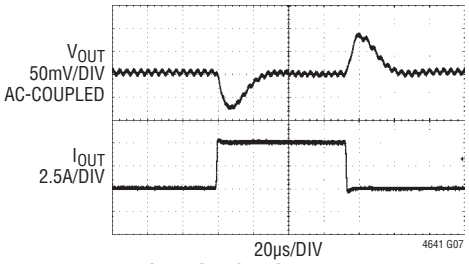


1V Transient Response, $38V_{IN}$



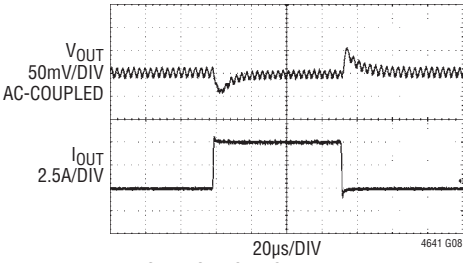
0A TO 5A LOAD STEPS AT 5A/µs
FRONT PAGE CIRCUIT WITH
OV_{PGM} = OPEN CIRCUIT

1V Transient Response, $4.5V_{IN}$



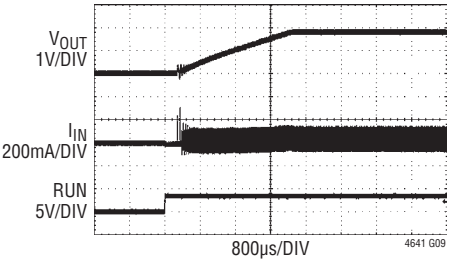
0A TO 5A LOAD STEPS AT 5A/µs
FRONT PAGE CIRCUIT WITH
OV_{PGM} = OPEN CIRCUIT

3.3V Transient Response, $28V_{IN}$ to $3.3V_{OUT}$



0A TO 5A LOAD STEPS AT 5A/µs
FIGURE 46 CIRCUIT

Output Start-Up, No Load

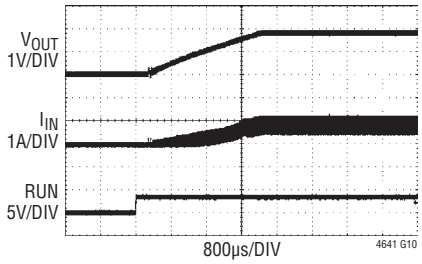


V_{IN} = 24V
$C_{IN(MLCC)} = 2 \times 10\mu F$ X7R

TYPICAL PERFORMANCE CHARACTERISTICS

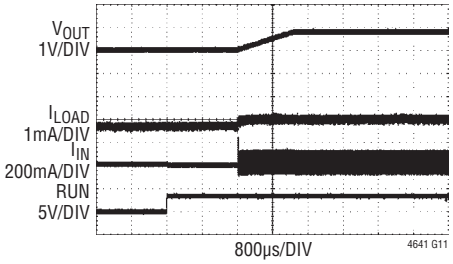
(Figure 45 circuit with R_{fSET} per Table 1 and R_{SET1A}, R_{SET1B} and R_{SET2} per Table 2, unless otherwise noted)

Output Start-Up, 10A Load



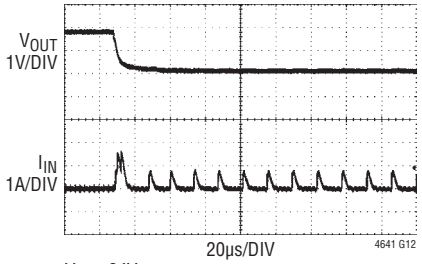
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Start-Up, Pre-Bias Condition



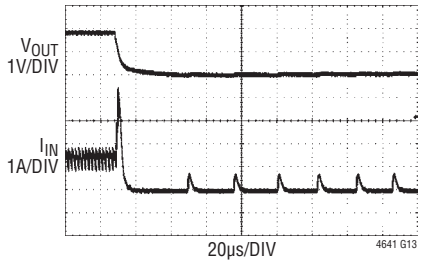
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Short-Circuit, No Initial Load



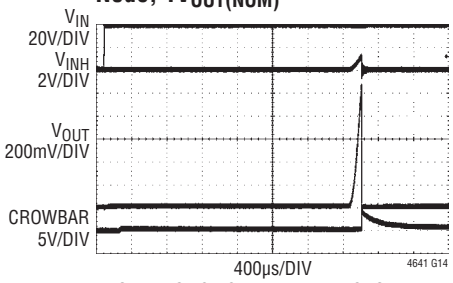
V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Output Short-Circuit, 10A Initial Load



V_{IN} = 24V
$C_{IN(MLCC)}$ = 2 × 10µF X7R

Start-Up with V_{INH} Shorted to SW Node, $1V_{OUT(NOM)}$



FRONT PAGE CIRCUIT WITH V_{INH} SHORT CIRCUITED TO SW PRIOR TO POWER-UP. APPLYING UP TO $38V_{IN}$. NO LOAD

Start-Up with V_{INH} Shorted to SW Node, $3.3V_{OUT(NOM)}$

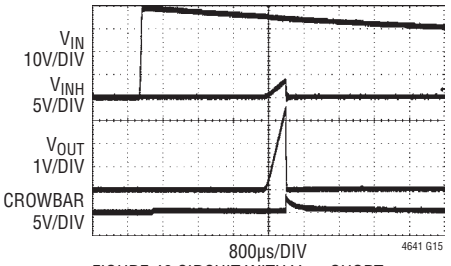


FIGURE 46 CIRCUIT WITH V_{INH} SHORT CIRCUITED TO SW PRIOR TO POWER-UP. APPLYING UP TO $38V_{IN}$. NO LOAD

Autonomous Restart with V_{INH} Shorted to SW Node, $3.3V_{OUT(NOM)}$

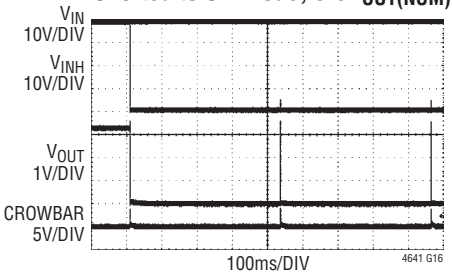
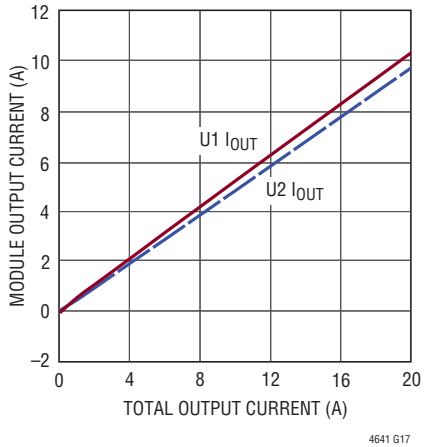
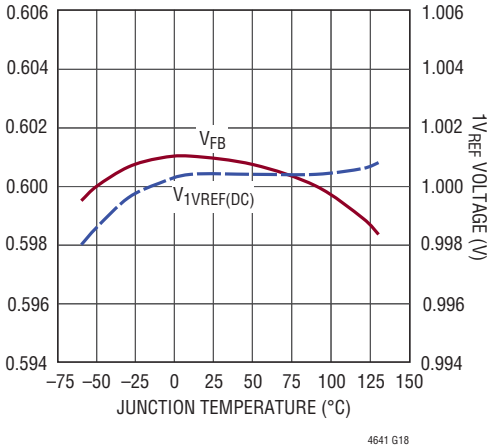


FIGURE 46 CIRCUIT, SHORT CIRCUITING V_{INH} TO SW IN SITU, OPERATING AT $38V_{IN}$ AND NO LOAD. $\overline{LATCH}$ CONNECTED TO $INTV_{CC}$ AND C_{TMR} = 47nF

Paralleled Modules, Current-Sharing Performance. cf. Figure 66 Circuit. $28V_{IN}$



Control IC Bandgap and $1V_{REF}$ Voltages vs Temperature. $28V_{IN}$



PIN FUNCTIONS

SGND (A1-A3; B1-B3; C1-C4; K1, K3; L3; M1-M3): Signal Ground Pins. This is the return ground path for all analog control and low power circuitry. SGND is tied to GND internal to the µModule regulator in a manner that promotes the best internal signal integrity—therefore, SGND should not be connected to GND in the user's PCB layout. See the Layout Checklist/Example section of the Applications Information section for more information pertaining to SGND and layout. All SGND pins are electrically connected to each other, internally.

HYST (A4): Input Undervoltage Hysteresis Programming Pin. Normally used as an output, but can be used as an input. If the LTM4641's inherent, default undervoltage lockout (UVLO) settings are satisfactory, $4.5V_{IN(RISING, MAX)}$ and $4V_{IN(FALLING, MAX)}$, HYST can be left electrically open circuit. See the Applications Information section to customize the LTM4641's UVLO thresholds.

HYST is a logic-high output with moderate pull-up strength that commands LTM4641's internal control IC to regulate the module's output voltage when conditions on the RUN, UVLO, OVLO, IOVRETRY, TEMP, CROWBAR, $INTV_{CC}$ and DRV_{CC} pins permit it (any recent latchoff events notwithstanding, otherwise OTBH and LATCH can also play a role). When a fault condition is detected, internal circuitry (M_{HYST}; see Figure 1) drives HYST logic low and the LTM4641's output is turned off. HYST can be used as a fault-indicator. See the Applications Information section.

HYST is pulled low when the RUN pin is pulled low, via an internal Schottky diode. HYST can be driven low by external open-collector/open-drain circuitry directly—as an alternate to the RUN pin interface. However, external circuitry should never drive HYST high, since doing so (indiscriminately) could cause thermal overstress to M_{HYST}, when M_{HYST} is on.

TEMP (A5): Power Stage Temperature Indicator and Overtemperature Detection Pin. When left electrically open circuit, TEMP's voltage varies according to an internal NTC (negative temperature coefficient) thermistor, residing in close proximity to LTM4641's power stage. When TEMP falls below 438mV (corresponding to a thermistor and power stage temperature of ~145°C), the LTM4641 pulls HYST low to inhibit regulation of its output voltage. HYST may be deasserted when TEMP subsequently exceeds 514mV (nominally corresponding to a cool-off hysteresis of ~10°C), depending on the OTBH setting. (See OTBH and the Applications Information section.)

To disable the µModule regulator's overtemperature shutdown feature, connect the TEMP and $1V_{REF}$ pins. The thermal shutdown inception threshold can also be modified, see the Applications Information section.

IOVRETRY (A6): Nonlatching Input Overvoltage Threshold Programming Pin. The LTM4641 pulls HYST low to inhibit regulation of its output voltage when IOVRETRY exceeds 0.5V. The LTM4641 can resume switching action when IOVRETRY is below 0.5V. If no nonlatching input overvoltage shutdown behavior is desired, connect this pin to SGND. Do not leave this pin open circuit.

GND (A7-A12; B6-B8, B11-B12; C7-C8; D6-D8; E1-E8; F1-F12; G1-G12; H3-H9, H11-H12; J5-J12; K5-K6, K11-K12; L4-L6; M4-M6): Power ground pins for input and output returns. See the Layout Checklist/Example section of the Applications Information section. All GND pins are electrically connected to each other, internally.

UVLO (B4): Input Undervoltage Lockout Programming Pin. The LTM4641 pulls HYST low to inhibit regulation of its output voltage whenever UVLO is less than 0.5V. The LTM4641 can resume switching action when UVLO exceeds 0.5V. Do not leave this pin open circuit.

If the LTM4641's default UVLO settings are used, $4.5V_{IN(RISING, MAX)}$ and $4V_{IN(FALLING, MAX)}$, then the UVLO pin should be electrically connected to $1V_{REF}$ or $INTV_{CC}$. Otherwise, see HYST and the Applications Information section for using a resistor-divider network to implement personalized UVLO rising and UVLO falling settings.

OVLO (B5): Input Overvoltage Latchoff Programming Pin. LTM4641 pulls HYST low to inhibit regulation of its output voltage when OVLO exceeds 0.5V. If OVLO subsequently falls below 0.5V, the module's output remains latched off; the LTM4641 cannot resume regulation of the output voltage until either the $\overline{LATCH}$ pin is toggled high or V_{INL} is power cycled. If input overvoltage latchoff behavior is not desired, electrically short this pin to SGND. Do not leave this pin open circuit.

PIN FUNCTIONS

CROWBAR (B9): Crowbar Output Pin. Normally logic low, with moderate pull-down strength to SGND.

When an output overvoltage (OOV) condition is detected, the LTM4641's fast OOV comparator pulls CROWBAR logic high through a series-connected internal diode. If utilizing LTM4641's OOV feature, CROWBAR should connect to the gate of a logic-level N-channel MOSFET configured to crowbar the module's output voltage (MCB, in Figure 1).

Furthermore, the LTM4641 latches off its output when CROWBAR nominally exceeds 1.5V and latches HYST logic low (see HYST).

If not using the OOV protection features of the LTM4641, leave CROWBAR electrically open circuit.

OV_{PGM} (B10): Output Overvoltage Threshold Programming Pin. The voltage on this pin sets the trip threshold for the inverting input pin of LTM4641's fast OOV comparator. When left electrically open circuit, resistors internal to the LTM4641 nominally bias OV_{PGM} to 666mV (OV_{PTH})—11% above the nominal V_{FB} feedback voltage (600mV) that the control loop strives to present to the noninverting input pin of LTM4641's fast OOV comparator. The aforementioned voltages correspond proportionally to the module's OOV inception threshold and V_{OUT}'s nominal voltage of regulation, respectively. Altering the OV_{PGM} voltage provides a means to adjust the OOV threshold; its DC-bias setpoint can be tightened with simple connections to external components (see the Applications Information section). Trace route lengths and widths to this sensitive analog node should be minimized. Minimize stray capacitance to this node unless altering the OOV threshold as described in the Applications Information section and Appendix F.

$\overline{LATCH}$ (C5): Latchoff Reset Pin. When a latchoff fault occurs, the LTM4641 turns off its output and latches M_{HYST} on to indicate a fault condition has occurred (see HYST). To configure the LTM4641 for latched off response to latchoff faults, connect $\overline{LATCH}$ to SGND. As long as $\overline{LATCH}$ is logic low, the LTM4641 will not unlatch. Regulation can be resumed by cycling V_{INL} or by toggling $\overline{LATCH}$ from logic low to high. It is also permissible to connect $\overline{LATCH}$ to $INTV_{CC}$; this configures the LTM4641 for autonomous restart with a timeout delay (programmed by C_{TMR}—see TMR).

If no latchoff faults are present when $\overline{LATCH}$ transitions from logic low to logic high, the LTM4641 immediately unlatches. If any latchoff fault is present when $\overline{LATCH}$ is logic high, a timeout delay timing requirement is imposed: the LTM4641 will not unlatch until all latchoff fault-monitoring pins meet operationally valid states for the full duration of the timeout delay. If $\overline{LATCH}$ becomes logic low before that timeout delay has expired, the LTM4641 remains latched off and the timeout delay is reset. Unlatching the LTM4641 can be reattempted by pulling $\overline{LATCH}$ logic high at a later time.

The following are latchoff fault conditions:

- CROWBAR activates (see CROWBAR)
- Input latchoff overvoltage fault (see OVLO)
- Latchoff overtemperature fault (when OTBH is logic low; see TEMP and OTBH)

$\overline{LATCH}$ is a high impedance input and must not be left electrically open circuit. $\overline{LATCH}$ can be driven by a µController in intelligent systems: a reasonable implementation for unlatching the LTM4641 is to pull $\overline{LATCH}$ logic high for the maximum anticipated timeout delay time—after which, HYST can be observed to indicate whether the LTM4641 has become unlatched.

$1V_{REF}$ (C6): Buffered 1V Reference Output Pin. Minimize capacitance on this pin, to assure the OV_{PGM} and TEMP pins are operational in a timely manner at power-up. $1V_{REF}$ should never be externally loaded except as explained in the Applications Information section.

V_{OUT} (C9-C12; D9-D12; E9-E12): Power Output Pins of the LTM4641 DC/DC Converter Power Stage. All V_{OUT} pins are electrically connected to each other, internally. Apply output load between these pins and the GND pins. It is recommended to place output decoupling capacitance directly between these pins and the GND pins. Review Table 9. See the Layout Checklist/Example section of the Applications Information section.

V_{ORB}^+ (D1): V_{OSNS}^+ Readback Pin. This pin connects to V_{OSNS}^+ internal to the µModule regulator. It is recommended to route this pin (differentially with V_{ORB}^-) to a test point so as to allow the user a way to confirm the integrity

PIN FUNCTIONS

of the remote-sense connections prior to powering up the LTM4641. V_{ORB}^+ can also be connected as a redundant feedback connection to V_{OSNS}^+ on the user's motherboard.

V_{ORB}^- (D2): V_{OSNS}^- Readback Pin. This pin connects to V_{OSNS}^- internal to the µModule regulator. It is recommended to route this pin (differentially with V_{ORB}^+) to a test point so as to allow the user a way to confirm the integrity of the remote-sense connections prior to powering up the LTM4641. V_{ORB}^- can also be connected as a redundant feedback connection to V_{OSNS}^- on the user's motherboard.

OTBH (D3): Overtemperature Behavior Programming Pin. When an overtemperature condition is detected (see TEMP), HYST pulls logic low to inhibit switching. If OTBH is connected to SGND, the LTM4641 latches HYST low. If OTBH is left floating, output voltage regulation can resume when the overtemperature event clears.

TMR (D4): Timeout Delay Timer and Power-On Reset (POR) Programming Pin. Connect a capacitor (C_{TMR}) from TMR to SGND to program the POR and timeout delay time of the LTM4641; 9ms delay time per nanofarad of capacitance. The minimum delay time is ~90µs, when TMR is left electrically open circuit. Even though they use the same capacitor, the power-on reset and timeout delay timers operate independently of each other. Any nonlatching fault or latching fault will reset the respective timer to the full delay time without impacting the other timer.

The timeout delay time programmed by a C_{TMR} capacitor can be negated by pulling TMR to $INTV_{CC}$.

RUN (D5): Run (On/Off) Control Pin. A RUN pin voltage below 0.8V will turn off the module. A voltage above 2V will command the module to turn on, if HYST is not asserted low by M_{HYST}. The LTM4641 contains a moderate (10k) pull-up resistor from HYST to $INTV_{CC}$, and a pull-up Schottky diode from RUN to HYST (see Figure 1). When RUN is pulled logic low, HYST is pulled logic low via the internal Schottky diode. RUN is compatible with direct-drive (totem-pole output drive) as well as open-collector/open-drain interfaces.

V_{OSNS}^+ (H1): Positive Input to the Remote Sense Differential Amplifier. This pin connects to the positive side of the output voltage remote sense point (V_{OUT} potential) via a resistor (R_{SET1A}). When regulating the output voltage, the LTM4641 control loop drives the differential voltage between V_{OSNS}^+ and V_{OSNS}^- to the lesser of TRACK/SS and 0.6V. V_{OSNS}^+ is connected to V_{ORB}^+ internal to the module (see V_{ORB}^+). A resistor may be needed from V_{OSNS}^+ to V_{OSNS}^- for some output voltage settings. (See the Applications Information section: Setting the Output Voltage.) Minimize stray capacitance to this pin to protect the integrity of the output voltage feedback signal.

V_{OSNS}^- (H2): Negative Input to the Remote Sense Differential Amplifier. This pin connects to the negative side of the output voltage remote sense point (GND potential) via a resistor (R_{SET1B}). When switching action is on, the LTM4641 control loop drives the differential voltage between V_{OSNS}^+ and V_{OSNS}^- to the lesser of TRACK/SS and 0.6V. V_{OSNS}^- is connected to V_{ORB}^- internal to the module (see V_{ORB}^-). A resistor may be needed from V_{OSNS}^+ to V_{OSNS}^- for some output voltage settings. (See the Applications Information section.) Minimize stray capacitance to this pin to protect the integrity of the output voltage feedback signal.

SW (H10): Switching Node of the Power Stage. Mainly used for testing purposes, however, one may optionally connect a snubber (series-configured capacitor C_{SW} and resistor R_{SW}) from SW to GND to reduce radiated EMI—in exchange for a minor compromise to power conversion efficiency. (See the Applications Information section.)

COMP (J1): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold of LTM4641's valley current mode control loop—and correspondingly, the commanded trough of the power inductor current—increases as this control voltage increases. It can be useful to make COMP available for observation on a PCB via or test pad with an oscilloscope probe. However, stray capacitance and trace lengths to this sensitive analog node should be minimized.

f_{SET} (J2): Switching Frequency Setting and Adjustment Pin. This pin interfaces directly to the I_{ON} pin of LTM4641's internal control IC. Current flow into the I_{ON} pin programs the on-time of the control loop's one-shot timer and power control MOSFET, M_{TOP}. Minimize stray capacitance and any tracelengths to this pin.

For applications requiring regulated output voltages of 3V or less at any time including during voltage rail tracking,

PIN FUNCTIONS

an on-time adjustment with a resistor to f_{SET} is required. Otherwise, f_{SET} can be left open circuit. See the Applications Information section for details.

V_{INL} (J3): Input Voltage Pin, Low Current for Power Control and Logic Bias. Feeds LTM4641's internal 5.3V LDO (see $INTV_{CC}$). Apply input voltage bias between this pin and GND. Decouple to GND with a capacitor (0.1µF to 1µF). This pin powers the heart of LTM4641's DC/DC controller and internal housekeeping ICs. V_{INL} bias current is within ~5mA of the sum of $INTV_{CC}$ and CROWBAR loading currents.

If using the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{INL} to either the drain of the external power-interrupt power MOSFET, identified on the front page schematic as MSP, or a separate input bias supply. If not making use of the advanced OOV protection features, V_{INL} and V_{INH} can connect directly to the same input power source.

LDO losses can be eliminated by connecting V_{INL}, $INTV_{CC}$, and DRV_{CC} if a low power auxiliary ~5V rail is available to power the resulting node. (See the Applications Information section, Figure 47 and Figure 49.)

DRV_{CC} (J4): Power MOSFET Driver Input Power Pin. DRV_{CC} is normally connected to $INTV_{CC}$. It must be kept within two diode drops (2 • V_{BE} or ~1.2V at 25°C) of $INTV_{CC}$. DRV_{CC} powers the internal MOSFET driver that interfaces to the switching MOSFETs (M_{TOP} and M_{BOT}) within LTM4641's power stage. It is pinned out separately from $INTV_{CC}$ to allow gate-driver current to be observed, and to allow an auxiliary ~5V to 6V bias supply to optionally provide the MOSFET driver bias current. The $INTV_{CC}$/DRV_{CC} pin pair can be biased from up to 6V (absolute maximum) from an external supply with 50mA peak sourcing capability, to reduce the LTM4641's $INTV_{CC}$ LDO losses (see Applications Information section and Figure 51). When DRV_{CC} is connected directly to $INTV_{CC}$, no bypass capacitance is needed except in rare applications where very fast output voltage ramp up is required (e.g., no soft-start capacitor on TRACK/SS, or rail-tracking rails with sub-60µs turn-on rise-time). Otherwise, ~2.2µF to 4.7µF X7R MLCC local bypassing to GND is recommended. Higher impedance sources may require higher bypass capacitance, to mitigate DRV_{CC} sag during V_{OUT} start-up.

An undervoltage lockout detector monitors DRV_{CC}. HYST is pulled low and switching action is inhibited if DRV_{CC} is less than 4.2V rising (maximum) and 3.5V falling (maximum).

FCB (K2): Forced Continuous/Pulse-Skipping Mode Operation Programming Pin. Connect this pin to SGND to force continuous mode operation of the synchronous power MOSFETs (M_{TOP} and M_{BOT}) at all output load conditions. Connect this pin to $INTV_{CC}$ to enable pulse-skipping mode operation: the freewheeling power switching MOSFET (M_{BOT}) is turned off of to prevent reverse flow of output current (I_{OUT}) at light loads. See Appendix E for more details. This is a high impedance input and must not be left electrically open circuit.

$INTV_{CC}$ (K4): Internal 5.3V LDO Output. LDO operates off of V_{INL}. The INTVCC rail biases low power control and housekeeping circuitry. $INTV_{CC}$ is usually connected to DRV_{CC} to power the MOSFET drivers interfacing to the switching power MOSFETs. No decoupling capacitance is needed on this pin unless it is being used to bias external circuitry (not common); do not apply more than 4.7µF (±20% tolerance) of external decoupling capacitance. The $INTV_{CC}$/DRV_{CC} pin pair can be overdriven by an external supply, from up to 6V (absolute maximum) with 50mA peak sourcing capability, to eliminate power losses otherwise incurred by the LTM4641's V_{INL}-to-$INTV_{CC}$ linear regulator (see the Applications Information section and Figure 51).

V_{INH} (K7-10; L7-12; M7-8, 11-12): Input Voltage Pin, High Current to the Power Converter Stage of the LTM4641. All V_{INH} pins are electrically connected to each other internally. Devote a large copper plane to connect as many of the V_{INH} pins to each other as is feasible. This will help form a low impedance electrical connection between the input source and the LTM4641's power stage. It will also provide a thermal path for removing heat from the BGA package and minimize junction temperature rise of the LTM4641 for a given application.

If utilizing the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{INH} to the source pin(s) of the external power-interrupt MOSFET, identified on the front page schematic as MSP, with a short wide trace, or preferably a small copper plane capable of adequately

PIN FUNCTIONS

handling the input current to LTM4641's power stage. *Do not* decouple the V_{INH} pins with any bypass capacitance in this case. Instead, place all decoupling capacitance directly between the drain of MSP to GND.

If not utilizing the advanced OOV protection features of the LTM4641, *do* decouple the V_{INH} pins to GND with local ceramic and bulk decoupling capacitance (see the Applications Information section).

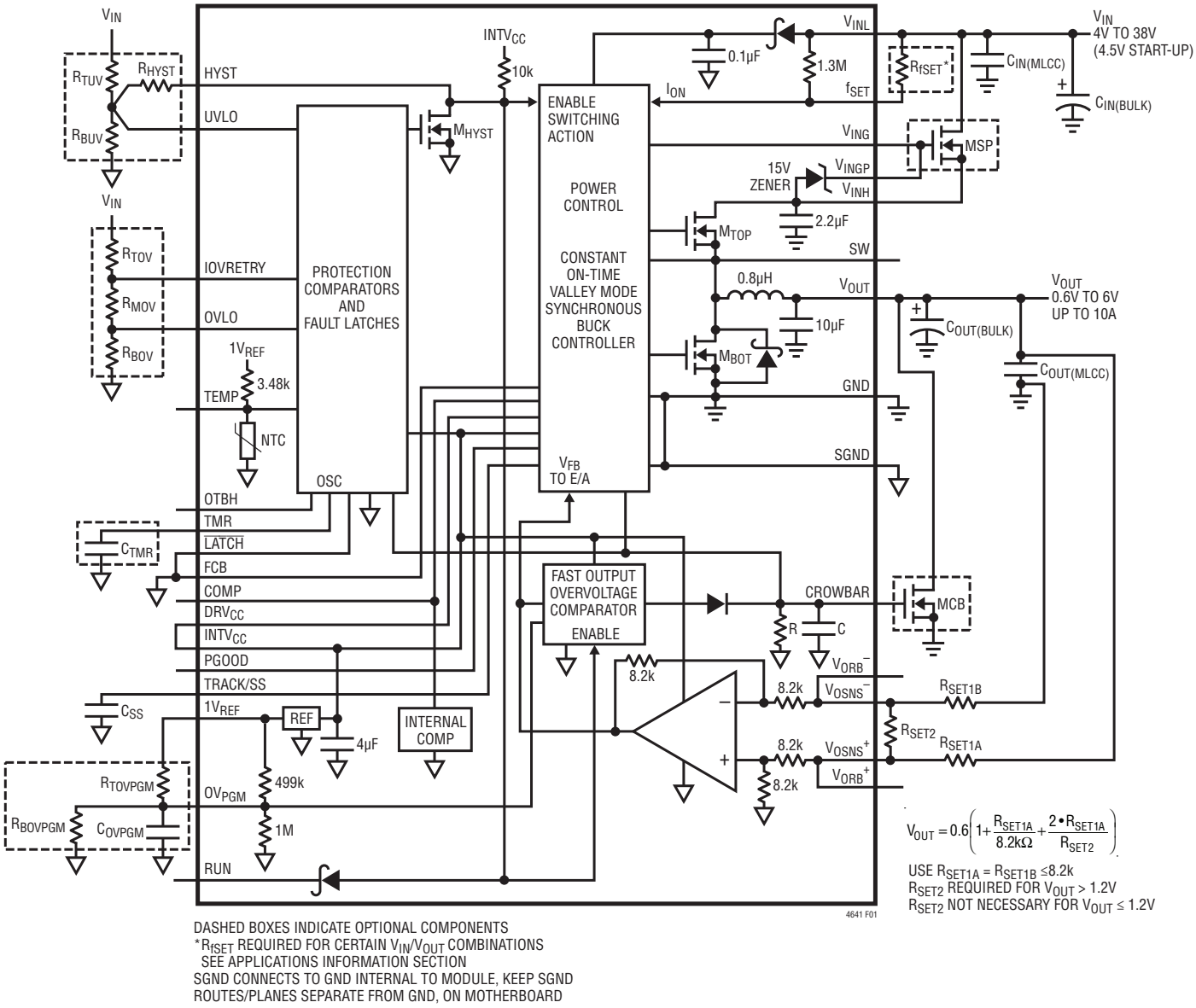
PGOOD (L1): Output Voltage Power Good Indicator. This is an open-drain logic output pin that is pulled to ground when the output voltage (and accordingly, the divided-down representation of the output voltage, V_{FB}, as presented to the control loop) is outside ±10% of the nominal target for regulation.

TRACK/SS (L2): Output Voltage Tracking and Soft-Start Programming Pin. This pin has a 1.0µA pull-up current source, typical. A capacitor can be placed from this pin to SGND to obtain an output voltage soft-start ramp-up rate whose turn-on time is 0.6ms per nanofarad of capacitance. Alternatively, when a voltage is applied to TRACK/SS through a resistor-divider network from another rail, the LTM4641 output is able to track the external voltage to satisfy coincident and ratiometric rail-voltage sequencing requirements. See the Applications Information section.

V_{ING} (M9): Gate Drive Output Pin. If utilizing the advanced output overvoltage (OOV) protection features of the LTM4641, connect V_{ING} to V_{INGP} and to the gate of the external power-interrupt N-channel MOSFET feeding V_{INH}, identified on the front page schematic as MSP; otherwise, leave this pin electrically open circuit.

V_{INGP} (M10): Gate Drive Protection Pin. If utilizing the advanced OOV protection features of the LTM4641, connect V_{INGP} to V_{ING} and to the gate of the external power-interrupt N-channel MOSFET feeding V_{INH}, MSP; otherwise, leave this pin electrically open circuit.

SIMPLIFIED BLOCK DIAGRAM



DASHED BOXES INDICATE OPTIONAL COMPONENTS
*R_{fSET} REQUIRED FOR CERTAIN V_{IN}/V_{OUT} COMBINATIONS
SEE APPLICATIONS INFORMATION SECTION
SGND CONNECTS TO GND INTERNAL TO MODULE, KEEP SGND ROUTES/PLANES SEPARATE FROM GND, ON MOTHERBOARD

Figure 1. Simplified Block Diagram. cf. Functional Block Diagram in Appendix A, Figure 62

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN(MLCC)}$ + $C_{IN(BULK)}$	External Input Capacitor Requirement	I_{OUT} = 10A, 2 × 10µF or 4 × 4.7µF		20		µF
$C_{OUT(MLCC)}$ + $C_{OUT(BULK)}$	External Output Capacitor Requirement	I_{OUT} = 10A, 3 × 100µF or 6 × 47µF		300		µF

OPERATION

Introduction

The LTM4641 contains a buck-topology regulator employing a constant on-time current mode control scheme, including built-in power MOSFET devices with fast switching speed and a power inductor. In its most basic configuration (see Figure 45), the module operates as a standalone nonisolated switching mode DC/DC step-down power supply. It can provide up to 10A of output current with a few external input and output capacitors and output feedback resistors. The supported output voltage range is from 0.6V DC to 6V DC. The supported input voltage range is 4V to 38V, with a maximum start-up voltage of 4.5V (over temperature). Power conversion from lower input voltages can be realized if an auxiliary bias supply is available to power LTM4641's control and housekeeping bias input pin, V_{INL}. The LTM4641 Simplified Block Diagram is found in Figure 1. For a more detailed look, the Functional Block Diagram is found in Appendix A, Figure 62.

Motivation

Pulsed loading conditions and abnormal disturbances within the electrical systems found in industrial, vehicle, aeronautic, and military applications can induce wildly varying voltage transients (surges) on what is nominally a 24V DC to 28V DC distributed bus (28V DC bus). The duration of such disturbances can extend for periods of time between a millisecond to a minute in length, with excursions sometimes reaching (or exceeding) 40V and falling below 6V.

While switching buck regulators are of universal interest due to their compact size and ability to deliver DC/DC power conversion at high efficiency, FMEA (failure modes and effects analysis) leads one to believe that there is no way to reduce the severity rating and effects of an electrical short from the input source to the output load—however improbable. The LTM4641 challenges this notion by protecting the load from seeing excessive voltage stress, even when its high side switching MOSFET is short circuited.

Power µModule Regulator Reliability

First and foremost, Linear Technology µModule products adhere to rigorous testing and high reliability control, fabrication, and manufacturing processes—as is required of all its products. Furthermore, as part of its commitment to excellence, the Linear Technology Quality Control program periodically updates its Reliability Data report for LTM4600 series products to include cumulative data obtained from ongoing and routine in-house testing relating to operational life, highly accelerated stress, power and temperature cycling, thermal and mechanical shock, and much more. To view the latest report visit http://www.linear.com/docs/13557.

The LTM4641 easily supports high step-down ratios with few external components. The additional protection features when implemented provide an extra degree of insurance beyond other µModule regulators.

Overview

When configured as shown in Figure 46, the LTM4641 can regulate an output voltage between 0.6V and 6V from an input voltage between 4V and 38V ($4.5V_{IN}$ start-up, maximum).

If an optional N-channel power MOSFET, MSP, is placed between the input power source (V_{IN}) and the power stage input pins (V_{INH}), MSP's role becomes that of a resettable electronic power-interrupt switch. The gate of MSP is operated by V_{ING}, and its gate-to-source voltage is assured to be clamped by a built-in 15V Zener diode accessed via V_{INGP}. When switching action is engaged, V_{ING} charges the gate of MSP to nominally 10V above V_{INH} potential—suitable for driving a standard-logic MOSFET—and MSP becomes enhanced to pull V_{INH} up to the input source supply's electrical potential. The switching regulator steps down V_{INH} potential to V_{OUT} when MSP is on. When switching action is inhibited by pulling the RUN pin low or when a fault condition is detected by LTM4641's internal circuitry—such as an output overvoltage (OOV) condition—the gate of MSP is discharged and MSP turns off. The input source supply is thus disconnected from LTM4641's power stage input (V_{INH}).

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

The operation of MSP as a power interrupter provides a critical element of robust OOV protection: it removes a means for input power to flow through a damaged power stage to any precious loads on the output voltage rail, even when input power is cycled.

For even greater resilience to a short-circuit between V_{INH} and the SW switching node of the power stage, an external logic-level N-channel power MOSFET, MCB, is optionally placed—in a crowbar configuration—on the output of the power module. When an OOV condition is detected, CROWBAR turns on MCB (within 500ns, maximum) to discharge the output capacitors and transform any residual energy in LTM4641's power stage into a trivial amount of heat—energy which would otherwise have only served to inject charge into (further pump up the voltage on) the output capacitors, where precious loads reside.

The control and monitoring circuitry within the LTM4641 power module provide the following:

- Fast, accurate, latching output overvoltage detector (<500ns response time, <±12mv threshold error)
- N-channel output overvoltage crowbar power MOSFET drive
- Accurate (<±2.4%) nonlatching and resettable latching input overvoltage shutdown thresholds
- N-channel overvoltage power-interrupt MOSFET drive
- Accurate (<±2.4%) Input UVLO rising and UVLO falling thresholds
- Built-in and adjustable overtemperature shutdown protection, programmable for resettable latching or nonlatching (hysteretic restart) response
- Analog temperature indicator output pin
- Adjustable power-on reset and timeout delay time
- Latchoff behavior that can be altered to instead provide autonomous restart after timeout delay time expires
- Parallelable for higher output power
- Differential remote sensing of POL voltage
- Internal loop compensation
- Output current foldback protection
- Selectable pulse-skipping mode operation
- Output voltage soft-start and rail tracking
- Power-up into pre-biased conditions without sinking current from the output capacitors
- Adjustable switching frequency
- Power good indicator
- RUN enable pin

Novel and simple circuit implementations with LTM4641 and a few external components enable surge ride-through protection and overtemperature detection of a power-interrupt MOSFET. (See Figure 47, for example.) The aforementioned features enabled by LTM4641 are grouped by function and described in the remainder of the Applications Information section.

Power (V_{INH}) and Bias (V_{INL}) Input Pins

LTM4641's power stage (V_{INH}) and control bias (V_{INL}) input pins are brought out separately to allow freedom for implementing more sophisticated system configurations, such as: fully utilizing LTM4641's advanced output overvoltage (OOV) protection features to protect the load (e.g., front page schematic or Figure 46); providing rudimentary input surge ride-through protection (Figure 47); performing DC/DC down conversion from a power rail below LTM4641's inherent UVLO thresholds (from a 3.3V bus in Figure 49).

If V_{INH} and V_{INL} are powered from separate rails, it is recommended to power up V_{INL} prior to or concurrently with V_{INH}. V_{INL} should have a final value of at minimum 3.5V within 2ms of V_{INH} exceeding 3.5V. The recommendation to sequence V_{INL} ahead of or closely with V_{INH} is not related at all to module device reliability but stems rather from a desire to assure that the control section of LTM4641 drives the MOSFETs in LTM4641's power stage deterministically whenever any appreciable V_{INH} voltage is present. It is always permissible for V_{INL} voltage to be present—regardless of the state of V_{INH}—however, realize that there is no UVLO detection on V_{INH}.

To prevent the control section from trying to regulate through a dropout condition or commencing switching activity in the absence of V_{INH} potential, it is recommended

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

to implement a custom UVLO falling setting above the dropout curve in Figure 4 (see also Figure 11).

LT3010-5 is shown in Figure 47 to provide bias for V_{INL}, to enable ride-through of 80V transients on V_{IN}. UVLO detection of V_{IN} is realized in this example by D2 creating a discharge path for V_{INL} in the event of loss of V_{IN}.

V_{INH} and V_{INL} have no specific power-down sequencing requirement, only that V_{INL} should stay above 3.5V whenever V_{INH} is above 3.5V.

V_{INL} and V_{INH} sequencing is inherently addressed by the LTM4641 in the Figure 45 and Figure 46 circuits.

The V_{IN} and V_{INL} start-up and shutdown waveforms of the Figure 47 circuit—but with 1Ω output load and TMR tied to $INTV_{CC}$—are shown in Figure 2. The effect of the timing capacitor, C_{TMR}, that normally generates a power-on reset (POR) delay at start-up is negated by tying TMR to $INTV_{CC}$. The ~3ms V_{IN}-to-V_{OUT} start-up delay time seen in Figure 2 is due to POR of the LTM4641's fault-monitoring circuitry and soft-start ramp (C_{SS}).

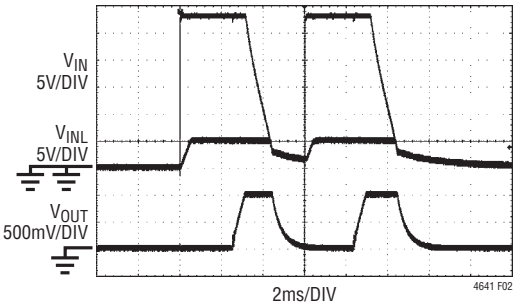


Figure 2. Start-Up and Shutdown Waveforms of Figure 47 Circuit. TMR Tied to $INTV_{CC}$ to Highlight V_{IN} and V_{INL} Sequencing without POR Delay. 1Ω Load

Switching Frequency (On Time) Selection and Voltage Dropout Criteria (Achievable V_{IN}-to-V_{OUT} Step-Down Ratios)

The LTM4641 controller employs a current mode constant on-time architecture, in which the COMP voltage corresponds to the trough inductor current at which the internal high side power MOSFET (M_{TOP}) is commanded on by the control loop—for a duration of time proportional to controller's I_{ON} pin current (Refer to Figure 1). Regulation is maintained by a pulsed frequency modulation (PFM) scheme. During a load transient step-up, the control loop will command a higher inductor trough current to compensate for a deficiency in output voltage; the effective switching frequency will increase until the output voltage returns to normal (an overcurrent event, notwithstanding). During a load transient step-down, the control loop will command a lower inductor trough current to compensate for an excess of output voltage; the effective switching frequency will decrease until the output voltage returns to normal. The control loop perceives inductor current-sense information via the voltage signal that appears across the synchronous power MOSFET, M_{BOT}, when M_{BOT} is on (this is commonly referred to in the industry as $R_{DS(ON)}$ current sensing).

The on-time of the one-shot timer—and hence the power control MOSFET, M_{TOP},—is given, in units of seconds, by:

$$t_{ON} = \frac{0.7V \bullet 10pF}{I_{ION}} \quad (1)$$

where I_{ION} is in units of amperes. For output voltages greater than 3V, and for non-rail-tracking applications, no external R_{fSET} resistor is needed, and the I_{ION} current (units: amperes) is set solely by the V_{INL} voltage (units: volts) and the internal 1.3MΩ V_{INL}-to-f_{SET} resistor:

$$I_{ION} = \frac{V_{INL}}{1.3M\Omega} \quad (2)$$

The switching frequency of operation of the LTM4641's buck converter power stage at full load in this scenario is given, in Hz, by:

$$f_{SW} = \frac{V_{OUT}}{0.7V \bullet 1.3M\Omega \bullet 10pF} \quad (3)$$

where V_{OUT} is the desired nominal output voltage, in units of volts.

An external R_{fSET} resistor can be applied when setting V_{OUT} greater than 3V, if desired, to obtain increased switching frequency. Usually, increasing switching frequency comes from a desire to reduce output voltage ripple and/or output capacitance requirement—but at a moderate penalty to DC/DC conversion efficiency. There are some limitations to how low an R_{fSET} value can be applied in practice due

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

to non-zero minimum off-time, dropout voltage, and maximum achievable switching frequency of operation.

When an R_{fSET} resistor external to the LTM4641 is connected between V_{INL} and f_{SET} to decrease the default on-time setting, the total I_{ON} current (units: amperes) is given by:

$$I_{ION} = \frac{V_{INL}}{1.3M\Omega} + \frac{V_{INL}}{R_{fSET}} = \frac{V_{INL}}{1.3M\Omega \,||\, R_{fSET}} \quad (4)$$

where V_{INL} is in units of volts and R_{fSET} is in units of ohms. R_{fSET} is needed for output voltage settings less than or equal to $3V_{OUT}$, and for rail-tracking applications.

The minimum on-time the LTM4641 supports is 43ns, typical, but guard banded conservatively to 75ns, maximum. Therefore, for a conservative design, t_{ON} should be larger than 75ns, typical. From Equation 1, it follows that I_{ION} should be designed to be less than 93.3µA.

When an external R_{fSET} resistor is applied between V_{INL} and R_{fSET} (and V_{INL} and V_{INH} are operating from the same rail—Figure 45 and Figure 46), the switching frequency of operation of the power stage at full load, in Hz, is given by:

$$f_{SW} = \frac{V_{OUT}}{0.7V \bullet (1.3M\Omega \,||\, R_{fSET}) \bullet 10pF} \quad (5)$$

where R_{fSET} is in ohms, and V_{OUT} is the desired nominal output voltage, in units of volts.

In the general case, the switching frequency of the buck converter power stage at full load is given, in Hz, by:

$$f_{SW} = \frac{V_{OUT}}{V_{INH} \bullet t_{ON}} = \frac{V_{OUT} \bullet I_{ION}}{V_{INH} \bullet 0.7V \bullet 10pF} \quad (6)$$

See Appendix C for a detailed discussion on the following topics:

- Why should the switching controller be operated at a higher switching frequency (i.e., programmed for a shorter on-time with R_{fSET}) than that yielded by the internal 1.3MΩ V_{INL}-to-f_{SET} resistor alone…

  …for nominal output voltages of 3V and less?

  …in rail-tracking applications?

- When V_{INL} and V_{INH} are operated from separate supplies…

  … why should R_{fSET} ordinarily connect to the V_{IN} power source rather than V_{INH} (Figure 49)?

  …when is it okay for R_{fSET} to connect to V_{INH} (Figure 47)?

For application circuits of the form found in Figure 45, Figure 46, Figure 47 and Figure 51: see Figure 3 for the maximum recommended value of R_{fSET} as a function of nominal target output voltage, and resulting full-load switching frequency corresponding to those R_{fSET} values.

Figure 3 can also be interpreted to provide the lowest recommended switching frequency for a given target output voltage. Table 1 summarizes nominal values of R_{fSET} endorsed for some popular output voltages; use of commonly available ±5% tolerance resistors or better with ±100ppm/°C temperature coefficient or better is recommended.

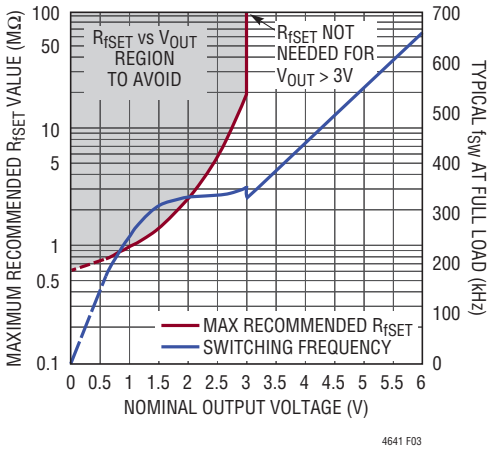


Figure 3. Maximum Recommended R_{fSET} (Nominal Values) for Non-Tracking Applications, and Resulting Full-Load Operating Switching Frequency vs Nominal Output Voltage

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

Table 1. Endorsed R_{fSET} Resistor Value vs Output Voltage for Non-Tracking Applications—and Resulting Full-Load Switching Frequency (cf. Figure 45, Figure 46, Figure 47, and Figure 51 Circuits)

$V_{OUT(NOM)}$ (V)	R_{fSET} (MΩ) (Nearest EIA-Standard Values)	f_{SW} (kHz)
0.6	0.787	175
0.7	0.825	200
0.8	0.887	215
0.9	0.931	235
1.0	1.00	255
1.2	1.13	285
1.5	1.43	315
1.8	2.00	325
2.0	2.55	330
2.5	5.76	335
Greater Than 3.0	∞ (Not Used)	See Figure 2
3.3	∞ (Not Used)	360
5.0	∞ (Not Used)	550
6.0	∞ (Not Used)	660

In rail-tracking applications, it is recommended to use the R_{fSET} value corresponding to the lowest voltage needed to be regulated during output voltage ramp down. For example: to ramp V_{OUT} down to 0.5V requires R_{fSET} to be not more than 750kΩ (nominal) per Figure 3.

It is often permissible to use lower R_{fSET} values than those indicated in Figure 3 and Table 1 if, for example, lower output ripple voltage and/or a lower output capacitance is desired. However, be aware of three guiding principles:

I. Minimum On-Time. Ensure $I_{ION} < 93.3\mu A$. See Equations 1 and 4.

II. Minimum Off-Time and Dropout Operation. The minimum off-time, $t_{OFF(MIN)}$, is the shortest time required for the LTM4641 to perform the following tasks: turn on its power synchronous MOSFET (M_{BOT}), trip the control loop's current comparator, and turn off M_{BOT}. The minimum input voltage on V_{INH}, in volts, that one can regulate the output at and still avoid dropout is given by:

$$V_{IN(DROPOUT)} = V_{OUT} \bullet \left(1 + \frac{t_{OFF(MIN)}}{t_{ON}}\right) + R_{PS} \bullet I_{OUT} \quad (7)$$

where:

- V_{OUT} is nominal output voltage in volts.
- $t_{OFF(MIN)}$ is the minimum length of time M_{BOT} can be on, after M_{TOP} turns off. For a conservative design, use a value of 300ns, taken from the Electrical Characteristics Table.
- t_{ON} is the on-time of the power control MOSFET, M_{TOP}, as programmed by the current flowing into the I_{ON} pin of LTM4641's internal control IC.
- R_{PS} is the series resistance of the module's power stage, from V_{INH} to V_{OUT}. For $V_{IN} \geq 6V$, this is less than 50mΩ, even at extreme temperatures ($T_J \approx 125°C$). For $V_{IN} < 6V$, the effective series resistance increases due to drop in $INTV_{CC}$ voltage and corresponding decreased gate-drive enhancement of M_{TOP}. Printed circuit board (PCB) and/or cable resistance present in the copper planes and/or wires that physically connect the output of the module to the load adds to R_{PS}'s effective value.
- I_{OUT} is the load current on V_{OUT} in amperes.

For applications of the form shown in Figure 45, Figure 46 and Figure 47: the minimum allowable V_{INH} voltage of operation to avoid dropout for $3V < V_{OUT} \leq 6V$ is shown in Figure 4. The curves are a result of realizing that $V_{IN(DROPOUT)}$ equals V_{INH} (neglecting MSP voltage drop) when dropout actually occurs, and that Equations 1 and 2 yield an expression for t_{ON} as a function of V_{INH}. M_{TOP} will be less fully enhanced during its on-time if DRV_{CC} is less than its nominal value of 5.3V (for example, when $V_{INL} < 6V$ and when DRV_{CC} bias is provided by $INTV_{CC}$). DRV_{CC}'s effect on R_{PS} at low line is illustrated in Figure 4.

III. Maximum Attainable f_{SW}. The maximum attainable switching frequency of operation (in units of Hz) for a given on-time (t_{ON}, in seconds) is governed simply by:

$$f_{MAX} = \frac{1}{t_{ON} + t_{OFF(MIN)}} \quad (8)$$

where a conservative value of 300ns can be used for $t_{OFF(MIN)}$.

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

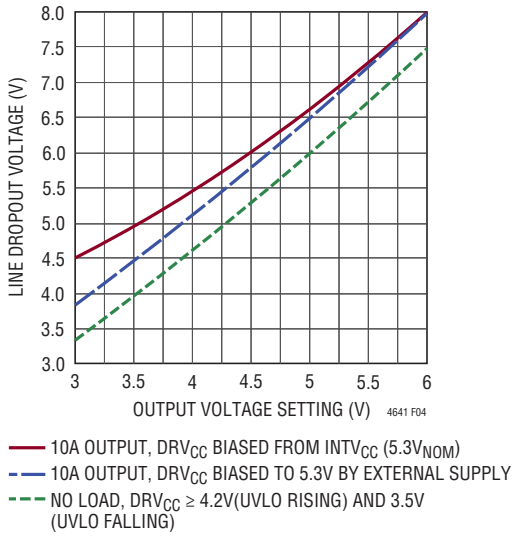


Figure 4. Line Dropout Voltage vs Output Voltage at No Load and Full Load. Figure 45, Figure 46 and Figure 47 Circuit Applications. R_{fSET} = Open and R_{SET1A}, R_{SET1B}, R_{SET2} Values Setting V_{OUT} for Regulation at or Above 3V

Given that the PFM control scheme increases switching frequency (to as high as f_{MAX}) to maintain regulation during a transient load step-up, the design guidance is: set the steady-state operating frequency f_{SW} to be less than f_{MAX}. Furthermore, when the LTM4641 is in dropout operation, the switching frequency of the converter *is* f_{MAX}.

It is best to avoid operation in dropout scenarios, because the control loop will rail COMP high to command M_{TOP} at highest possible duty cycle. If input voltage "snaps upwards" at a sufficiently high slew rate when COMP has railed, the control loop may be unable provide satisfactory line rejection.

See Figure 11 to set the UVLO falling response of LTM4641 above the computed $V_{IN(DROPOUT)}$ voltage; this will inhibit switching action for $V_{IN} < V_{IN(DROPOUT)}$. Input voltage ripple, and any line sag between the input source supply and the V_{INH} pins—and voltage drop across the power interrupt MOSFET, MSP, if used—must be taken into account by the system designer.

Setting the Output Voltage; the Differential Remote Sense Amplifier

A built-in differential remote-sense amplifier enables precision regulation at the point-of-load (POL), compensating for any voltage drops in the system's output distribution path: the total variation of LTM4641's output DC voltage over line, load, and temperature is better than ±1.5%.

The basic feedback connection between the POL and the module's feedback sense pins is shown in Figure 5.

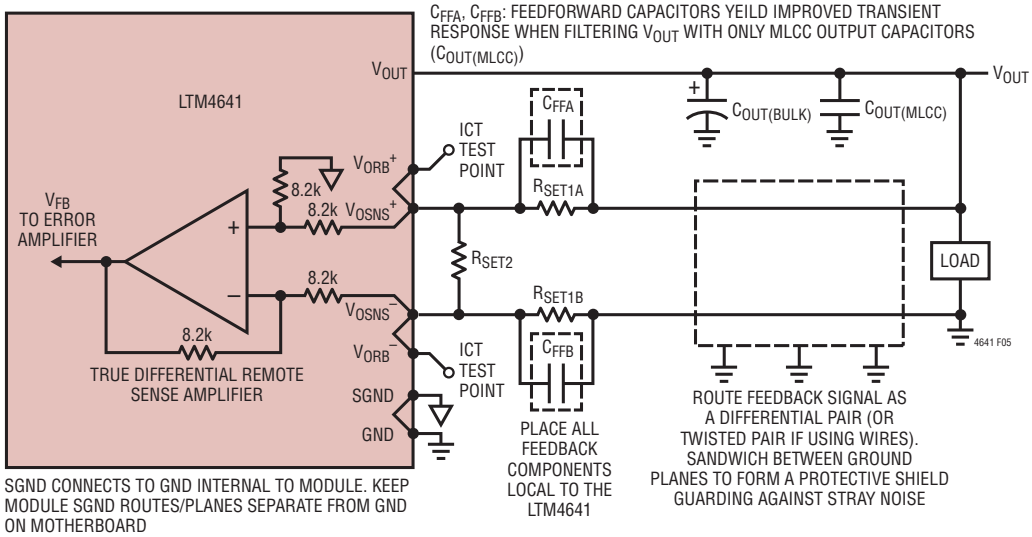


Figure 5. Basic Feedback Remote Sense Connections and Techniques; Setting the Output Voltage

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

The output voltage at the POL is differentially sensed via a symmetrical impedance-divider network. In Figure 1 and Figure 5, it is seen that the control loop regulates the output voltage such that the differential V_{OSNS}^+-to-V_{OSNS}^- feedback signal voltage is the lesser of the TRACK/SS pin voltage or the regulator's nominal bandgap voltage of 600mV. The arrangement and values of the resistors in the symmetrical impedance-divider network set the output voltage.

The remote sense pins (V_{OSNS}^+, V_{OSNS}^-) have redundant connections internal to the module to readback pins (V_{ORB}^+, V_{ORB}^-). The readback pins provide a means to verify the integrity of the feedback signal connection during motherboard ICT (in circuit test). The importance of verifying the integrity of the connection of the feedback signal to the output voltage prior to powering up the input voltage cannot be understated. If one or both feedback pins are left electrically floating due to manufacturing assembly defect, for example, or if the remote-sense pins are short circuited to each other, the control loop and overvoltage-detector circuitry have no awareness of the actual output voltage condition. A compromised feedback connection presents a very real danger of (1) the control loop commanding on M_{TOP} at the highest possible duty cycle—due to the lack of negative feedback—and (2) the LTM4641's protection circuitry being unaware of any issue. In a production environment, modern day ICT can easily catch any such stuffing or assembly errors; in a lab or prototyping environment, an ohmmeter can do the job.

For many applications that use a mixture of MLCC and bulk (low ESR tantalum or polymer) output capacitors, the symmetrical impedance-divider network that feeds back the POL's voltage to the module need only be constructed with resistors R_{SET1A} and R_{SET1B}, for output voltages of $1.2V_{OUT}$ and lower. R_{SET2} must be present for output voltages in excess of $1.2V_{OUT}$. R_{SET1A} and R_{SET1B} should always have the same nominal value. Applications with MLCC-only output capacitors (see Output Capacitors and Loop Stability in following pages) will demonstrate improved transient response when feedforward capacitors C_{FFA} and C_{FFB}, nominally equal in value, are installed electrically in parallel with R_{SET1A} and R_{SET1B}, respectively.

Use of 0.1% tolerance resistors (or better) for R_{SET1A}, R_{SET1B}, and R_{SET2} are recommended—with temperature coefficients of resistance suitable for one's operating range of PCB temperature—to assure that output voltage error introduced by resistor value variation is acceptable for the application. SMT resistors with T.C.R.s of ±25ppm/°C and better are readily available in the marketplace.

For output voltage settings less than or equal to $1.2V_{OUT}$, R_{SET2} is not needed, and R_{SET1A} and R_{SET1B} are given by:

$$R_{SET1A} = R_{SET1B} = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet 8.2k\Omega \quad (9)$$

For output voltages above $1.2V_{OUT}$, R_{SET1A} (and R_{SET1B}) should be set equal to 8.2kΩ (or less, if 8.2kΩ is not a convenient value for the user), and R_{SET2} is then given by:

$$R_{SET2} = \frac{2 \bullet R_{SET1A}}{\frac{V_{OUT}}{0.6} - \frac{R_{SET1A}}{8.2k\Omega} - 1} \quad (10)$$

It is always permissible to select a value for R_{SET1A} (and R_{SET1B}) less than that given by Equation 9—and then calculate a valid value for R_{SET2} from Equation 10—as long as R_{SET1A} and R_{SET1B} are designed to withstand the higher resulting power dissipation.

When V_{OUT} is in regulation, the voltages at V_{OSNS}^+ and V_{OSNS}^- are given by:

$$V_{VOSNS}^+ = \left(\frac{0.6V}{(8.2k\Omega \,||\, R_{SET1A} \,||\, R_{SET2})} + \frac{\Delta V_{GND}}{R_{SET1A}}\right) \bullet (R_{SET1A} \,||\, 16.4k\Omega) \quad (11)$$

and

$$V_{VOSNS}^- = V_{VOSNS}^+ - 0.6V \quad (12)$$

respectively. ΔV_{GND} is the voltage drop between ground at the POL and LTM4641's SGND pins in volts. This voltage drop is usually entirely a result of I • R drop in the output distribution path—largest when maximum load current is being drawn:

$$\Delta V_{GND} = V_{GND(POL)} - V_{SGND(LTM4641)} \quad (13)$$

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

With R_{SET1A}, R_{SET1B}, and R_{SET2} determined, double-check the output voltage setting with:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_{SET1A}}{8.2k\Omega} + \frac{2 \bullet R_{SET1A}}{R_{SET2}}\right) \quad (14)$$

Some recommended values for R_{SET1A}, R_{SET1B}, and R_{SET2} for popular output voltages are shown in Table 2.

Table 2. Recommended R_{SET1A}, R_{SET1B} and R_{SET2} Values for Some Popular Output Voltages, cf. Figure 5 Feedback Connections.

V_{OUT}	R_{SET1A}, R_{SET1B}	R_{SET2}
0.6V	0Ω	∞ (Not Used)
0.7V	1.37kΩ	∞ (Not Used)
0.8V	2.74kΩ	∞ (Not Used)
0.9V	4.12kΩ	∞ (Not Used)
1.0V	5.49kΩ	∞ (Not Used)
1.2V	8.2kΩ	∞ (Not Used)
1.5V	8.2kΩ	33.2kΩ
1.8V	8.2kΩ	16.5kΩ
2.0V	8.2kΩ	12.4kΩ
2.5V	8.2kΩ	7.5kΩ
3.3V	8.2kΩ	4.7kΩ
5.0V	8.2kΩ	2.61kΩ
6.0V	8.2kΩ	2.05kΩ

See Appendix D for a detailed discussion on the following topics:

- What is the rationale for using a symmetrical resistor network?
- What should I do if I cannot shield the differential sense feedback lines with GND? (I anticipate differential mode noise in the feedback signal?)
- What should I do if the module and the load(s) are separated by a significant distance (~50cm or more), or if the load current flows through a cable assembly or power connector? (I anticipate common mode noise in the feedback signal?)

Input Capacitors

The LTM4641 module should be connected to a low AC impedance, nominally DC output voltage source. MLCC input bypass capacitors must be provided externally, as close in proximity to the module as possible (see Figure 43). If external MOSFET MSP is not used (Figure 45), two 10µF or four 4.7µF ceramic capacitors should be electrically connected directly between the V_{INH} and GND pins. If MSP is used (Figure 46, Figure 47 and Figure 49), then MSP must be placed as close to the LTM4641's V_{INH} pins as possible, and two 10µF or four 4.7µF ceramic capacitors should be electrically connected directly between the drain of MSP and GND (see Figure 44). A 47µF to 100µF surface mount bulk capacitor can be used to supplement input power bypassing, and can share the burden of any local ceramic capacitors in filtering the power stage's ripple current. If low impedance power planes are used to bring V_{IN} to the vicinity of the module, input source impedance will be low enough that bulk capacitors will not be needed. A localized bulk input capacitor is needed when an underdamped LC-resonant tank is formed by routing long input leads or traces (low ESR inductance) bypassed only with MLCCs (ultralow ESR capacitance).

Neglecting the inductor peak-to-peak current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \bullet \sqrt{D \bullet (1-D)} \quad (15)$$

where η is the power conversion efficiency of the LTM4641 module and D is the duty cycle on-time of M_{TOP}. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a polymer capacitor.

For a buck converter, the switching duty cycle of M_{TOP} can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (16)$$

Output Capacitors and Loop Stability/Loop Compensation

The current mode constant on-time architecture enables very high step-down input-to-output ratios with compelling transient response. It also enables cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. The LTM4641 is internally compensated to yield stability over all operating conditions.

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

The output capacitors $C_{OUT(BULK)}$ and $C_{OUT(MLCC)}$ must be chosen with low enough effective series resistance (ESR) to meet the output voltage ripple requirements and provide localized bypassing for the load. Although the LTM4641 provides fast transient response, the output voltage at the POL is reliant on nearby charge stored in a reservoir of ceramic capacitors $C_{OUT(MLCC)}$ to minimize sag and overshoot in the initial microseconds of a high dI/dt transient load step-up and step-down, respectively. If used, $C_{OUT(BULK)}$ can be comprised of low ESR tantalum or low ESR polymer capacitor(s); these capacitors then serve as a local reservoir to replenish the MLCCs during transient load events. It is also possible to use $C_{OUT(MLCC)}$ only, however, the use of feedforward capacitors, C_{FF}, should then be installed in the remote-sense feedback path, to obtain an optimized transient response (see Figure 5 feedback connections).

The $C_{OUT(MLCC)}$ ceramic capacitors should be at least X5R-type material. X5R-type and X7R-type MLCCs are recommended when operating PCB temperatures are not more than 85°C and 125°C, respectively. Both materials are renown in the industry for having a relatively low capacitance change over their respective temperature range of operation (±15%). However, X5R and X7R MLCCs do exhibit significant loss of capacitance with applied DC voltage and are subject to aging effects, and this must be taken into account in any system design. Refer to the capacitor manufacturer's specifications for details.

The typical output capacitance range is between 200µF to 800µF. The system designer should use discretion in determining whether additional output filtering may be needed, if further reduction of output ripple—or output voltage deviation during dynamic load or line transient events—is required.

In Table 9, guidelines are provided for output capacitor selection, for various operating conditions. The table optimizes total equivalent ESR and total bulk capacitance for the transient load step performance. Stability criteria is considered. The Linear Technology LTpowerCAD™ design tool is available for transient simulation and stability analysis, if desired.

Pulse-Skipping Mode vs Forced Continuous Mode

In applications where high DC/DC conversion efficiency at light-load currents is highly desired—when the input voltage source is a battery, for example—pulse-skipping mode operation should be employed. Pulse-skipping mode operation prevents power flow from the output capacitors to the input source. Be aware, however, due to M_{BOT}'s resulting asynchronous operation at light load, applications employing pulse-skipping mode may necessitate more output capacitance and/or a higher OV_{PGM} setting than operation in forced continuous mode would.

Pulse-skipping mode is activated by connecting FCB to $INTV_{CC}$. Forced continuous operation is activated by connecting FCB to SGND.

Be aware that in pulse-skipping mode and ultralight loads (say, less than 20mA out), the V_{ING} voltage may appear as a sawtooth waveform as a result of being charge-pumped at a slower rate, to conserve energy.

See Appendix E for more information on how pulse-skipping mode works.

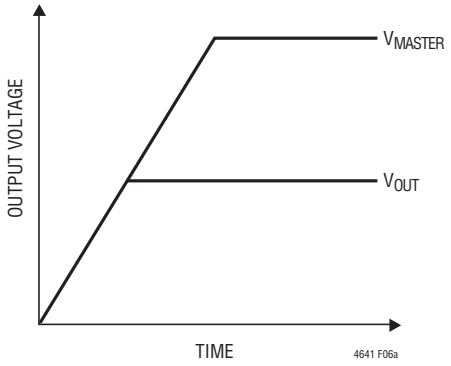
Soft-Start, Rail-Tracking and Start-Up Into Pre-Bias

The TRACK/SS pin can be used to either soft-start the output of the LTM4641 regulator, or make LTM4641's output voltage track another rail coincidentally or ratiometrically. When RUN or HYST is low, the TRACK/SS pin is discharged. When RUN and HYST are released, TRACK/SS sources a microamp of current.

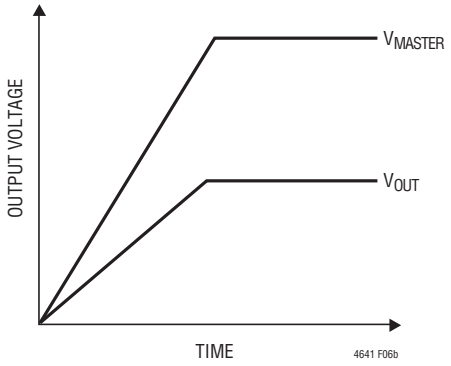
When a soft-start capacitor, C_{SS}, is applied to the pin, the current source is responsible for generating an output voltage turn-on time of 0.6ms per nanofarad of capacitance. The power stage is high impedance (M_{TOP} and M_{BOT} are off) until the TRACK/SS pin voltage exceeds V_{FB}, the remote-sense differential amplifier's output voltage. This allows power-up into pre-biased output voltage conditions without sinking of current from the output capacitors. When TRACK/SS exceeds the control IC's 600mV bandgap voltage, V_{FB} is regulated at 600mV and V_{OUT} reaches its nominal output voltage.

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

Figure 6 shows idealized output voltage waveforms for applications in which LTM4641's output (V_{OUT}) tracks a master rail (V_{MASTER}) coincidently and ratiometrically, respectively.



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

To configure LTM4641 for coincident or ratiometric tracking, begin the design (initially) the same way as for nontracking applications:

(1) Determine the R_{SET1A} , R_{SET1B}, and R_{SET2} values appropriate for the final, "full-scale" (FS) output voltage.

(2) Determine the R_{fSET} resistor needed to guarantee ramp down of the output voltage to the desired value. For example, if it is necessary for V_{OUT} to ramp down to 0.8V while tracking the master rail, then R_{fSET} is recommended from Table 1 to be ~887kΩ. If ramp-down tracking is not needed, then R_{fSET} can be chosen according to Table 1 (or Figure 3) and the FS output voltage of the LTM4641 generated rail.

(3) Choose output capacitors and input capacitors for the design in the same manner as is done for nontracking applications.

To fulfill a coincident rail-tracking requirement, recognize that when the output voltage of the master rail reaches the tracking rail's nominal FS voltage, the TRACK/SS pin of the LTM4641 (tracking slave) needs to be 600mV. This can be satisfied by forming a resistor-divider network composed of R_{TAC} and R_{TBC}, interfacing V_{OUT_MASTER} to TRACK/SS of the LTM4641 tracking slave, and terminating to SGND of the LTM4641 tracking slave. In Figure 7 and Figure 8, U1 generates a master rail while U2 generates a coincident-tracking rail that follows U1's output. Values of R_{TAC} and R_{TBC} are selected such that:

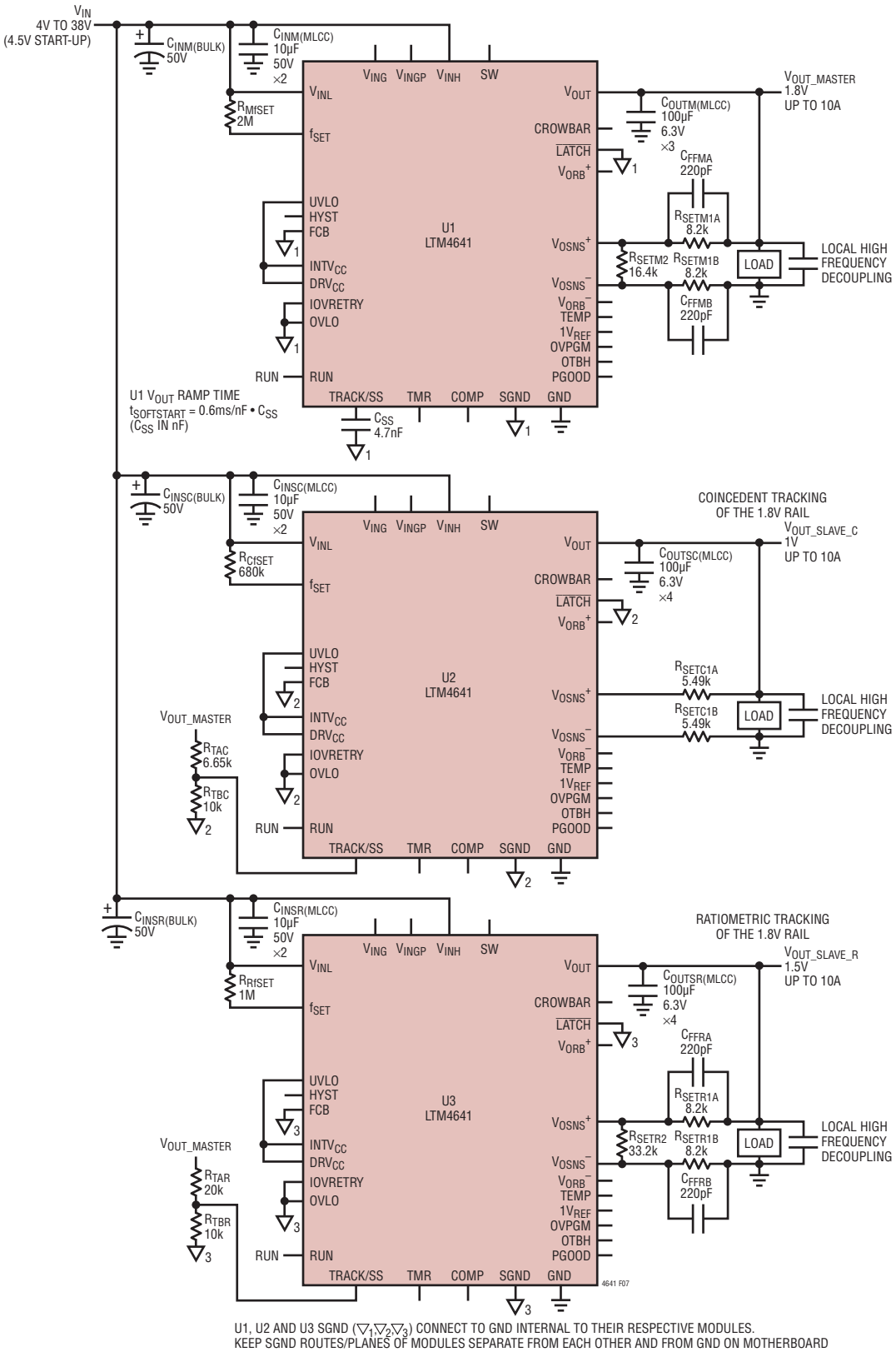
$$R_{TAC} = \left(\frac{V_{OUT_SLAVE_C\ (FS\ OUTPUT)}}{0.6V} - 1 \right) \bullet R_{TBC} \quad (17)$$

In the example circuit of Figure 7, the master rail generated by U1 ramps up its output to 1.8V. The coincident-tracking rail is generated by U2 and has a nominal FS output voltage of 1V. Values of R_{TAC} and R_{TBC} are determined such that when U1's output reaches 1V, the TRACK/SS pin of U2 reaches ~600mV; choosing R_{TBC} to be 10kΩ yields R_{TAC} = (1V/0.6V – 1) • 10kΩ, or ~6.65kΩ. It is common to choose resistor values of 10k or less for this task, so that voltage offset errors introduced by the 1µA current source on TRACK/SS working into the R_{TAC}/R_{TBC} network are sufficiently small.

To fulfill a ratiometric rail-tracking requirement, recognize that when the output voltage of the master rail reaches its final FS value, the TRACK/SS pin of the LTM4641 (tracking slave) needs to reach 600mV. This can be satisfied by forming a resistor-divider network composed of R_{TAR} and R_{TBR}, interfacing V_{OUT_MASTER} to TRACK/SS of the LTM4641 tracking slave, and terminating to SGND of the LTM4641 tracking slave. In Figure 7 and Figure 8, U3 generates a ratiometric-tracking rail that follows U1's output. Values of R_{TAR} and R_{TBR} are selected such that:

$$R_{TAR} = \left(\frac{V_{OUT_MASTER\ (FS_OUTPUT)}}{0.6V} - 1 \right) \bullet R_{TBR} \quad (18)$$

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES



U1, U2 AND U3 SGND ($\nabla_1\nabla_2\nabla_3$) CONNECT TO GND INTERNAL TO THEIR RESPECTIVE MODULES.
KEEP SGND ROUTES/PLANES OF MODULES SEPARATE FROM EACH OTHER AND FROM GND ON MOTHERBOARD

Figure 7. Examples of LTM4641 Performing Coincident and Ratiometric Rail-Tracking. cf. Figure 8 Waveforms

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

In the example circuit of Figure 7, the master rail generated by U1 ramps up its output to 1.8V. The ratiometric-tracking rail is generated by U3 and has a nominal FS output voltage of 1.5V. Values of R_{TAR} and R_{TBR} are determined such that when U1's output reaches its final value, 1.8V, the TRACK/SS pin of U3 reaches ~600mV: choosing R_{TBR} to be 10kΩ yields $R_{TAR} = (1.8V/0.6V – 1) • 10k\Omega$, or ~20kΩ. It is common to choose resistor values of 10k or less for this task, so that errors introduced by the 1µA current source on TRACK/SS are sufficiently small.

Figure 8 shows an oscilloscope snapshot of the output voltage waveforms of the modules configured per the Figure 7 circuit, with 6Ω load on V_{OUT_MASTER} and no load on the $V_{OUT_SLAVE_C}$ and $V_{OUT_SLAVE_R}$ outputs.

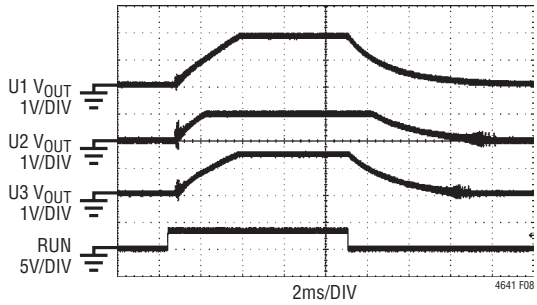


Figure 8. Output Voltage Waveforms of U1, U2 and U3. cf. Figure 7 Circuit.

For applications that do not require tracking or sequencing, applying at least 100pF on the TRACK/SS pin is recommended, corresponding to ~60µs output voltage start-up ramp time. The resulting soft-start period will limit start-up input surge current and output voltage overshoot.

$INTV_{CC}$ and DRV_{CC}

The LTM4641 module has an internal 5.3V low dropout regulator whose input is fed from the low current input voltage bias pin, V_{INL}, through a Schottky diode. The output, $INTV_{CC}$, is used to power control and housekeeping circuitry and the MOSFET drivers, and is up-and-running whenever bias on V_{INL} is present. DRV_{CC} is the power input pin to the MOSFET driver circuitry. In most cases, connect $INTV_{CC}$ to DRV_{CC}. The $INTV_{CC}$ regulator can source up to 30mA, continuous, which is sufficient for powering DRV_{CC}, even at the LTM4641's highest recommended switching frequency ($6V_{OUT}$ condition).

The power loss in the LDO can be considerable at high input voltage, given by:

$$P_{LOSS(INTVCC_LDO)} = (V_{INL} – 5.3V) • (5mA + I_{DRVCC}) \quad (19)$$

This power loss can be virtually eliminated when a ~5V to 6V rail is available to overdrive the $INTV_{CC}/DRV_{CC}$ pins through a Schottky diode, as shown in the Figure 51 circuit. This is because the LDO can only pull $INTV_{CC}$'s voltage in an upward direction—that is to say, the series-pass element turns off when $INTV_{CC}$ exceeds the LDO control loop's regulation setpoint. Infrared thermal images in Figures 52 to 55 illustrate operating conditions in which up to ~5°C reduction in package surface temperature is obtained by employing this technique. Note the importance to provide a diode-ORed path from V_{IN} to V_{INL} and from $INTV_{CC}/DRV_{CC}$ to V_{INL} when $INTV_{CC}/DRV_{CC}$ is overdriven by an auxiliary rail (or V_{OUT}). This assures proper MOSFET driver behavior regardless of disappearance/appearance of V_{INL} versus V_{AUX}, in any combination or sequence of rail ramp-up/ramp-down events. The series-connected Schottky diode internal to the LTM4641 that feeds the LDO from V_{INL} assures proper MOSFET driver and internal logic behavior, even in the event of rapid discharging and restoration of V_{INL}.

A housekeeping circuit that monitors DRV_{CC} voltage inhibits switching action until DRV_{CC} exceeds 4.05V. Once switching action commences, DRV_{CC} is allowed to fall to 3.35V before switching action is inhibited. The DRV_{CC} voltage monitor has glitch immunity characteristics as shown in Figure 12.

DRV_{CC} current is proportional to switching frequency. For applications with extremely fast output voltage start-up (e.g., C_{SS} < 100pF on TRACK/SS, or rail tracking very fast rails with sub 60µs turn-on time), switching frequency may

APPLICATIONS INFORMATION—POWER SUPPLY FEATURES

conceivably approach f_{MAX} at start-up, however briefly (see Equation 8). When biasing DRV_{CC} from $INTV_{CC}$ in such applications, $INTV_{CC}$ may require additional bypass capacitance to ride through the resulting current surge on DRV_{CC}. $INTV_{CC}$ can by bypassed with up to 4.7µF (±20% tolerance) of external decoupling capacitance.

$1V_{REF}$

A housekeeping IC internal to the LTM4641 generates a 1V ±1.5% reference voltage. This voltage reference is generated independent of the control IC's 600mV bandgap voltage. The $1V_{REF}$ should only be used to alter the OV_{PGM} threshold programming voltage for the fast OOV comparator (see Fast Output Overvoltage Comparator Threshold section) or to implement an auxiliary overtemperature detector with an NTC having ultrahigh resistance (470k at 25°C, B-value < 5000K)—in the manner shown in Figure 47. Loading $1V_{REF}$ beyond ±100µA is not recommended.

$1V_{REF}$ must become established quickly at start-up to properly bias OV_{PGM}, and therefore no external capacitance should be applied to this pin. To minimize disturbance to the OV_{PGM} voltage, dynamic step-loading of the $1V_{REF}$ is not recommended. Figure 9 shows the step response of $1V_{REF}$ to a 0µA to 100µA step load with 100A/s slew rates, and the resulting impact to OV_{PGM}'s voltage waveform.

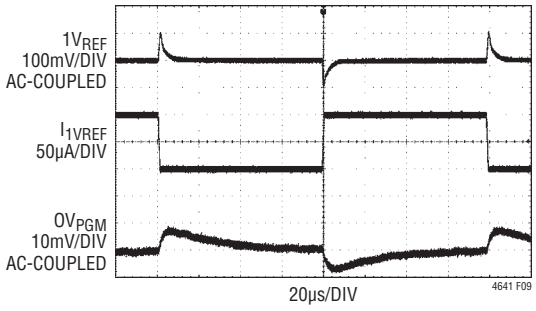


Figure 9. Response of $1V_{REF}$ to 0µA ⇔ 100µA Load Steps Applied at 100A/s—and Resulting Disturbance and Recovery of OV_{PGM}. Figure 43 Circuit. Do Not Load $1V_{REF}$ Arbitrarily

TEMP, OTBH and Overtemperature Protection

As seen in Figure 1, a resistor-NTC-divider network formed between $1V_{REF}$ and SGND generates TEMP, an analog temperature indicator pin. The pin nominally measures ~0.98V at 25°C and colder, and ~585mV at 125°C. A graph of the relationship between junction temperature, NTC resistance, and TEMP voltage is found in Figure 10.

The TEMP pin also connects indirectly to a comparator input whose output can pull HYST low to inhibit switching action. If TEMP falls below 438mV, corresponding to a junction temperature of ~147°C, switching action is inhibited. If OTBH is logic low when TEMP falls below 438mV, a latchoff overtemperature event is registered. Restarting regulation after a latchoff event has occurred is explained in detail in the Start-Up/Shutdown section. If OTBH is open circuit when TEMP falls below 438mV, a nonlatching overtemperature event is registered: switching action can resume when the units cools off and the TEMP pin rises above 514mV, corresponding to a junction temperature of ~136°C.

The LTM4641's overtemperature protection feature is intended to protect the device during momentary overload conditions. Recognize that the LTM4641 is rated for 125°C junction, absolute maximum, and that junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

The overtemperature protection circuit can be disabled by connecting TEMP to $1V_{REF}$. With moderate linear circuit analysis, the information in Figure 10 and Figure 62 (Appendix A) can be used to alter the overtemperature inception and recovery thresholds. If desired, the thresholds can be increased by applying a resistor from TEMP to $1V_{REF}$, or decreased by applying a resistor from TEMP to SGND. The overtemperature comparator contains built-in filtering, yielding glitch immunity characteristics shown in Figure 12.

APPLICATIONS INFORMATION—INPUT PROTECTION FEATURES

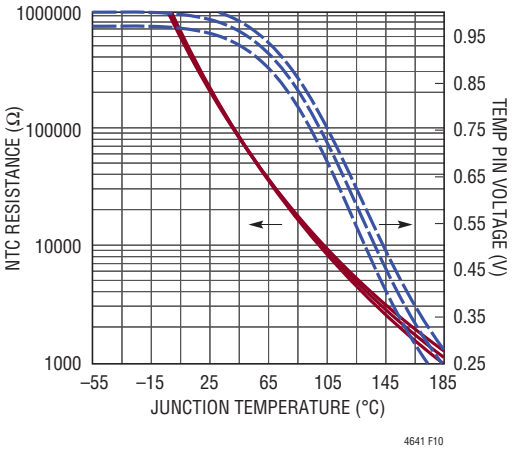


Figure 10. Relationship of NTC Resistance to Junction Temperature and Resulting TEMP Voltage. Curves for Nominal Values and Calculated Extreme Values Shown

Input Monitoring Pins: UVLO, IOVRETRY, OVLO

The UVLO pin feeds directly into the inverting input of a comparator whose trip threshold is 0.5V. The behavior of the UVLO pin is an example of a nonlatching fault: when the UVLO pin falls below 0.5V, HYST is pulled low and switching action is inhibited; when the UVLO pin exceeds 0.5V, HYST goes logic high and switching action can resume. The IOVRETRY and OVLO pins each feed directly into noninverting inputs of comparators whose trip thresholds are 0.5V. The behavior of the IOVRETRY pin is also an example of a nonlatching fault pin: when the IOVRETRY pin exceeds 0.5V, HYST is pulled low and switching action is inhibited; when IOVRETRY falls below 0.5V, switching action can resume. The behavior of the OVLO pin is an example of a latchoff fault pin: when the OVLO pin exceeds 0.5V, HYST is pulled low and switching action is inhibited; when OVLO subsequently falls below 0.5V, HYST remains latched low, and switching action cannot occur until the latch has been reset. Restarting regulation after a latchoff event has occurred is explained in detail in the Start-Up/Shutdown section.

These three pins give added flexibility to tailor some behaviors of the LTM4641. The UVLO pin input is primarily used to set customized UVLO rising and UVLO falling thresholds, utilizing a high impedance connection to the HYST pin to obtain hysteresis. There are times when the LTM4641's default UVLO rising and UVLO falling thresholds of $4.5V_{IN}$ rising (maximum) and $4V_{IN}$ falling (maximum) are not suitable. For example, it can be convenient to apply customized UVLO settings to inhibit switching prior to entering a region of possible dropout operation (Figure 51). It may be desirable to set a very large UVLO hysteresis, if line sag is problematic. UVLO is highly recommended to be customized to monitor the source supply feeding V_{INH} when V_{INL} is biased from an auxiliary rail (Figure 49).

The UVLO pin input may also be used to provide novel circuit solutions such as one found in Figure 47: to detect an overtemperature event in MSP—sensed via an external NTC in close proximity to the power interrupt MOSFET, MSP; and to respond to MSP overtemperature by inhibiting switching action and turning off MSP until the MOSFET returns to normal temperatures.

IOVRETRY is primarily used to set the input voltage (V_{IN}) threshold above which switching action is inhibited, but not latch off. OVLO is primarily used to set the input voltage (V_{IN}) threshold above which switching action latches off. Just as the UVLO pin can be used in versatile ways, so can IOVRETRY and OVLO.

Consult Appendix A to see the UVLO/IOVRETRY/OVLO pins' functions in greater detail.

The most common arrangement of components connecting V_{IN} to UVLO, HYST, IOVRETRY and OVLO is shown in Figure 11.

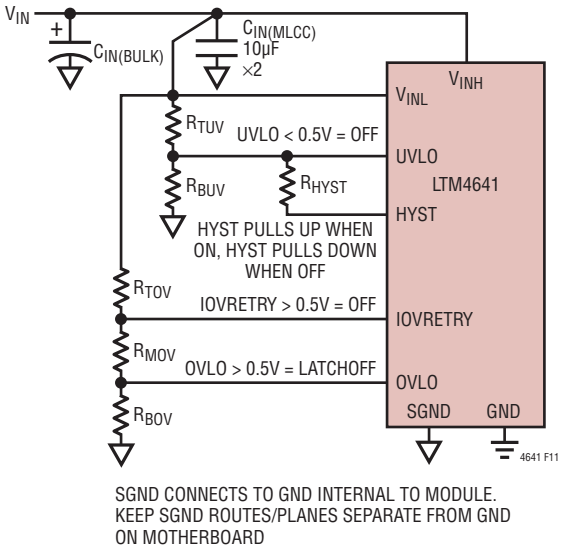


Figure 11. Setting the LTM4641 Custom UVLO Rising and UVLO Falling Thresholds, Nonlatching Input Overvoltage Threshold, and Latching Input Overvoltage Threshold

APPLICATIONS INFORMATION—INPUT PROTECTION FEATURES

Variables to define up-front are as follows:

- V_{SU}: V_{IN} start-up voltage, in volts. This is the customized UVLO rising voltage.
- V_{SD}: V_{IN} shutdown voltage, in volts. This is the customized UVLO falling voltage.
- V_{HYST}: The value of the voltage on the HYST pin (in volts) when switching action is on and just prior to the input voltage (V_{IN}) falling below V_{SD}.
- R_{HYST}: The hysteresis-setting resistor. If used, R_{HYST} is recommended to take on a value of 1MΩ or higher, so that the HYST voltage is negligibly affected by external loading.
- V_{OV}: The input voltage above which a latchoff input overvoltage event occurs.
- V_{RT}: The input voltage above which a nonlatching input overvoltage event occurs.

Then, R_{TUV} and R_{BUV} are given by:

$$R_{TUV} = \frac{V_{SU} - V_{SD}}{V_{HYST}} \bullet R_{HYST} \quad (20)$$

and

$$R_{BUV} = \frac{UVOV_{TH}}{\frac{V_{SU} - UVOV_{TH}}{R_{TUV}} - \frac{UVOV_{TH}}{R_{HYST}}} \quad (21)$$

$UVOV_{TH}$ is nominally 0.5V, from the Electrical Characteristics Table. The value of V_{HYST} used in the above equations requires more careful consideration. Review Figure 1 and assess system details of the specific application in which the LTM4641 is being placed. It is known from the Electrical Characteristics table that when $V_{INL} \geq 6V$ that $INTV_{CC}$ = 5.3V; and we see the voltage on the HYST pin, when switching action is on, is $V_{HYST(SWITCHING_ON)}$, 5.1V—nominally. Observe that if the RUN pin were driven high by 3.3V logic, however, that V_{HYST} would be a Schottky diode forward-voltage drop above 3.3V—and V_{HYST} in that instance would be 3.6V. If V_{SD} is targeted below $6V_{IN}$, it is necessary to consider that V_{HYST}'s pull-up voltage, $INTV_{CC}$, is decreasing with V_{INL}. For example, at V_{INL} = 4.5V input, $INTV_{CC}$ is nominally 4.3V ($V_{INTVCC(LOWLINE)}$), and it is inferred (in that scenario) that V_{HYST} would be closer to 4.1V, when RUN is floating.

It is the moderately weak pull-up strength of HYST (10kΩ pull-up to $INTV_{CC}$), and the desire for any loading of the HYST signal to negligibly alter the HYST logic-high output voltage level (less than ~50mV), that motivates a high impedance (~1MΩ) hysteresis-setting resistor to interface between HYST and UVLO, when custom UVLO settings are desired.

The customized UVLO start-up and shutdown input voltage settings can be double-checked with:

$$V_{SU} = UVOV_{TH} \bullet \left(\frac{R_{TUV}}{R_{BUV} \,||\, R_{HYST}} + 1 \right) \quad (22)$$

$$V_{SD} = V_{SU} - \frac{V_{HYST}}{R_{HYST}} \bullet R_{TUV} \quad (23)$$

To set the input overvoltage (latching and nonlatching) thresholds, choose first how much current, I_{DIV}, to continually have drawn by the $R_{TOV}/R_{MOV}/R_{BOV}$ resistor-divider string for this function, at ultrahigh line. 10µA to 20µA is a normal amount to allocate.

The total resistance of the divider string is then given by:

$$R_{TOT} = \frac{V_{OV}}{I_{DIV}} \quad (24)$$

Then, the resistors in the input overvoltage divider are given by:

$$R_{BOV} = \frac{R_{TOT} \bullet UVOV_{TH}}{V_{OV}}, \quad (25)$$

$$R_{MOV} = UVOV_{TH} \bullet R_{TOT} \bullet \left(\frac{1}{V_{RT}} - \frac{1}{V_{OV}} \right), \quad (26)$$

$$R_{TOV} = R_{TOT} - R_M - R_B \quad (27)$$

It may be tempting to try rearranging these equations so that R_{TOV}'s value is fixed, first, and to compute R_{MOV} and R_{BOV} subsequently. However, due to large divide-down ratio (usually) of ultrahigh line input voltage down to these pins with ~0.5V thresholds, the rounding off of R_{MOV} and R_{BOV} to nearest EIA standard values after fixing R_{TOV}'s

APPLICATIONS INFORMATION—INPUT PROTECTION FEATURES

value in place often significantly alters one or both V_{IN} referred overvoltage thresholds. It is more efficient to work through Equations 24 to 27 in the sequence shown and iterate (if necessary) towards finding convenient (EIA standard) resistor values.

The latchoff input overvoltage threshold can be double-checked with:

$$V_{OV} = UVOV_{TH} \bullet \left(\frac{R_{TOV} + R_{MOV}}{R_{BOV}} + 1 \right) \quad (28)$$

The nonlatching overvoltage threshold can be double-checked with:

$$V_{RT} = UVOV_{TH} \bullet \left(\frac{R_{TOV}}{(R_{MOV} + R_{BOV})} + 1 \right) \quad (29)$$

The UVLO, IOVRETRY and OVLO pins do not require any filter capacitance due to built-in filtering in the LTM4641's housekeeping IC. This results in glitch immunity with characteristics shown in Figure 12.

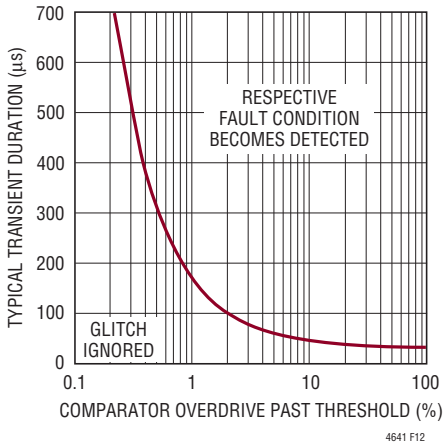


Figure 12. Transient Duration vs Comparator Overdrive Glitch Immunity Characteristics. Monitored Signals: UVLO, IOVRETRY, OVLO, TEMP, CROWBAR and DRV_{CC}

Start-Up/Shutdown and Run Enable; Power-On Reset and Timeout Delay Time

The LTM4641 is a feature-rich and versatile self-contained DC/DC converter system, and includes multiple on-board supply monitors. The inputs to several monitors are available to the user for system customization (UVLO, OVLO, IOVRETRY and TEMP).

The LTM4641 powers up its output when the following conditions are met:

- RUN exceeds 1.25V (nominal; 2V, overtemperature); power-on reset (POR) and timeout delay times do not apply to RUN.
- All nonlatching fault-monitor pins have been in their operationally valid states for the full duration of the POR delay time, set optionally by C_{TMR} (the capacitor on the TMR pin). Explicit pins and operationally valid thresholds follow:
  a. DRV_{CC} > 4.05V. In the circuits of Figures 45 and 46, this is guaranteed for $V_{INL} \geq 4.5V$, minimum. In Figure 49, this requirement is met when the auxiliary bias supply exceeds 4.05V.
  b. UVLO > 500mV
  c. IOVRETRY < 500mV
  d. TEMP > 514mV (when OTBH is electrically open circuit)
- No latchoff fault conditions are present, and the LTM4641 is not in a "latched off" state from any previously detected latchoff fault condition. If a latchoff fault condition occurs/occurred, the LTM4641 must be unlatched by a logic high $\overline{LATCH}$ signal: if all latchoff fault-monitoring pins are in operationally valid states when $\overline{LATCH}$ transitions from logic low to high, the LTM4641 becomes immediately unlatched; if, instead, any latchoff fault-monitoring pin is outside its operationally valid state when $\overline{LATCH}$ is logic high, the LTM4641 becomes unlatched if $\overline{LATCH}$ remains logic high after all latchoff fault-monitoring pins have been in their operationally valid states for the full duration of the timeout delay time (set optionally by C_{TMR}). Explicit pins and operationally valid thresholds follow:
  a. OVLO < 500mV
  b. TEMP > 514mV (when OTBH is logic low)
  c. CROWBAR < 1.5V

The POR and timeout delay time is 9ms per nanofarad of C_{TMR} capacitance. If C_{TMR} is not used, the POR and timeout delay time is ~90µs.

APPLICATIONS INFORMATION—LOAD PROTECTION FEATURES

If any nonlatching fault conditions occur, internal circuitry pulls HYST low and switching action is inhibited. The power stage will be high impedance until the aforementioned start-up conditions are met. If any latchoff fault condition occurs, HYST is latched low and switching action is inhibited until the LTM4641 is unlatched (by pulling $\overline{LATCH}$ logic high) or V_{INL} power is recycled (with $INTV_{CC}$ falling below 2V).

The LTM4641 can be configured to restart autonomously after an adjustable timeout delay time—instead of exhibiting latchoff behavior—by leaving $\overline{LATCH}$ logic high (connected to $INTV_{CC}$, for example) and setting the hiccup retry timeout delay time with C_{TMR} (see Figure 47). Be reminded that use of C_{TMR} also introduces POR behavior, yet the POR and timeout delay timers operate independently. The effect of C_{TMR} can be negated by pulling the TMR pin to $INTV_{CC}$.

Switching action will be inhibited if any of the following occur:

- RUN is less than 1.15V (nominal; 0.8V, overtemperature). Not a fault; no POR or timeout delay time is imposed.
- Any nonlatching faults occur:
  a. DRV_{CC} falls below 3.35V. In the Figure 45 and Figure 46 circuits, this happens at V_{INL} < 4V, maximum.
  b. UVLO falls below 0.5V.
  c. IOVRETRY exceeds 0.5V.
  d. TEMP falls below 438mV when OTBH is electrically open circuit.
- Any latchoff faults occur:
  a. OVLO exceeds 0.5V.
  b. CROWBAR exceeds 1.5V.
  c. TEMP falls below 438mV when OTBH is logic low.

The LTM4641's state diagram is provided in Appendix B. Start-up and shutdown mechanisms for any given operating scenario are identified in the state diagram. The TEMP and DRV_{CC} pins have built-in hysteresis. The UVLO, IOVRETRY, OVLO, TEMP, CROWBAR and DRV_{CC} pins connect to comparators with built-in glitch immunity, with characteristics indicated in Figure 12.

Overcurrent Foldback Protection

The LTM4641 has overcurrent protection (OCP). In a short circuit from V_{OUT} to GND, the internal current comparator threshold folds back during a short to reduce the output current, progressively down to about one-third of its normal value (down from 24A to 8A, typical). To recover from foldback current limit, the excessive load or low impedance short needs to be removed. Foldback current limiting action is disabled during soft-start and tracking start-up.

Power Good Indicator and Latching Output Overvoltage Protection

Internal overvoltage and undervoltage comparators assert the open-drain PGOOD output logic low if the output voltage is outside ±10% of nominal, after a 12µs "blanking time". The blanking time allows the output voltage to experience brief excursions (due to large load-step transients, for example) without nuisance-tripping PGOOD. The PGOOD output is deasserted without any deliberate blanking time when the output voltage returns to (or enters) the power good window, with ~2% to 3% of hysteresis. If the feedback voltage exceeds the upper PGOOD valid limit, the synchronous power MOSFET, M_{BOT}, turns on (with no blanking time)—to try sinking current from the output to GND, through LTM4641's power inductor—until the output voltage returns to the PGOOD valid region. If the output voltage exceeds an adjustable threshold set by OV_{PGM}, whose default value corresponds to 11% above nominal, the LTM4641 pulls its CROWBAR output logic high immediately (500ns response time, maximum) and latches off its output voltage: the power stage becomes high impedance, with both M_{TOP} and M_{BOT} turning off and staying latched off; furthermore, MSP's gate is pulled to V_{INH} potential rapidly (<2.6µs response time, maximum), to disconnect the input source voltage from the module's power stage. Restarting regulation after a latchoff event has occurred is explained in detail in the Start-Up/Shutdown section.

The behavior of turning on the synchronous MOSFET during detection of an output overvoltage is a rudimentary and popular kind of output overvoltage protection scheme commonly found in the power supply and semiconductor control IC industry. It can provide mediocre overvoltage

APPLICATIONS INFORMATION—LOAD PROTECTION FEATURES

protection during severe load current step-down events, but is not very effective at protecting loads from genuine fault conditions such as a short circuited high side power switching MOSFET. Furthermore, such schemes tend to be implemented with the overvoltage detector's threshold dependent on the same bandgap voltage that the output is being regulated to. Applications needing superior output overvoltage and load protection require the performance achieved with the output crowbar MOSFET, MCB and power interrupt switch, MSP, and LTM4641's use of an independent reference voltage($1V_{REF}$) to generate an OOV threshold.

Power-Interrupt MOSFET (MSP), CROWBAR Pin and Output CROWBAR MOSFET (MCB)

Within 500ns (maximum) of the control-loop-referred feedback signal, V_{FB}, exceeding the voltage on OV_{PGM} (plus-or-minus OVP_{ERR}), an OOV event is detected, and the CROWBAR output swings high enough to turn on an optional crowbaring device (MCB) residing on V_{OUT}. No more than 2.6µs after OOV detection, V_{ING} is discharged and an optional power interrupt switch, MSP, disconnects the LTM4641's power stage from the input source supply.

When MCB and MSP are used in conjunction as shown in the Figure 46 circuit, the LTM4641 is able to provide best-in-class output overvoltage protection against arguably the most despised failure mode high step-down buck converters can theoretically suffer: an electrical short between the input source to the output, via the switching node. Turning on MCB upon detection of OOV helps discharge the output capacitors and prevent any further positive excursion of output voltage by transforming residual energy in LTM4641's power stage into heat; meanwhile, turning off MSP removes a path for current flow between the input power source and the output—preventing hazardous (input) voltage from reaching the precious load.

It should be noted that when an OOV event is detected, CROWBAR is not held high (equivalently, MCB is not left turned on) indefinitely. The act of pulling CROWBAR high (above 1.5V nominal), whether due to internal or external circuitry, invokes a latchoff response and strong discharge of V_{ING}; HYST is latched low and switching action is inhibited after CROWBAR overcomes the glitch immunity requirement (see Figure 12). The fast OOV comparator's output is fed through a blocking PN diode into a 10nF capacitor on the CROWBAR output; internal circuitry interfacing to CROWBAR presents itself as a ~10kΩ load (see Figure 62 in Appendix A). The use of the PN diode and 10nF capacitor creates a way for the CROWBAR output to stay logic high, even if the duration of OOV is very brief, and assures the glitch immunity of the latchoff detection circuitry is overcome. The 10kΩ load and 10nF capacitor provide an upper bound for the duration of time MCB might be on after CROWBAR activates: 400µs, or four time constants. Parasitic capacitance on the gate of MCB may increase this time, slightly.

Observe that when HYST is low, the noninverting input to the fast OOV comparator (see Appendix A) is clamped by a Schottky diode. (When RUN is low, the noninverting input to the fast OOV comparator is clamped by two series Schottky diodes.) This differs from when switching action is engaged, where the noninverting input to the fast OOV comparator is normally the V_{FB} signal. Therefore, be aware that the CROWBAR output is nominally inhibited when switching action is inhibited.

Restarting regulation after a latchoff event has occurred is explained in detail in the Start-Up/Shutdown section.

MCB should be placed close to the majority of the load(s)'s bulk and MLCC local bypass capacitors. CROWBAR should be connected to the gate of MCB with a generous signal trace width (20mils, or 0.5mm), to support driving the peak current needed to turn on MCB upon OOV detection. At the instant that MCB turns on, it typically draws hundreds of amps from the output capacitors which are mainly located near the load. When MCB turns off, the B-field that may have been built up in the parasitic inductance in the copper plane between the output capacitors and MCB cannot vanish instantaneously, and the collapsing of that B-field can induce a negative voltage across the output capacitors and load. Closer proximity of MCB to the majority of the output capacitors minimizes this parasitic inductance and hence the resulting magnitude of the negative voltage spike.

MCB must be selected according to the following criteria:

- MCB must be a logic-level N-channel MOSFET
- The drain-to-source rating of MCB must be greater than the maximum output voltage, $V_{OUT(PEAK,OOV_DETECTED)}$

APPLICATIONS INFORMATION—LOAD PROTECTION FEATURES

- When CROWBAR goes logic high, the peak drain current in MCB will be given by $V_{OUT(PEAK,OOV_DETECTED)}/R_{DS(ON)}$. The peak drain current, and its duration, must not exceed the maximum safe operating area of the MOSFET; consult the MOSFET vendor's data sheet. An upper bound for MCB's on-time is 400µs. However, this worst-case conduction time can only happen if the output capacitance on V_{OUT} is extraordinarily large. The length of time that MCB can possibly conduct ultrahigh drain current is also bounded by $4 \bullet R_{DS(ON)} \bullet C_{OUT(TOTAL)}$. In a majority of applications, output capacitance is low enough that MCB does not conduct ultrahigh drain current for longer than a few microseconds, as seen on the front page.
- MCB's junction temperature must not exceed its specified maximum at any time. Consult the MOSFET vendor's data sheet for device thermal characteristics for "single shot" thermal transients or "single pulse" power-handling capability. The peak power sustained by MCB is $V_{OUT(PEAK,OOV_DETECTED)}^2/R_{DS(ON)}$.

If MCB is used and it is expected that $\overline{LATCH}$ will be toggled high (to unlatch the LTM4641) or held logic high continuously (for automatic LTM4641 restart after fault-off), recognize that peak power sustained by MCB during CROWBAR activity may not be single pulse anymore. Therefore, to prevent MCB thermal overstress in such applications, it is recommended to use C_{TMR} to set a reasonable cool-down period for the MOSFET. Additionally, one may opt to implement a circuit that shuts down the LTM4641 when MCB temperature is detected to be too high: a minor modification to Figure 47, RT1 would be located as close in proximity to MCB as possible (instead of MSP), and R1, R2, and R3 would be experimentally determined. Consult the MOSFET vendor's data sheet for maximum rated junction temperature and device thermal characteristics for repeated pulsed-power transients.

When using MSP, connect V_{ING} to V_{INGP} and to the gate of MSP. See the Input Capacitors section (earlier) for information on the input bypassing technique when MSP is used.

MSP must be selected according to the following criteria:

- MSP can be either a standard logic or a logic-level N-channel MOSFET.
- The drain-to-source breakdown voltage of MSP must be greater than the maximum input source voltage. Consult the MOSFET vendor's data sheet and consider temperature effects.
- In order to support very fast turn-on of output voltage (e.g., sub 1ms ramp up), MSP should be turned on quickly to bring up V_{INH} quickly. Therefore, a gate input capacitance (C_{ISS}) below 4.7nF is preferred (less is better).
- MSP must be able to conduct the maximum input current to the LTM4641's power stage without getting too hot. Choose a suitable MOSFET package size and $R_{DS(ON)}$ that results in reasonable MOSFET junction temperature rise. Be mindful that $I_{Q(VINH)}$ is highest during low line operation.

Blowing a series-pass input fuse with a crowbaring SCR can be an effective overvoltage protection scheme for higher output voltages, e.g., 5V, but a crowbaring MOSFET on the output of the converter is more effective at clamping the output voltage. For the same current, the power MOSFET will have much less voltage drop than the PN-junction voltage drop of an SCR. SCR-based circuits involving the LTM4641 are not presented here. Evaluation of induced or simulated overvoltage events on a demo board (such as DC1543) is recommended to ensure the end result meets the user's expectations.

Fast Output Overvoltage Comparator Threshold

OV_{PGM} is nominally biased by internal circuitry to 666mV, according to a 499kΩ and 1MΩ resistor-divider network internal to the LTM4641 driven from the $1V_{REF}$. This pin connects directly to the inverting input of the fast OOV comparator—setting the trip threshold that the control-loop-referred feedback voltage, V_{FB}, would have to exceed to result in CROWBAR becoming logic high. Recall that the control-loop pulse frequency modulates M_{TOP} such that V_{FB} is driven to the lesser of the TRACK/SS pin or the bandgap reference voltage of 600mV. When TRACK/SS (and hence, the output voltage) has been fully ramped up, the 666mV on OV_{PGM} represents an OOV setting 11% above nominal output voltage. To increase the OOV threshold, a resistor can be connected externally from $1V_{REF}$ to OV_{PGM}; to decrease the OOV threshold, a resistor can be connected externally from

APPLICATIONS INFORMATION—EMI PERFORMANCE

OVPGM to SGND. Furthermore, the OV_{PGM} trip voltage can be made more accurate than its default setting by paralleling the existing (internal) OV_{PGM} resistor-divider with an external resistor divider comprised of low T.C.R. ±0.1%-tolerance resistors, for example. See Appendix F for details on how to adjust or tighten the fast OOV comparator trip threshold.

The Switching Node: SW Pin

The SW pin provides access to the midpoint of the power MOSFETs in LTM4641's power stage.

Connecting an optional series RC network from SW to GND can dampen high frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or "snubs") the resonance of the parasitics, at the expense of higher power loss.

To use a snubber, choose first how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 1W resistor to be used—derated conservatively to 600mW (P_{SNUB})—then the capacitor in the snubber network (C_{SW}) is computed by:

$$C_{SW} = \frac{P_{SNUB}}{V_{INH(MAX)}^2 \bullet f_{SW}} \quad (30)$$

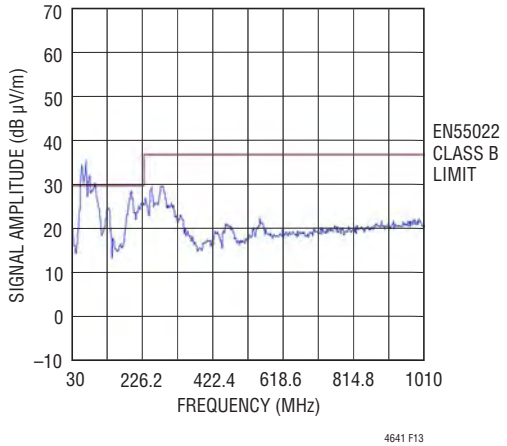


Figure 13. Radiated Emissions Scan of LTM4641 Producing $5V_{OUT}$ at 10A, from $12V_{IN}$. DC1543 Hardware with No Snubber Network Installed. f_{SW} = 550kHz. $C_{IN(BULK)} = 2 \times 100\mu F$, $C_{IN(MLCC)} = 4 \times 10\mu F$ X7R + $2 \times 4.7\mu F$ X7R. Measured in a 10 Meter Chamber. Quasi-Peak Detect Method

where $V_{INH(MAX)}$ is the maximum input voltage that the input to the power stage (V_{INH}) will see in the application, and f_{SW} is the DC/DC converter's full load switching frequency of operation. C_{SW} should be NPO, C0G or X7R-type (or better) material.

The snubber resistor (R_{SW}) value is then given by:

$$R_{SW} = \sqrt{\frac{5nH}{C_{SW}}} \quad (31)$$

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

EMI performance of LTM4641 (on DC1543) with and without a snubber is compared and contrasted in Figures 13 to 16. In the examples shown, the snubber networks reduce EMI signal amplitude by as much as ~5dB.

Access to SW is also provided to make it possible to deliberately induce a short circuit between the input of LTM4641's power stage (V_{INH}) and its switch node—to evaluate, in hardware, the performance of the LTM4641 when a high side MOSFET fault condition is simulated.

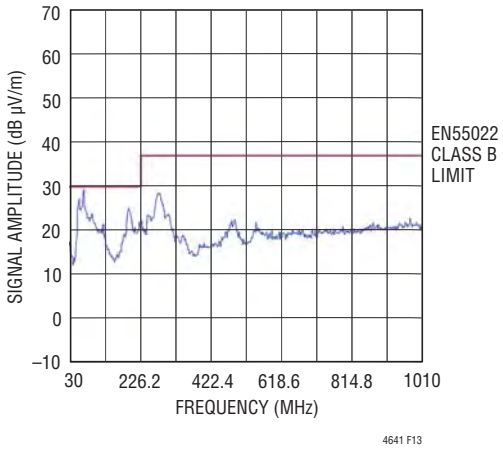


Figure 14. Radiated Emissions Scan of LTM4641 Producing $5V_{OUT}$ at 10A, from $12V_{IN}$. DC1543 Hardware with Ad Hoc Snubber Network Installed Directly Between SW Probe Point and GND, C_{SW} = 10nF, R_{SW} = 1Ω (1W-Rated). f_{SW} = 550kHz. $C_{IN(BULK)} = 2 \times 100\mu F$, $C_{IN(MLCC)} = 4 \times 10\mu F$ X7R + $2 \times 4.7\mu F$ X7R. Measured in a 10 Meter Chamber. Quasi-Peak Detect Method

APPLICATIONS INFORMATION—EMI PERFORMANCE

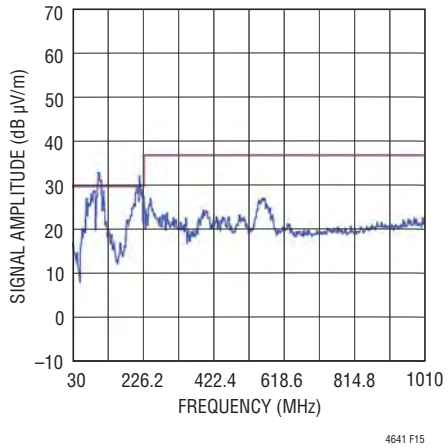


Figure 15. Radiated Emissions Scan of LTM4641 Producing 2.5V_{OUT} at 10A, from 24V_{IN}. DC1543 Hardware with No Snubber Network Installed. f_{SW} = 335kHz. $C_{IN(BULK)}$ = 2 × 100µF, $C_{IN(MLCC)}$ = 4 × 10µF X7R + 2 × 4.7µF X7R. Measured in a 10 Meter Chamber. Quasi-Peak Detect Method

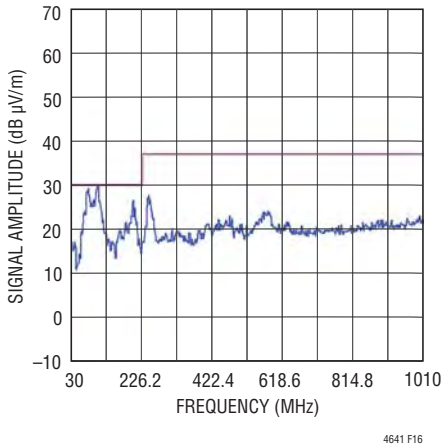


Figure 16. Radiated Emissions Scan of LTM4641 Producing 2.5V_{OUT} at 10A, from 24V_{IN}. DC1543 Hardware with Ad Hoc Snubber Network Installed Directly Between SW Probe Point and GND, C_{SW} = 2.2nF, R_{SW} = 2.2Ω (1W Rated). f_{SW} = 335kHz. $C_{IN(BULK)}$ = 2 × 100µF, $C_{IN(MLCC)}$ = 4 × 10µF X7R + 2 × 4.7µF X7R. Measured in a 10 Meter Chamber. Quasi-Peak Detect Method

APPLICATIONS INFORMATION—MULTIMODULE PARALLEL OPERATION

For loads that demand more than 10A of load current, multiple LTM4641 devices can be paralleled to provide more output current. See Figures 56 and 66 for examples of four or two LTM4641 operating in parallel to deliver 40A or 20A load current, respectively, while providing robust output overvoltage protection.

The LTM4641 does not support phase interleaving or clock synchronization, and therefore no ripple-current cancelation effect and no multiplication effect on the output voltage ripple frequency occurs when modules are paralleled. Therefore, it should be anticipated that paralleled applications contain beat frequencies in the output voltage waveform and are contained in the reflected input current. For example, if one module operates freely at 400kHz while its paralleled sibling operates freely at 410kHz, the conducted EMI content will include not only the switching fundamental frequencies—400kHz and 410kHz—but also a beat frequency at the difference of those frequencies, 10kHz. The system designer may be motivated to apply an external LC (or "pi") filter on the input to each LTM4641 if attenuation of the reflected input currents is desired.

The LTM4641 device is a current mode controlled device, so paralleled modules demonstrate good current sharing. This helps equilibrate power losses and reduce thermal differences between paralleled modules.

The following pins should be connected to all corresponding LTM4641s' pin(s) when paralleling LTM4641 outputs:

- V_{OUT}
- GND
- V_{INH}
- V_{INL}
- HYST (to synchronize start-up and shutdown)
- TRACK/SS
- COMP (to accomplish current sharing)
- CROWBAR (to synchronize output overvoltage response)
- $\overline{LATCH}$ (to reset all modules after a latchoff event)
- V_{ING}, if MSP is used

APPLICATIONS INFORMATION—MULTIMODE PARALLEL OPERATION

- V_{OSNS}^+, differentially bussed with V_{OSNS}^-; use GND shielding
- V_{OSNS}^-, differentially bussed with V_{OSNS}^+; use GND shielding
- PGOOD, if used

Pulling any one module's RUN pin low will pull all module's HYST pins low, to cease switching and output voltage regulation. When paralleling LTM4641 outputs, each module should have its own R_{fSET} resistor locally (if needed) to set the on time (I_{ION}) consistent with the output voltage setting (cf. Table 1 and Figure 3). Customized UVLO settings, latching and nonlatching input overvoltage thresholds, and output overvoltage thresholds need only be configured on one LTM4641. $INTV_{CC}$ and DRV_{CC} should be connected to each other, separately on each module (see Figures 56 and 66)—or, if powering DRV_{CC} from an auxiliary bias rail, then by applying the technique of Figure 51 to each module.

If MSP is used, only one V_{INGP} need be connected to the gate of MSP. The routing of MSP's source pins to the V_{INH} of all modules may be difficult to accomplish in layout without introducing significant loop area; it may be necessary then to use one MSP MOSFET on the input to each LTM4641 power stage for practical routing. Also, the connections of V_{OSNS}^+ and V_{OSNS}^- to multiple modules can be difficult to shield, in practice, so leaving provision for differential-mode filtering of the remote sense signal (C_{DM1}, C_{DM2}) local to each modules' remote-sense input pins is advisable.

Be aware that the loading of the paralleled remote sense amplifiers on the bussed feedback signal alters the equations for setting output voltage as follows.

When paralleling n modules, for $V_{OUT} \le 1.2V$, select R_{SET1A} not larger than that given by:

$$R_{SET1A} = R_{SET1B} = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet \left(\frac{8.2k\Omega}{n}\right) \quad (32)$$

For $V_{OUT} > 1.2V$, select R_{SET1A} not larger than that given by:

$$R_{SET1A} = R_{SET1B} = \frac{8.2k\Omega}{n} \quad (33)$$

Then, determine R_{SET2} by:

$$R_{SET2} = \frac{2 \bullet R_{SET1A}}{\frac{V_{OUT}}{0.6} - n \bullet \frac{R_{SET1A}}{8.2k\Omega} - 1} \quad (34)$$

The output voltage setting can be double-checked by:

$$V_{OUT} = 0.6V\left(1 + n \bullet \frac{R_{SET1A}}{8.2k\Omega} + \frac{2 \bullet R_{SET1A}}{R_{SET2}}\right) \quad (35)$$

The voltage on the V_{OSNS}^+ pins of the modules during regulation become:

$$V_{VOSNS+} = \left(\frac{0.6V}{\frac{8.2k\Omega}{n} \,||\, R_{SET1A} \,||\, R_{SET2}} + \frac{\Delta V_{GND}}{R_{SET1A}}\right) \bullet \left(R_{SET1A} \,||\, \frac{16.4k\Omega}{n}\right) \quad (36)$$

In multimodule parallel scenarios, $V_{OSNS}-$ and ΔV_{GND} are still given by Equations 12 and 13, respectively.

Lastly, be aware that the total charge current on the TRACK/SS net will be n • 1µA.

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1 θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2 $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3 θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4 θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 17; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4641, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4641 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-9 and JESD 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4641 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

The 6V, 3.3V and 1.5V power loss curves in Figures 18, 19 and 20 respectively can be used in coordination with the load current derating curves in Figures 21 to 42 for calculating an approximate θ_{JA} thermal resistance for the LTM4641 with various heat sinking and air flow conditions. These thermal resistances represent demonstrated

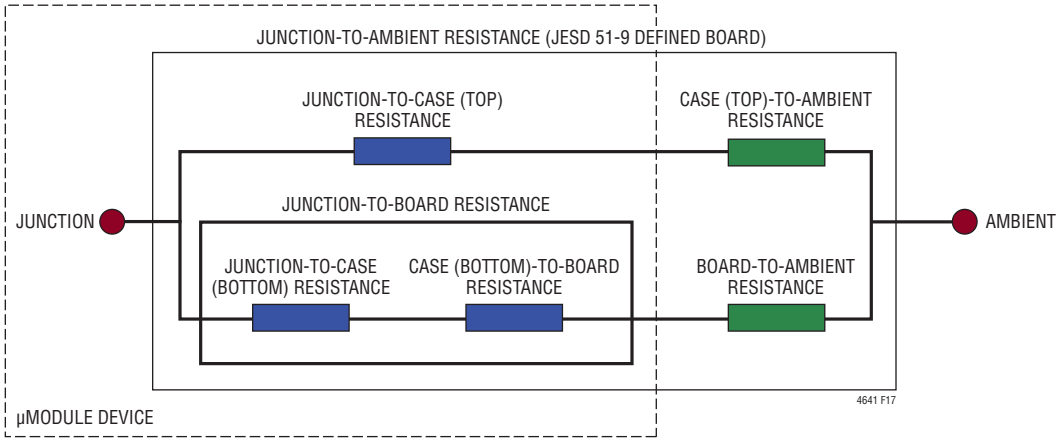


Figure 17. Graphical Representation of JESD51-12 Thermal Coefficients

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

performance of the LTM4641 on DC1543 hardware; a 4-layer FR4 PCB measuring 96mm × 87mm × 1.6mm using outer and inner copper weights of 2oz and 1oz, respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 3. (Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the output current starting at 10A and the ambient temperature at 40°C. The output voltages are 6V, 3.3V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The BGA heat sinks evaluated in Table 7 (and attached to the LTM4641 with thermally conductive adhesive tape listed in Table 8) yield very comparable performance in laminar airflow despite being visibly different in construction and form factor. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 38, the load current is derated to ~8A at ~81°C ambient with no air or heat sink and the power loss for this $36V_{IN}$ to $1.5V_{OUT}$ at $8A_{OUT}$ condition is ~3.1W. The 3.74W loss is calculated with the ~3.1W room temperature loss from the $36V_{IN}$ to $1.5V_{OUT}$ power loss curve at 8A (Figure 20), and the 1.205 multiplying factor at 81°C ambient (interpolating from Table 3). If the 81°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 39°C divided by 3.74W yields a thermal resistance, θ_{JA}, of 10.4°C/W—in good agreement with Table 6. Tables 4, 5 and 6 provide equivalent thermal resistances for 6V, 3.3V and 1.5V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 4, 5 and 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors.

Table 3. Power Loss Multiplicative Factors vs Ambient Temperature

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

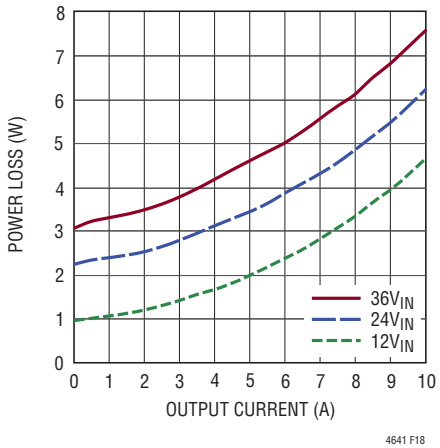


Figure 18. $6V_{OUT}$ Power Loss, f_{SW} = 660kHz at Full Load, FCB Tied to SGND

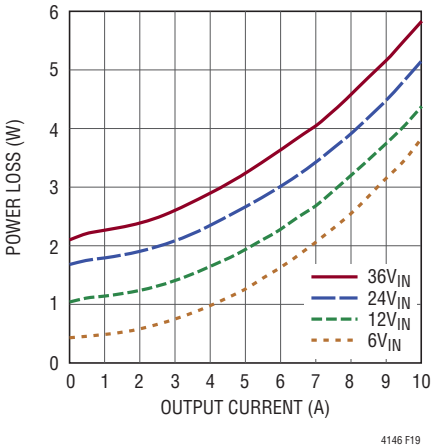


Figure 19. $3.3V_{OUT}$ Power Loss, f_{SW} = 360kHz at Full Load, FCB Tied to SGND

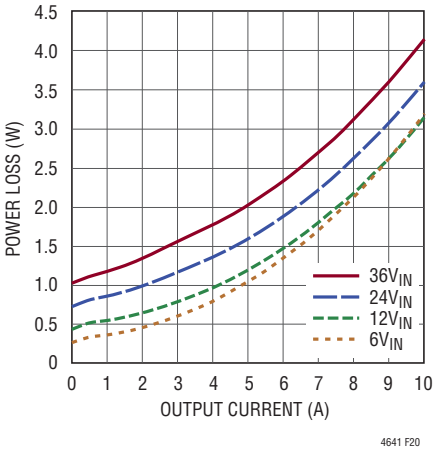


Figure 20. $1.5V_{OUT}$ Power Loss, f_{SW} = 315kHz at Full Load, FCB Tied to SGND

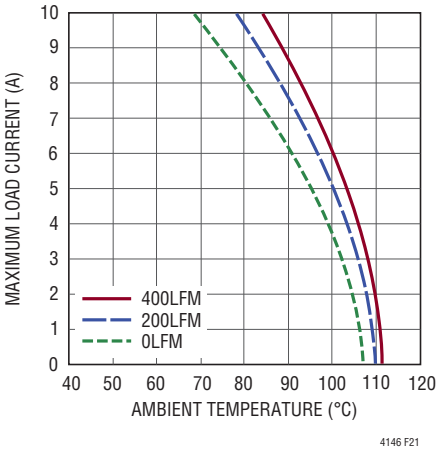


Figure 21. $12V_{IN}$ to $6V_{OUT}$, No Heat Sink, f_{SW} = 660kHz at Full Load

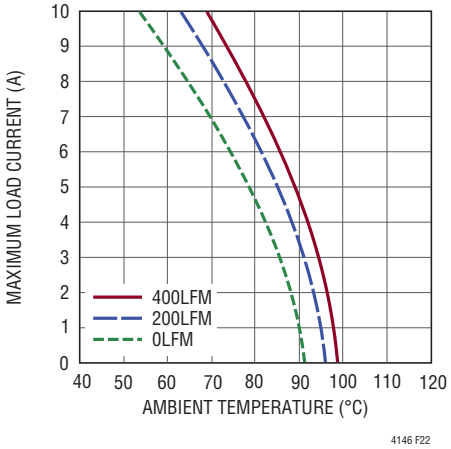


Figure 22. $24V_{IN}$ to $6V_{OUT}$, No Heat Sink, f_{SW} = 660kHz at Full Load

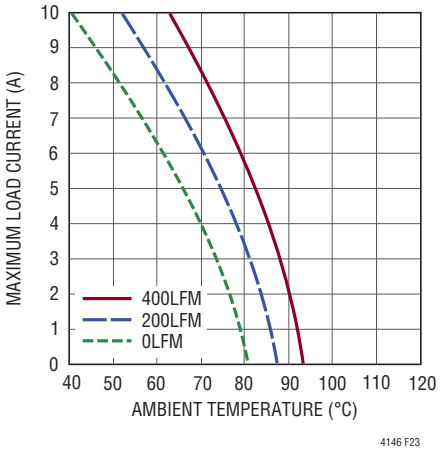


Figure 23. $36V_{IN}$ to $6V_{OUT}$, No Heat Sink, f_{SW} = 660kHz at Full Load

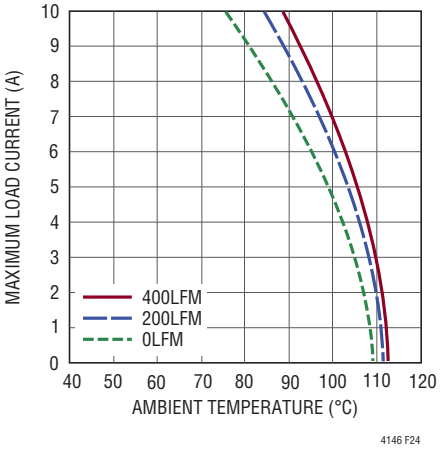


Figure 24. $12V_{IN}$ to $6V_{OUT}$ with Heat Sink, f_{SW} = 660kHz at Full Load

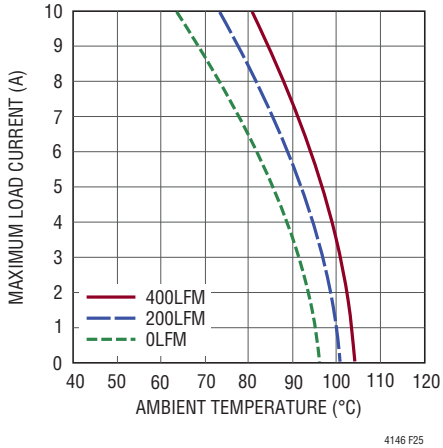


Figure 25. $24V_{IN}$ to $6V_{OUT}$ with Heat Sink, f_{SW} = 660kHz at Full Load

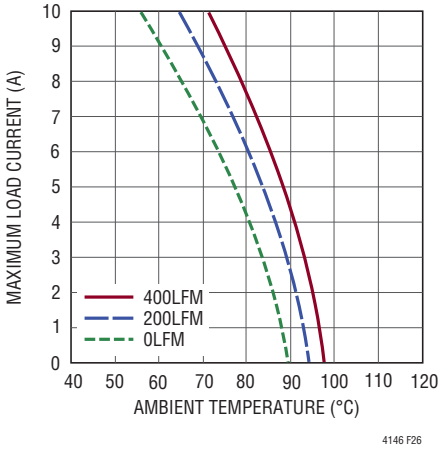


Figure 26. $36V_{IN}$ to $6V_{OUT}$ with Heat Sink, f_{SW} = 660kHz at Full Load

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

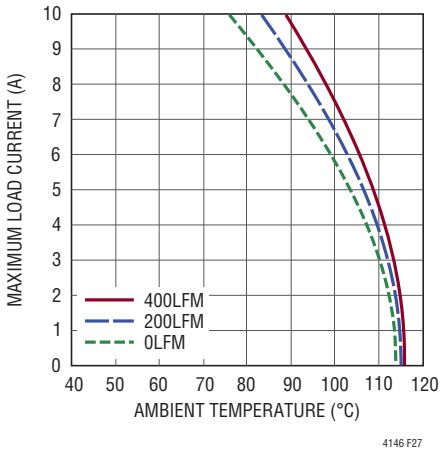


Figure 27. $6V_{IN}$ to $3.3V_{OUT}$ No Heat Sink, f_{SW} = 360kHz at Full Load

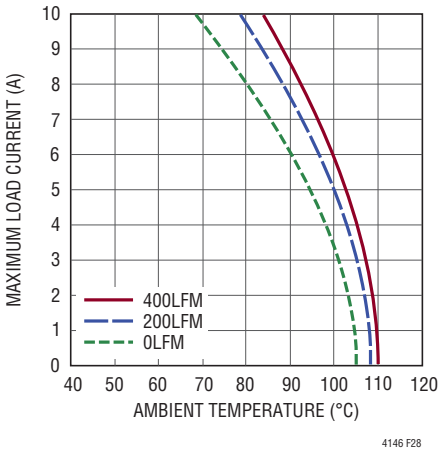


Figure 28. $12V_{IN}$ to $3.3V_{OUT}$ No Heat Sink, f_{SW} = 360kHz at Full Load

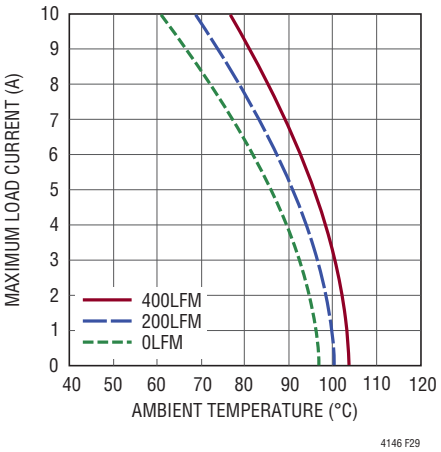


Figure 29. $24V_{IN}$ to $3.3V_{OUT}$ No Heat Sink, f_{SW} = 360kHz at Full Load

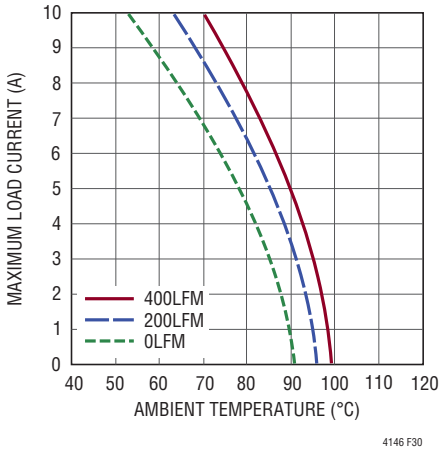


Figure 30. $36V_{IN}$ to $3.3V_{OUT}$, No Heat Sink, f_{SW} = 360kHz at Full Load

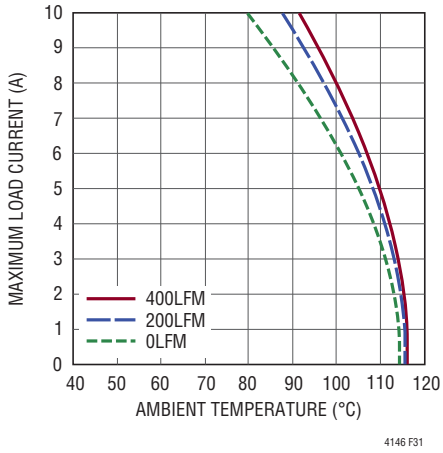


Figure 31. $6V_{IN}$ to $3.3V_{OUT}$, with Heat Sink, f_{SW} = 360kHz at Full Load

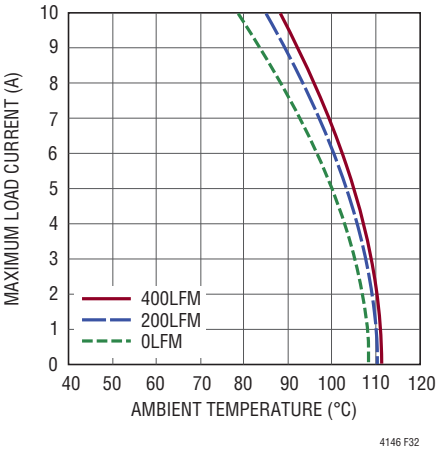


Figure 32. $12V_{IN}$ to $3.3V_{OUT}$, with Heat Sink, f_{SW} = 360kHz at Full Load

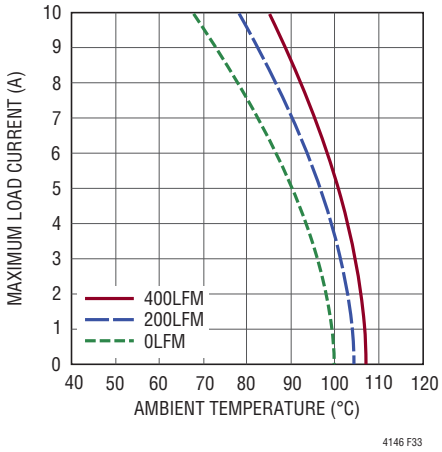


Figure 33. $24V_{IN}$ to $3.3V_{OUT}$ with Heat Sink, f_{SW} = 360kHz at Full Load

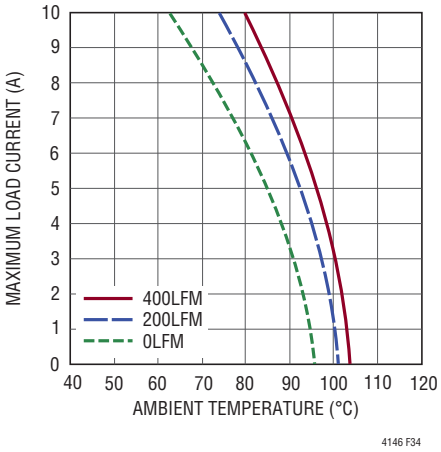


Figure 34. $36V_{IN}$ to $3.3V_{OUT}$ with Heat Sink, f_{SW} = 360kHz at Full Load

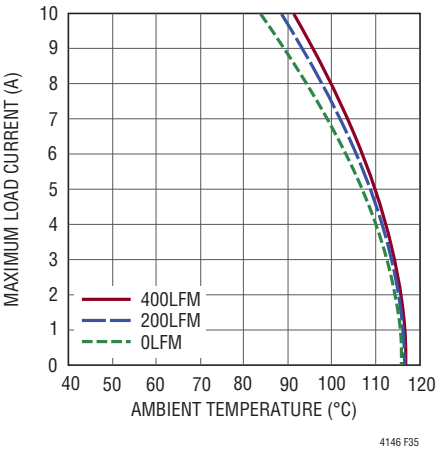


Figure 35. $6V_{IN}$ to $1.5V_{OUT}$ No Heat Sink, f_{SW} = 315kHz at Full Load

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

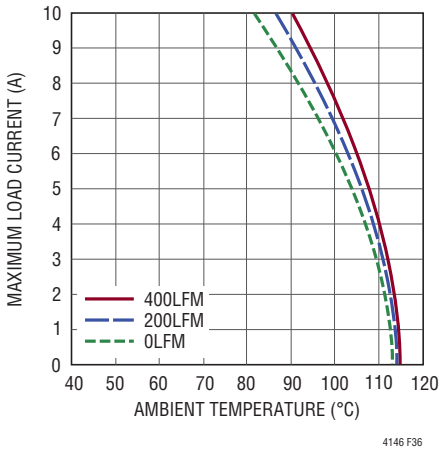


Figure 36. $12V_{IN}$ to $1.5V_{OUT}$ No Heat Sink, f_{SW} = 315kHz at Full Load

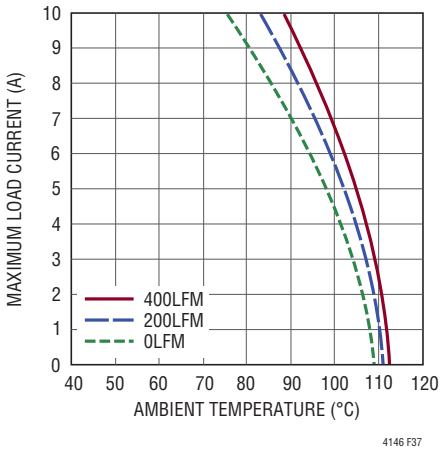


Figure 37. $24V_{IN}$ to $1.5V_{OUT}$ No Heat Sink, f_{SW} = 315kHz at Full Load

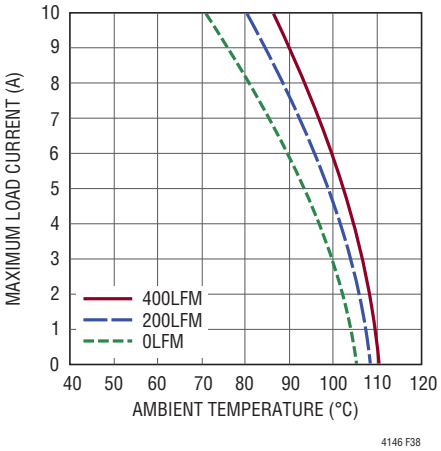


Figure 38. $36V_{IN}$ to $1.5V_{OUT}$ No Heat Sink, f_{SW} = 315kHz at Full Load

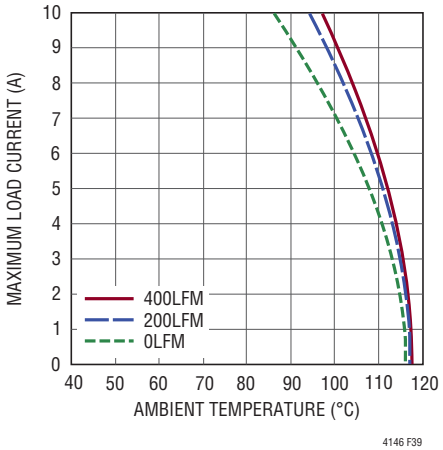


Figure 39. $6V_{IN}$ to $1.5V_{OUT}$, with Heat Sink, f_{SW} = 315kHz at Full Load

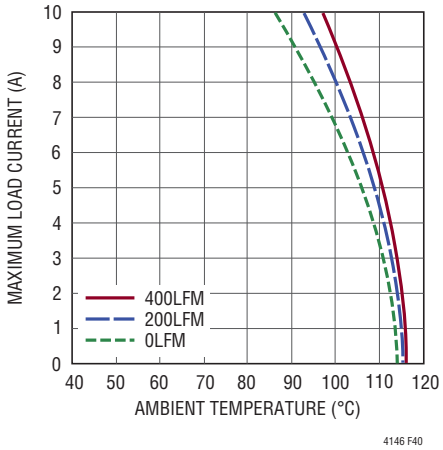


Figure 40. $12V_{IN}$ to $1.5V_{OUT}$, with Heat Sink, f_{SW} = 315kHz at Full Load

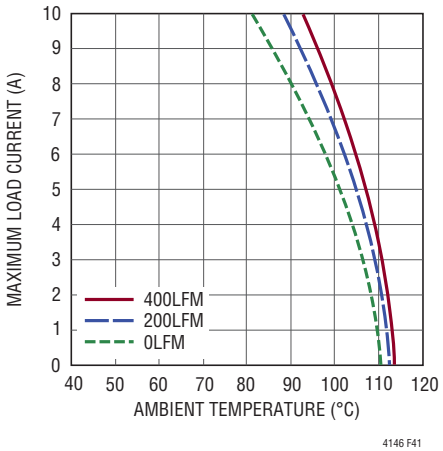


Figure 41. $24V_{IN}$ to $1.5V_{OUT}$, with Heat Sink, f_{SW} = 315kHz at Full Load

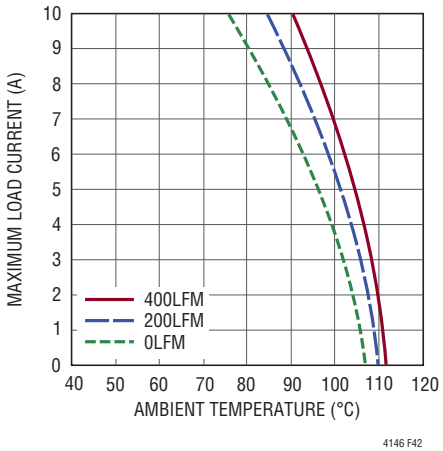


Figure 42. $36V_{IN}$ to $1.5V_{OUT}$ with Heat Sink, f_{SW} = 315kHz at Full Load

APPLICATIONS INFORMATION—THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

Table 4. 6V Output, Switching Frequency Nominally 660kHz at Full Load

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 21 to Figure 23	12V, 24V, 36V	Figure 18	0	None	10.1
Figure 21 to Figure 23	12V, 24V, 36V	Figure 18	200	None	8.2
Figure 21 to Figure 23	12V, 24V, 36V	Figure 18	400	None	6.8
Figure 24 to Figure 26	12V, 24V, 36V	Figure 18	0	BGA Heat Sink	8.1
Figure 24 to Figure 26	12V, 24V, 36V	Figure 18	200	BGA Heat Sink	6.5
Figure 24 to Figure 26	12V, 24V, 36V	Figure 18	400	BGA Heat Sink	5.5

Table 5. 3.3V Output, Switching Frequency Nominally 360kHz at Full Load

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 27 to Figure 30	6V, 12V, 24V, 36V	Figure 19	0	None	10.4
Figure 27 to Figure 30	6V, 12V, 24V, 36V	Figure 19	200	None	8.4
Figure 27 to Figure 30	6V, 12V, 24V, 36V	Figure 19	400	None	7.1
Figure 31 to Figure 34	6V, 12V, 24V, 36V	Figure 19	0	BGA Heat Sink	8.6
Figure 31 to Figure 34	6V, 12V, 24V, 36V	Figure 19	200	BGA Heat Sink	6.8
Figure 31 to Figure 34	6V, 12V, 24V, 36V	Figure 19	400	BGA Heat Sink	5.8

Table 6. 1.5V Output, Switching Frequency Nominally 315kHz at Full Load

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 35 to Figure 38	6V, 12V, 24V, 36V	Figure 20	0	None	10.3
Figure 35 to Figure 38	6V, 12V, 24V, 36V	Figure 20	200	None	8.4
Figure 35 to Figure 38	6V, 12V, 24V, 36V	Figure 20	400	None	7.2
Figure 39 to Figure 42	6V, 12V, 24V, 36V	Figure 20	0	BGA Heat Sink	9.0
Figure 39 to Figure 42	6V, 12V, 24V, 36V	Figure 20	200	BGA Heat Sink	7.0
Figure 39 to Figure 42	6V, 12V, 24V, 36V	Figure 20	400	BGA Heat Sink	5.8

Table 7. Heat Sink Vendors (with Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Wakefield Engineering	LTN20069	www.wakefield.com
Aavid Thermalloy	375424B00034G	www.aavid.com

Table 8. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

APPLICATIONS INFORMATION—OUTPUT CAPACITANCE TABLE

Table 9. Transient Performance (Typical Values) vs Recommended Output Capacitance. Figure 45 and Figure 46 Circuits

	$C_{OUT(MLCC)}$		$C_{OUT(BULK)}$	
V_{OUT}	**VENDOR**	**PART NUMBER**	**VENDOR**	**PART NUMBER**
≤ 3.3V	AVX	12106D107MAT2A (100µF, 6.3V, 1210 Case Size) 12066D226MAT2A (22µF, 6.3V, 1206 Case Size)	Sanyo POSCAP	6TPE680MI (680µF, 6.3V, 18mΩ ESR, D4 Case Size)
	Taiyo Yuden	JMK325BJ107MM-T (100µF, 6.3V, 1210 Case Size) JMK316BJ226ML-T (22µF, 6.3V, 1206 Case Size)		
	TDK	C3225X5R0J107MT (100µF, 6.3V, 1210 Case Size) C3216X5R0J226MT (22µF, 6.3V, 1206 Case Size)		
> 3.3V	AVX	1206YD226MAT2A (22µF, 16V, 1206 Case Size)	Sanyo POSCAP	10TPF150ML (150µF, 10V, 15mΩ ESR, D3L Case Size)
	Taiyo Yuden	LMK316BJ476ML-T (47µF, 10V, 1206 Case Size) EMK316BJ226ML-T (22µF, 16V, 1206 Case Size)		
	TDK	C3216X5R1A476M (47µF, 10V, 1206 Case Size) C3216X5R1C226M (22µF, 16V, 1206 Case Size)		

V_{OUT} (V)	V_{IN} (V)	R_{fSET} (MΩ)	R_{SET1A}, R_{SET1B} (kΩ)	R_{SET2} (kΩ)	C_{IN} (CERAMIC)	C_{IN}* (BULK)	C_{OUT2} (CERAMIC)	C_{OUT1} (BULK)	C_{FFA}, C_{FFB}	LOAD STEP SLEW RATE (A/µs)	TRANSIENT DROOP, 0A TO 5A LOAD STEP (mV)	TRANSIENT, PEAK-TO-PEAK, 0A TO 5A TO 0A STEP (mV_{PK-PK})	RECOVERY TIME (µs)
0.9	5, 12, 24, 36	0.931	4.12	–	2 × 10µF	100µF	3 × 22µF	680µF	–	5	60	130	25
0.9	5, 12, 24, 36	0.931	4.12	–	2 × 10µF	100µF	4 × 100µF	–	–	5	60	140	25
1	5, 12, 24, 36	1.00	5.49	–	2 × 10µF	100µF	3 × 22µF	680µF	–	5	65	135	25
1	5, 12, 24, 36	1.00	5.49	–	2 × 10µF	100µF	4 × 100µF	–	–	5	70	150	25
1.2	5, 12, 24, 36	1.13	8.2	–	2 × 10µF	100µF	3 × 22µF	680µF	–	5	70	140	25
1.2	5, 12, 24, 36	1.13	8.2	–	2 × 10µF	100µF	4 × 100µF	–	–	5	80	170	30
1.5	5, 12, 24, 36	1.43	8.2	33.2	2 × 10µF	100µF	3 × 22µF	680µF	–	5	75	155	30
1.5	5, 12, 24, 36	1.43	8.2	33.2	2 × 10µF	100µF	4 × 100µF	–	220pF	5	90	190	30
1.8	5, 12, 24, 36	2.00	8.2	16.5	2 × 10µF	100µF	3 × 22µF	680µF	–	5	80	170	40
1.8	5, 12, 24, 36	2.00	8.2	16.5	2 × 10µF	100µF	3 × 100µF	–	220pF	5	100	215	30
2.5	5, 12, 24, 36	5.76	8.2	7.5	2 × 10µF	100µF	3 × 22µF	680µF	–	5	100	230	50
2.5	5, 12, 24, 36	5.76	8.2	7.5	2 × 10µF	100µF	3 × 100µF	–	220pF	5	140	290	30
3.3	5, 12, 24, 36	–	8.2	4.7	2 × 10µF	100µF	3 × 22µF	680µF	–	5	140	275	60
3.3	5, 12, 24, 36	–	8.2	4.7	2 × 10µF	100µF	3 × 100µF	–	100pF	5	200	420	30
5	12, 24, 36	–	8.2	2.61	2 × 10µF	100µF	2 × 22µF	150µF	220pF	5	220	450	50
5	12, 24, 36	–	8.2	2.61	2 × 10µF	100µF	3 × 47µF	–	100pF	5	250	570	30
6	12, 24, 36	–	8.2	2.05	2 × 10µF	100µF	2 × 22µF	150µF	220pF	5	240	500	55
6	12, 24, 36	–	8.2	2.05	2 × 10µF	100µF	3 × 47µF	–	100pF	5	300	660	30

*Bulk Capacitance is optional if V_{IN} has very low input impedance.

APPLICATIONS INFORMATION—SAFETY AND LAYOUT GUIDANCE

Safety Considerations

The LTM4641 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If fusing is required, a slow blow fuse with a rating twice the maximum input current needs to be provided. The LTM4641 supports overcurrent protection and two kinds of overvoltage protection (see the Power Good Indicator and Latching Output Overvoltage Protection section).

Layout Checklist/Example

The high integration of LTM4641 makes the PCB board layout very straightforward. To optimize its electrical and thermal performance, some layout considerations are necessary. Figure 43 and Figure 44 show recommended layouts for the circuits shown in Figure 45 and Figure 46, respectively.

- Refer to the following document for device land pattern and stencil design: http://www.linear.com/docs/40146.
- The gerber file for demo board DC1543 can be downloaded at http://www.linear.com/demo
- Use a solid copper GND plane directly underneath the module. This will help form the return path electrical connections to the input source and output load. It will also provide a thermal path for removing heat from the BGA package and minimize junction temperature rise of the LTM4641 for a given application. For consistent ripple and noise from application to application, connect the output GND plane (the one that conducts load side return current back to the module) and the input GND plane (the one that conducts module return current back to the input source) underneath the module, only.
- Use large PCB copper areas for high current paths, including V_{INH} and V_{OUT}.
- Place high frequency ceramic input and output capacitors next to the V_{INH}, GND and V_{OUT} pins to minimize high frequency noise. V_{INH} exception: If MSP is used, (1) place MSP as close to the V_{INH} pins of the LTM4641 as possible and (2) bypass the drain of MSP—and *not* V_{INH}—to GND pins of the LTM4641. Only one or two high frequency MLCCs ($C_{OUT(MLCC)}$) need be placed directly next to the V_{OUT} and GND pins of the LTM4641, to minimize high frequency noise close to the source. The majority of $C_{OUT(MLCC)}$ should be located close to the load to provide high quality bypassing.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly under any pads, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connecting to signal pins. Components connecting to SGND should be placed as close to the module as possible and routed with minimum trace lengths and trace widths, for best noise immunity.
- Note that there are two clusters of SGND pins on the module: one, formed by Pins A1-A3, B1-B3, C1-C4 (A1-quadrant); and a second formed by Pins K1, K3, L3, and M1-M3 (M1-quadrant). It is good PCB design practice to provide a copper plane connecting all A1-quadrant SGND pins together and another plane connecting all M1-quadrant SGND pins together. It is *not* necessary to connect these two clusters of SGND copper planes to each other in the PCB layout, because all SGND pins are electrically connected to each other internal to the module.
- Do *not* connect the any SGND pins or SGND plane(s) to the GND plane; the electrical star connection is made internal to the module.
- For parallel module operation, see the Multimodule Parallel Operation section for a list of interconnecting pins across paralleled modules. Circuit Figures 56 and 66 show four and two LTM4641 devices operating in parallel, respectively. Route signal-level (non-power) nets on an internal layer, with GND planes overlapping signal routes to shield them from noise. It is even more effective to surround module-to-module signal connections on the internal layer containing the signal routes with adjacent GND planes or routes, and periodically "punching-through" GND via connections to GND plane shields on adjacent layers. This practice forms the equivalent of a "coaxial cable" structure within the PCB, and is highly effective at shielding sensitive signals from noise sources. Maintain differential routing of the $V_{OSNS}^{+}/V_{OSNS}^{-}$ pin pair.

APPLICATIONS INFORMATION—SAFETY AND LAYOUT GUIDANCE

- Place all feedback components as close to the module as possible, giving layout priority first to capacitors C_{FFA}, C_{FFB}, C_{CMA}, C_{CMB} and C_{DM} (if used)—followed next by R_{SET1A}, R_{SET1B} and R_{SET2} (if used). See Figure 5 in the Applications Information section and Figure 64 in Appendix D for more details. Maintain differential routing of the remote-sense lines between the load and the module. Form a "coaxial cable" structure that surrounds the remote-sense lines with GND potential within the PCB, to the extent that layout permits. See an example of routing the VOUT/GND remote-sense pin pair in Layer 3 of DC1543.
- To facilitate stuffing verification, and test and debug activities, consider routing control signals of the LTM4641 with short traces to localized test points, test pads or test vias—as PCB layout space permits. Both in-house and contract manufacturers enjoy gaining electrical access to all non low impedance (≥10Ω) pins of an IC or µModule regulator to improve in-circuit test (ICT) coverage.

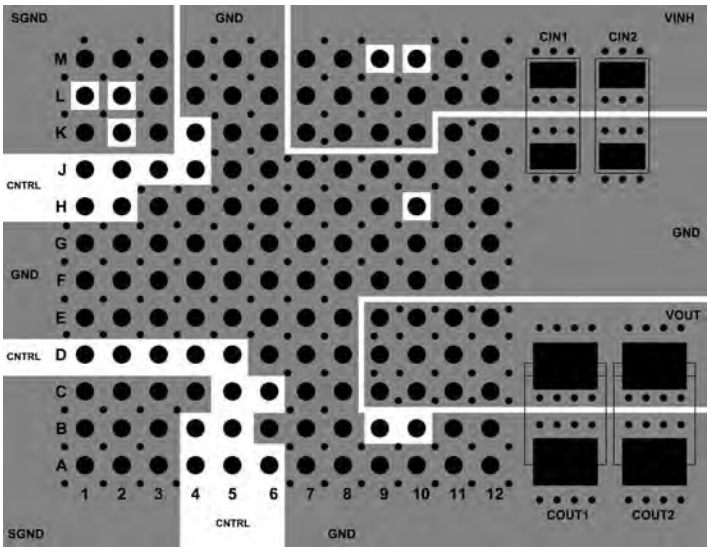


Figure 43. Recommended PCB Layout, Figure 45 Circuit. View of the LTM4641 from Top of Package

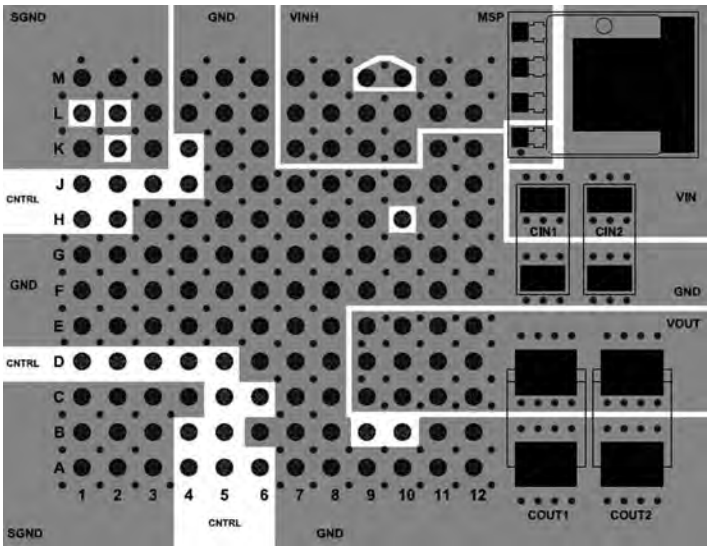


Figure 44. Recommended PCB Layout, Figure 46 Circuit. View of the LTM4641 from Top of Package

TYPICAL APPLICATIONS

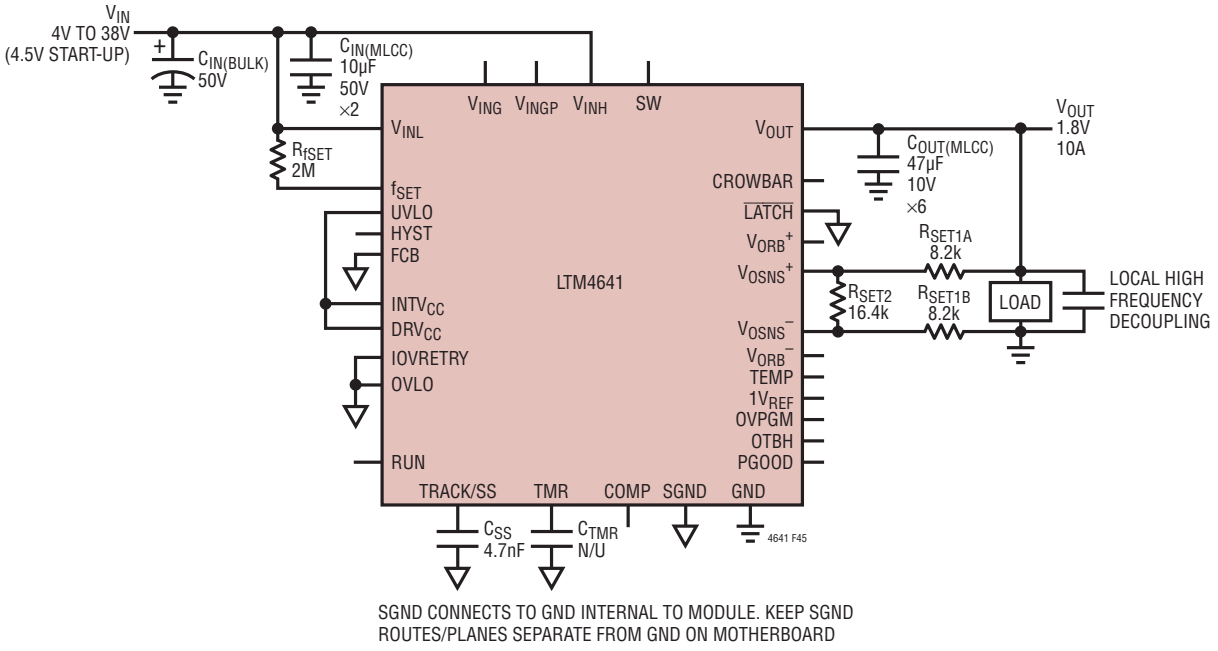


Figure 45. 4V_{IN} to 38V_{IN}, LTM4641 Basic Configuration, 1.8V Output at 10A

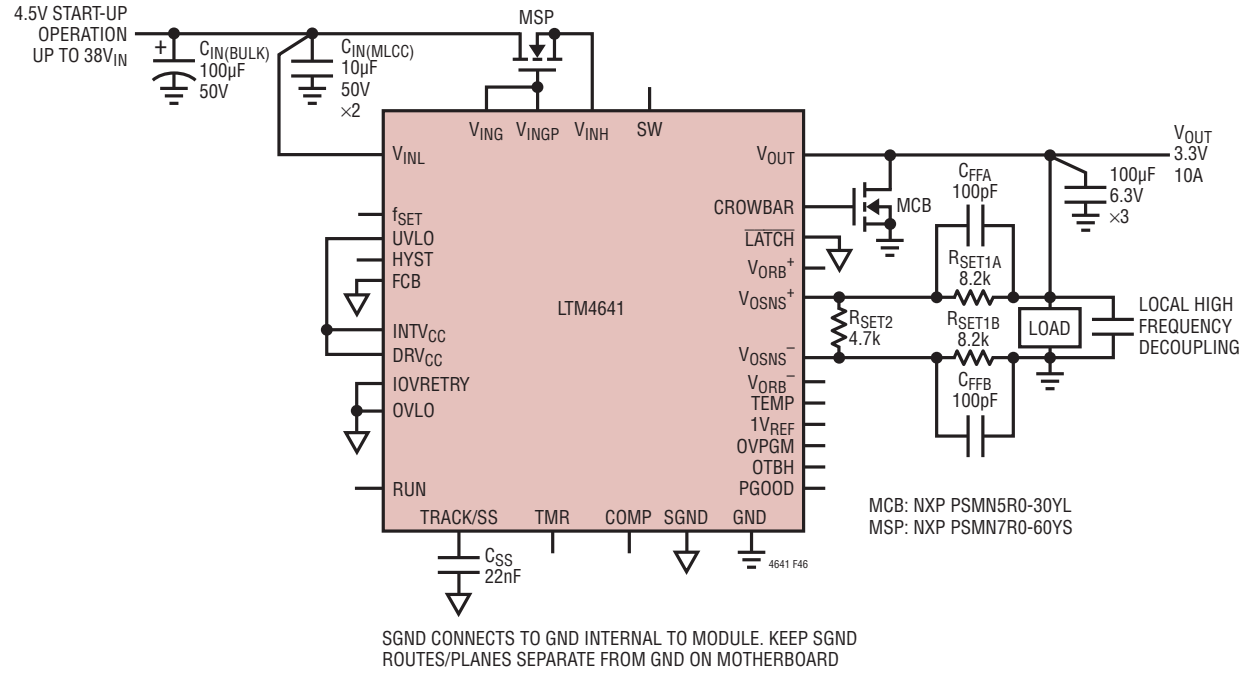


Figure 46. LTM4641 Delivering 3.3V Output at 10A, and Providing Robust Output Overvoltage Protection from up to 38V_{IN}. Dropout Operation May Occur Below 4.8V_{IN}. See Figure 11 to Implement Custom UVLO Rising/Falling Settings to Avoid Dropout Operation

TYPICAL APPLICATIONS

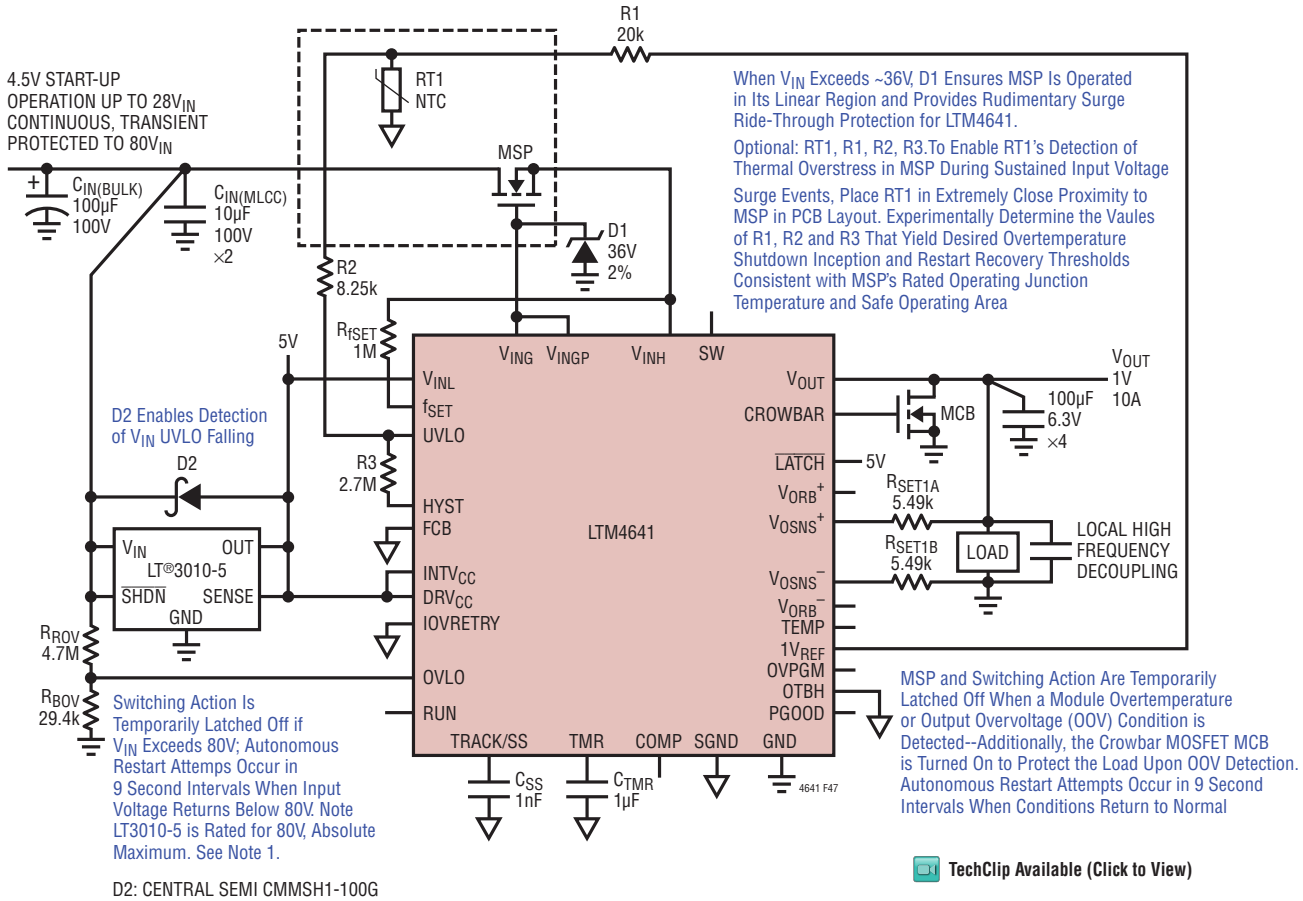


Figure 47. LTM4641 Generating 1V Output at 10A, Surge Protected up to $80V_{IN}$ Transients. Start-Up and Shutdown Waveforms with TMR = $INTV_{CC}$ Shown In Figure 2

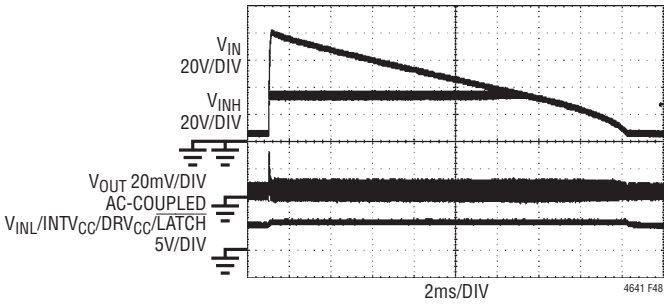


Figure 48. Oscilloscope Snap-Shot of Figure 47 Circuit Riding Through $80V_{IN}$ Transient While Delivering $1V_{OUT}$ at 10A to the Load

TYPICAL APPLICATIONS

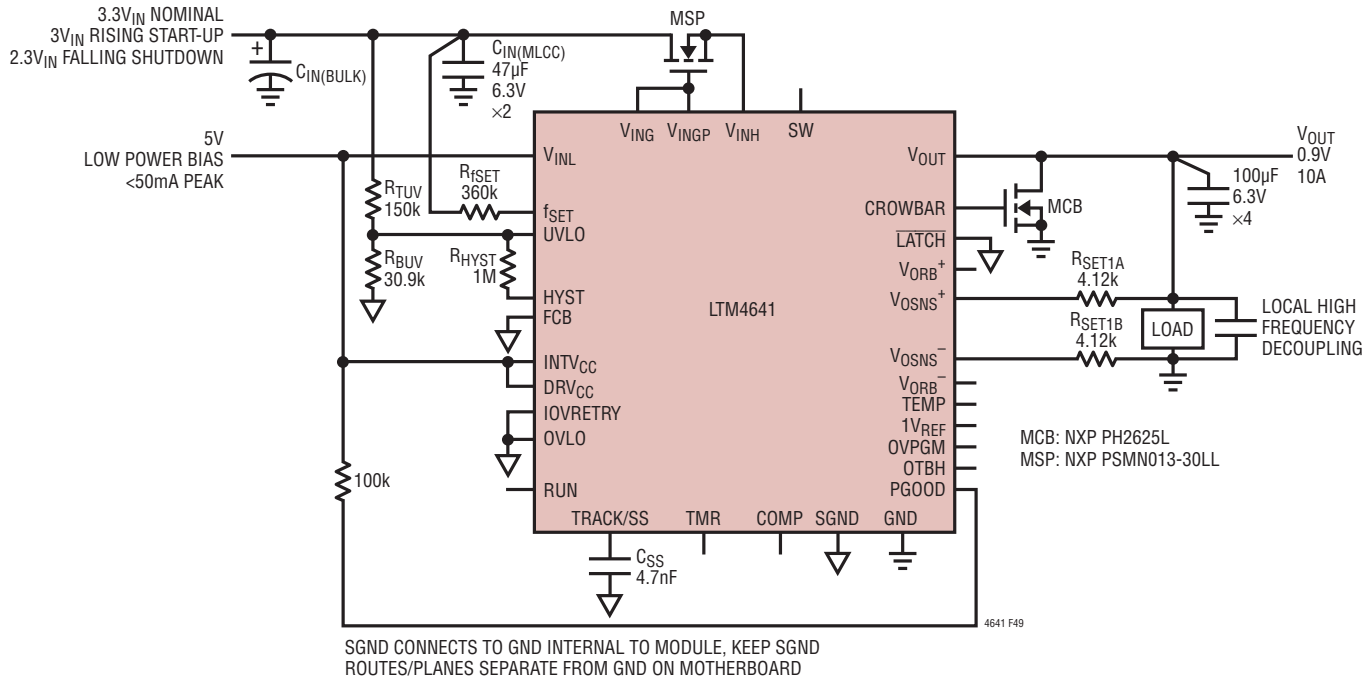


Figure 49. LTM4641 Producing $0.9V_{OUT}$ at 10A, from $3.3V_{IN}$, and Providing Advanced Output Overvoltage Protection. V_{INL}, $INTV_{CC}$, and DRV_{CC} Biased from a Low Power Auxiliary 5V Rail

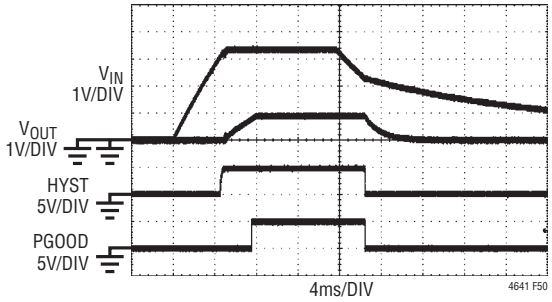


Figure 50. Oscilloscope Snap-Shot of Figure 49 Circuit, 2Ω Load on V_{OUT}. $3.3V_{IN}$ Applied Briefly to Highlight UVLO Rising and Falling Thresholds

TYPICAL APPLICATIONS

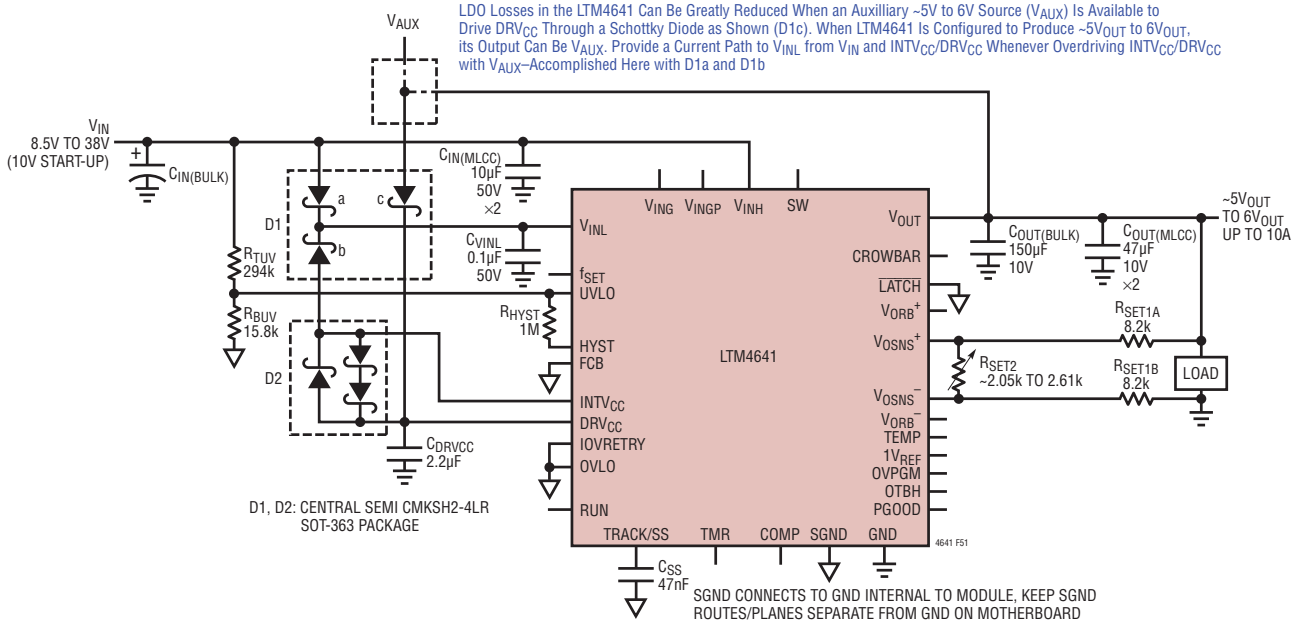


Figure 51. Over-Driving $INTV_{CC}/DRV_{CC}$ to Reduce V_{INL}-to-$INTV_{CC}$ Linear Regulator Losses (cf. Figures 52 to 54)

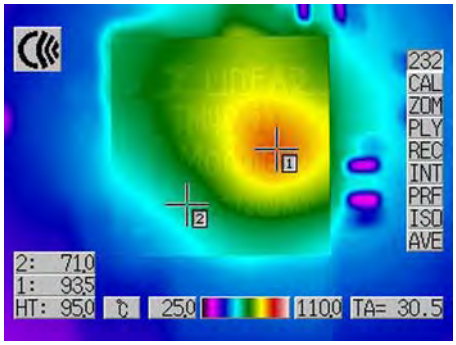


Figure 52. Thermal Image of U1 from Figure 51 Circuit. Delivering $5V_{OUT}$ at 10A from $36V_{IN}$, with $INTV_{CC}$ Connected to DRV_{CC} and D1c = Open and D2 = Open. T_A = 25°C, Bench Testing, No Airflow

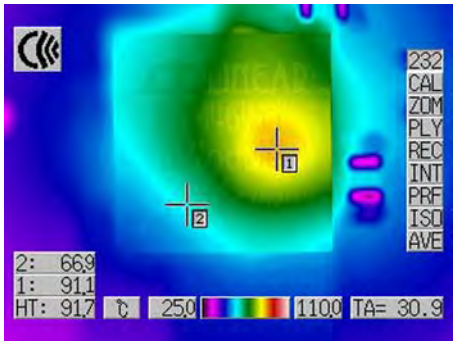


Figure 54. Thermal Image of U1 from Figure 51 Circuit. Delivering $5V_{OUT}$ at 10A from $36V_{IN}$, with $5V_{OUT}$ Feeding $INTV_{CC}/DRV_{CC}$ Through D1c Diode. T_A = 25°C, Bench Testing, No Airflow

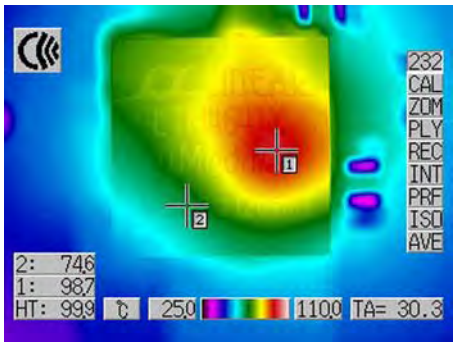


Figure 53. Thermal Image of U1 from Figure 51 Circuit. Delivering $6V_{OUT}$ at 10A from $36V_{IN}$, with $INTV_{CC}$ Connected to DRV_{CC} and D1c = Open and D2 = Open. T_A = 25°C, Bench Testing, No Airflow

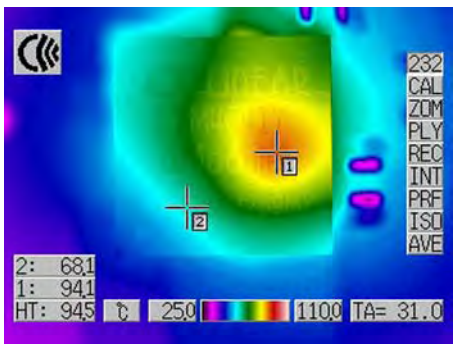


Figure 55. Thermal Image of U1 from Figure 51 Circuit. Delivering $6V_{OUT}$ at 10A from $36V_{IN}$, with $6V_{OUT}$ Feeding $INTV_{CC}/DRV_{CC}$ Through D1c Diode. T_A = 25°C, Bench Testing, No Airflow

TYPICAL APPLICATIONS

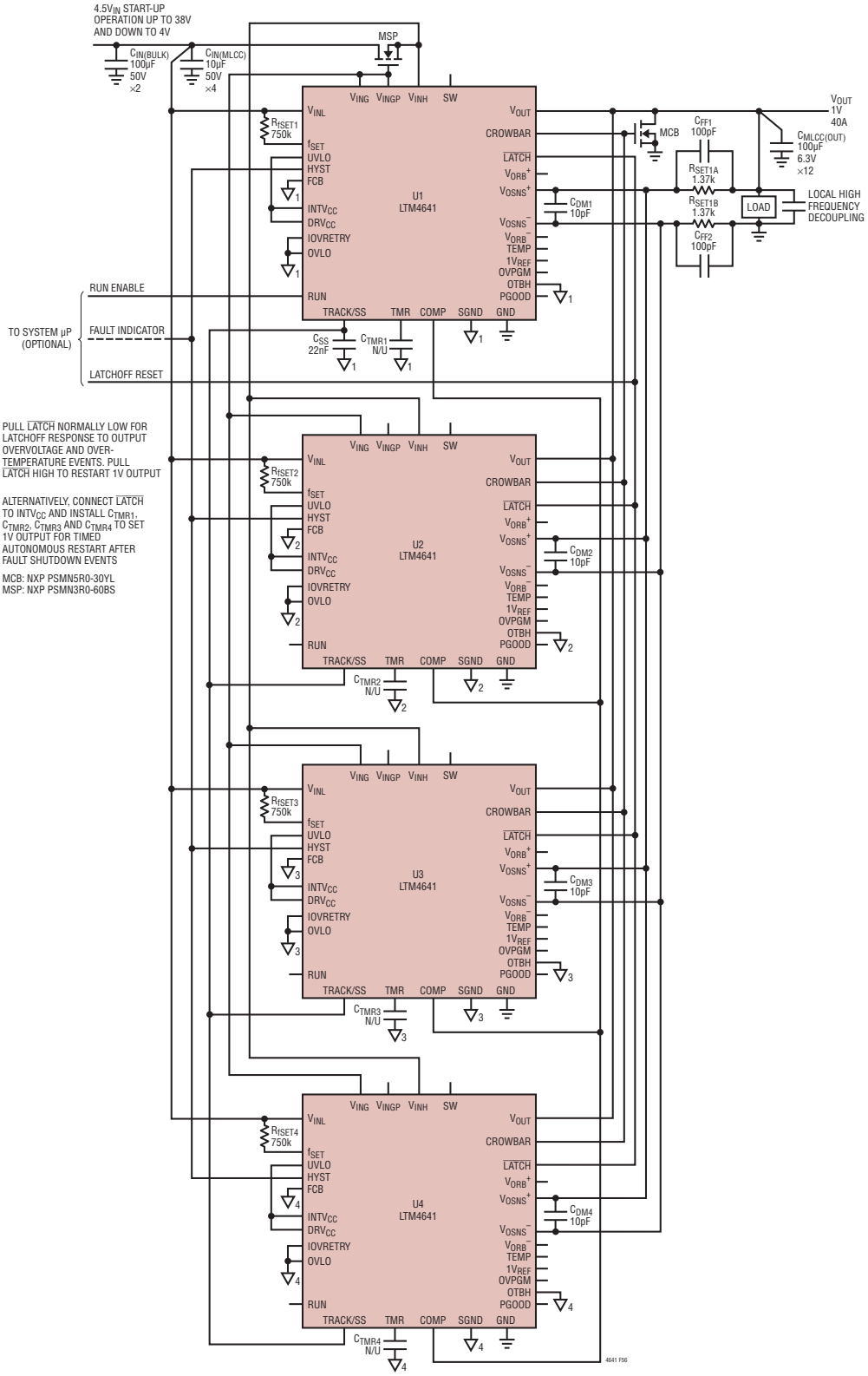


Figure 56: 1V, 40A Fault-Protected Load Powered by Four Parallel LTM4641—from Up to 38V_{IN}. cf. Figure 57

TYPICAL APPLICATIONS

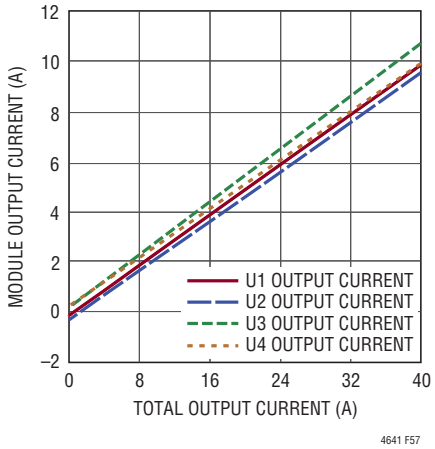


Figure 57: Current-Sharing Performance of Four Paralleled LTM4641. Figure 56 Circuit, Operating at 28V_{IN}

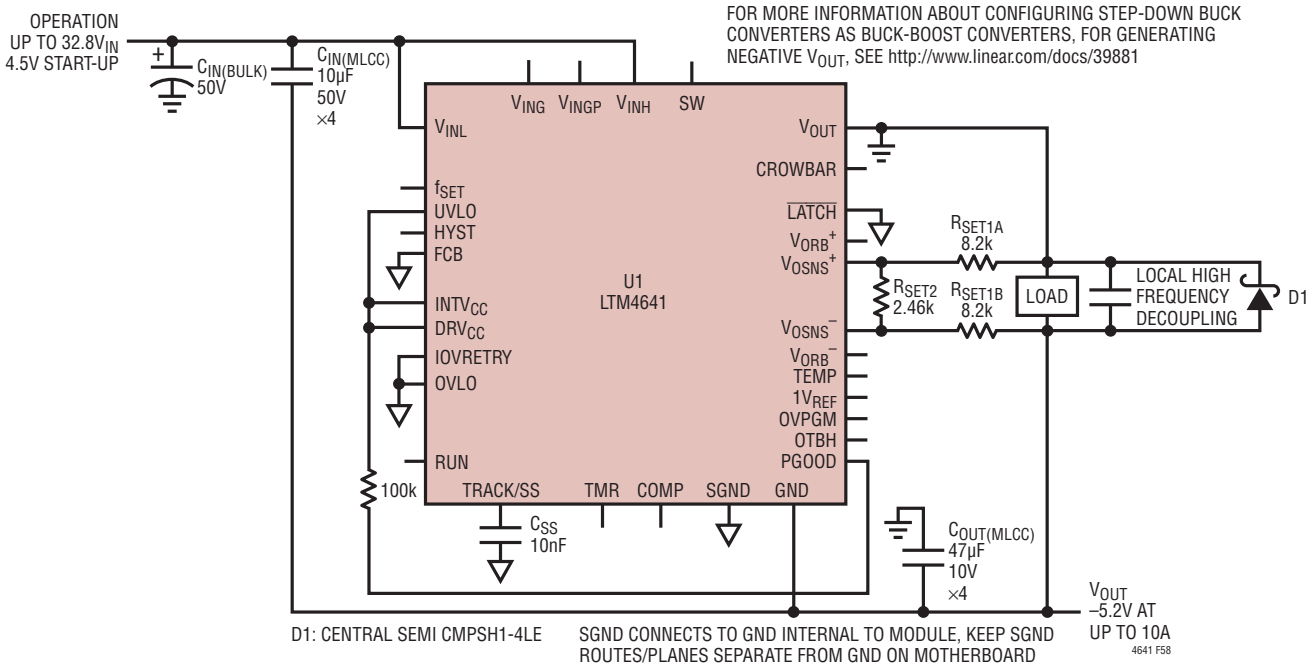


Figure 58. Negative Output Application. Delivering –5.2V_{OUT} at Up to 10A, from Up to 32.8V_{IN}. cf. Figure 59

TYPICAL APPLICATIONS

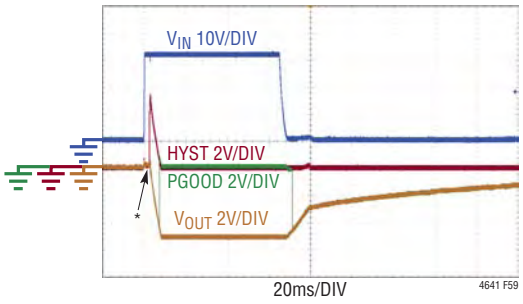


Figure 59. Pulsed Application of V_{IN}. Figure 58 Circuit with 500Ω Load. *Ultralow V_F of D1 Minimizes V_{OUT} Overshoot Upon Energization

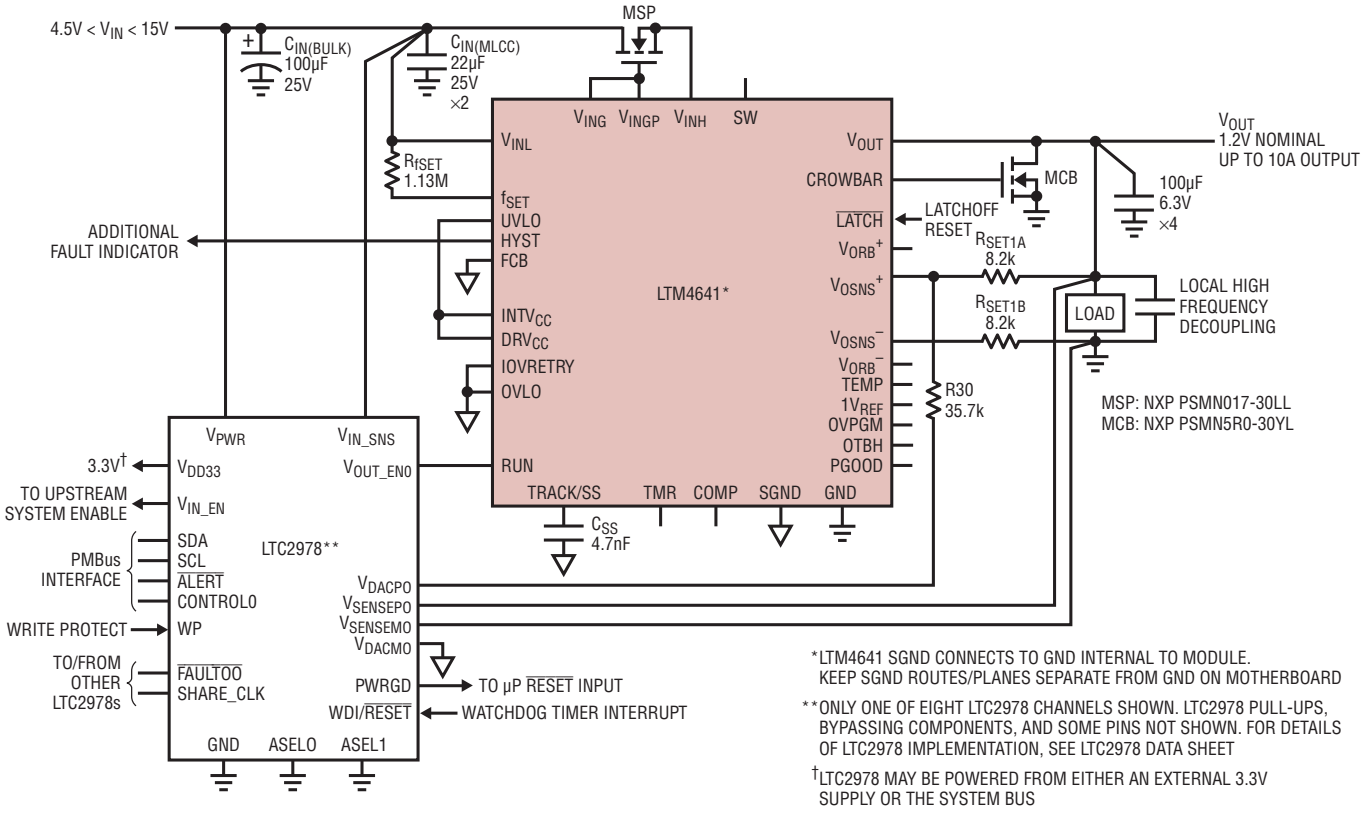
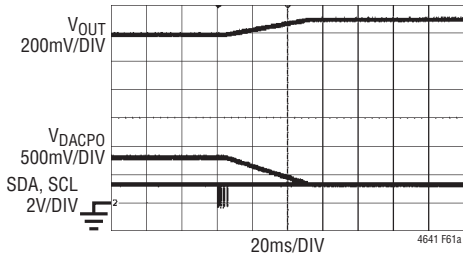
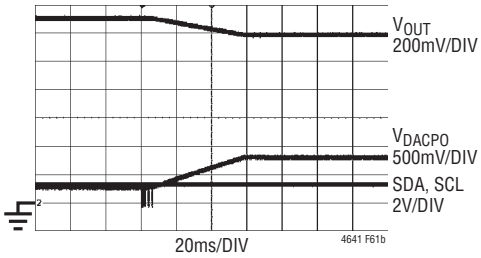


Figure 60. Fault-Protected Load with Power Supply Management. LTM4641's Fast Output Overvoltage Latchoff Trip Threshold Remains Consistently 11% Above LTC2978-Commanded Target V_{OUT}, Even as V_{OUT} is Margined Via I^2C

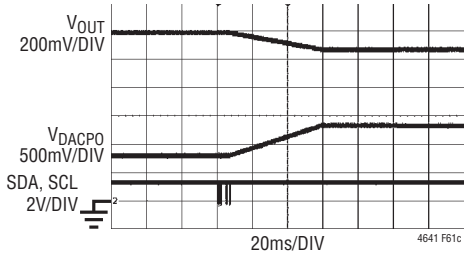
TYPICAL APPLICATIONS



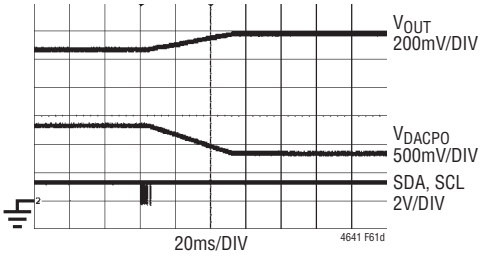
(61a) PMBus OPERATION (Reg. 0x01): 0x80 → 0xA8 (Margin High)



(61b) PMBus OPERATION (Reg. 0x01): 0xA8 → 0x80 (Margin Off)



(61c) PMBus OPERATION (Reg. 0x01): 0x80 → 0x98 (Margin Low)



(61d) PMBus OPERATION (Reg. 0x01): 0x98 → 0x80 (Margin Off)

Figure 61. LTM4641's V_{OUT} Margined High/Low by LTC2978 Via I^2C Commands. Figure 60 Circuit. $12V_{IN}$. VOUT_COMMAND (0x21) = 1.20V, VOUT_MARGIN_HIGH (0x25) = 1.32V, VOUT_MARGIN_LOW (0x26) = 1.08V

APPENDICES

Appendix A. Functional Block Diagram and Features Quick Reference Guide

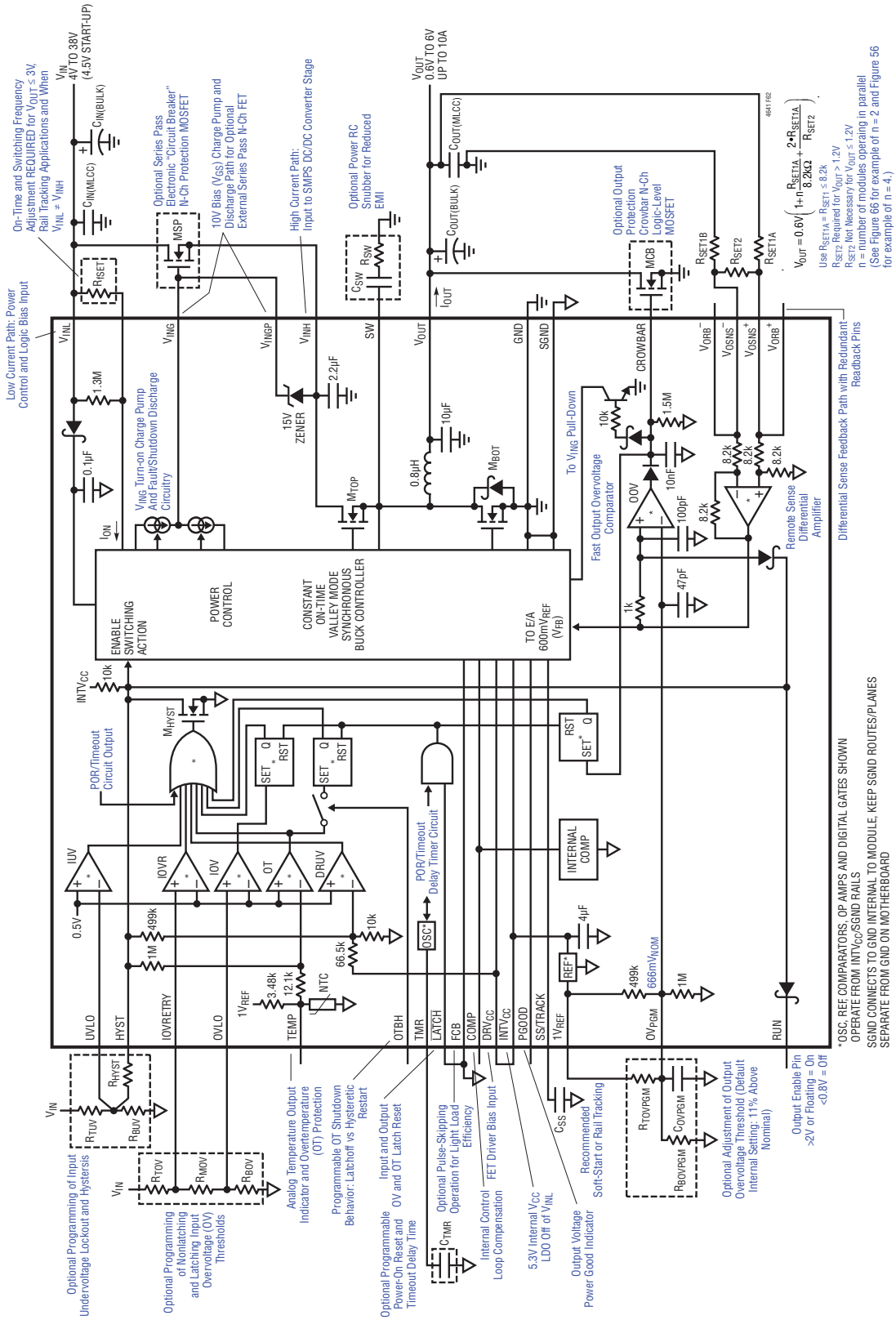


Figure 62. Functional Block Diagram

APPENDICES

Appendix B. Start-Up/Shutdown State Diagram

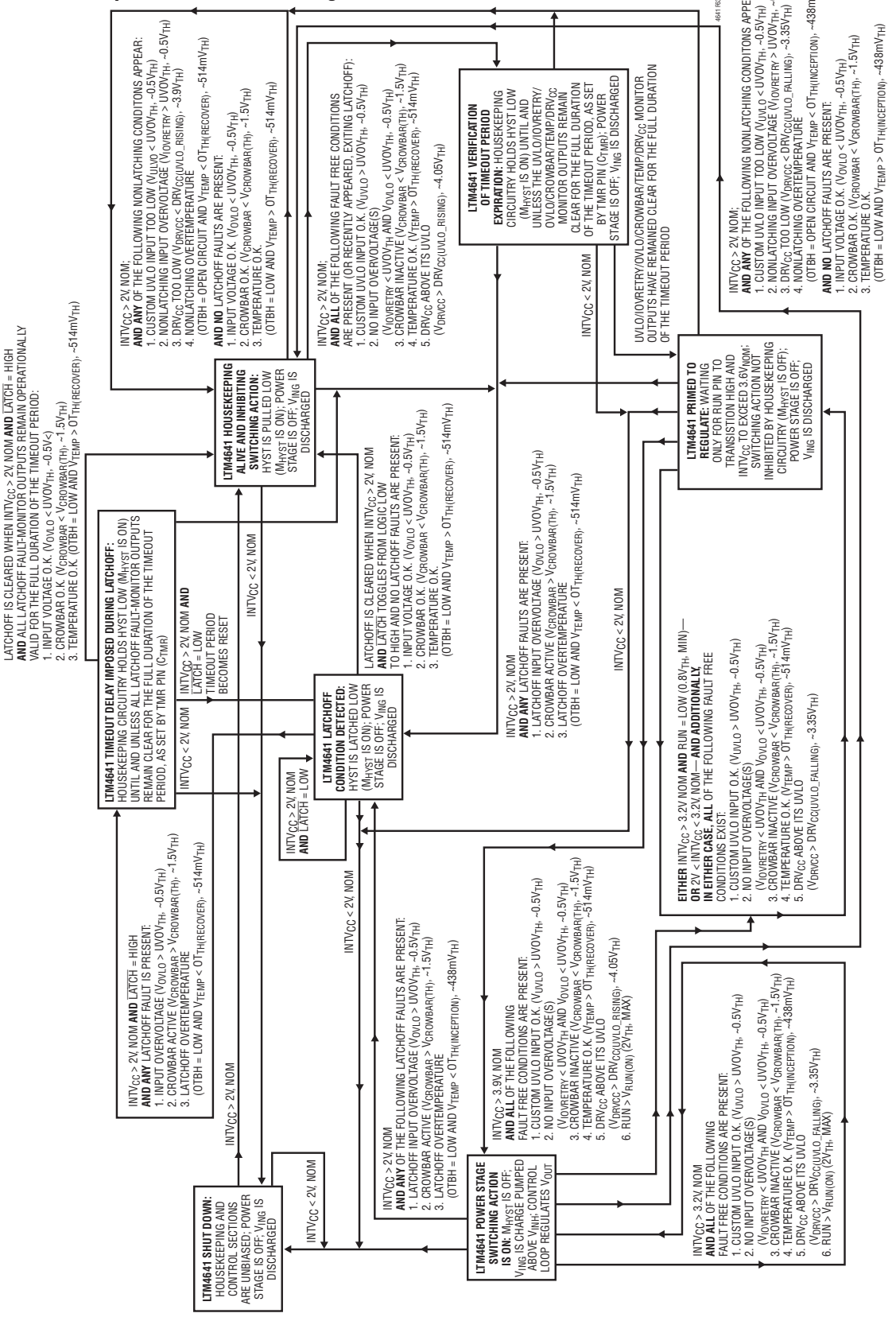


Figure 63. Start-Up/Shutdown State Diagram

APPENDICES

Appendix C. Switching Frequency Considerations and Usage of R_{fSET}

There exist many scenarios in which a resistor, R_{fSET}, should be connected externally to LTM4641's f_{SET} pin—to decrease the on-time of M_{TOP}: most commonly, when the output voltage setting is less than or equal to 3V, and in rail-tracking applications; and less commonly, when V_{INL} and V_{INH} are operating from different source supplies. In the former cases, R_{fSET} is usually applied from f_{SET} to V_{INL} (Figure 45 and front page application circuit); in the latter, R_{fSET} is usually applied from f_{SET} to the voltage source feeding LTM4641's power stage—upstream of MSP, if a power-interrupt input MOSFET is used (Figure 49). There are several motivations and considerations behind this guidance:

(1) Inherent to LTM4641's constant on-time architecture, the switching frequency of LTM4641 decreases as output voltage decreases. In order to maintain a reasonable output capacitor value solution size and output voltage ripple—even at lower output voltages ($\leq 3V_{OUT}$)—R_{fSET} should be applied, so that the controller's I_{ON} pin current and the resulting nominal switching frequency is higher than the on-time dictated by the internal V_{INL}-to-f_{SET}-connected 1.3MΩ resistor.

(2) The PFM control scheme employed by LTM4641 yields a switching frequency at zero load current ("no-load operation") that is typically 20% to 25% lower than what it is at full load. As a result, inductor ripple current is proportionally higher at no load than what it is at heavy load. Recall that LTM4641 employs $R_{DS(ON)}$ current sensing; furthermore, realize that it is essential for the controller's current-sense amplifier to be able to perceive and command sufficiently negative inductor trough current, enough to maintain a maximum average inductor current of 0A, so that output voltage can be properly regulated down to no load. A value of R_{fSET} should be used to assure that switching frequency is high enough (or on-time is small enough) at no load so that the current-sense information representing the trough of choke current is never too large in amplitude. Figure 3 provides conservative guidance on the maximum value of R_{fSET} (or equivalently, the minimum I_{ON} current) that assures proper no-load operation.

(3) In rail-tracking applications, LTM4641's output voltage must track a reference voltage not only during V_{OUT} ramp up but also during V_{OUT} ramp down; fulfilling the latter requires LTM4641 to sink current from the output capacitors. A value of R_{fSET} should be used that assures the output voltage can be ramped down to one's minimum desired output voltage of regulation—not just the intended nominal output voltage. Figure 3 provides this guidance.

(4) In order to maintain a relatively constant switching frequency for a given output voltage (across the full line voltage), the on-time of M_{TOP} should be inversely proportional to the voltage source feeding the V_{INH} power stage—upstream of MSP, if a power-interrupt MOSFET is used (Figure 46). When V_{INL} and V_{INH} are operated from different rails, this goal can be accomplished satisfactorily by placing R_{fSET} between f_{SET} and the power V_{IN} input source (see Figure 49: the connection is to V_{IN} and not V_{INL}, and usually not V_{INH}, but see a counterexample in Figure 47 and explanation in item number 5 of this list). A minor error term to the on-time is introduced by the internal 1.3MΩ V_{INL}-to-f_{SET}-connected resistor in such scenarios, so calculation of I_{ION} at all operating input voltage corner cases (power, V_{INH} and control bias, V_{INL} extremes) and the resulting switching frequency range of operation, given by Equation 6, should be considered.

(5) When MSP is used, and when V_{INL} and V_{INH} are operated from different rails—here is the reason it is recommended to connect R_{fSET} from f_{SET} to the drain of MSP rather than V_{INH}: prior to start-up, MSP is off, and V_{INH} is discharged. Connecting R_{fSET} to V_{INH} would set the on-time at the instant switching activity commenced to be much lower than intended. The on-time would not reach its final settling value until V_{ING} circuitry had turned on MSP enough for V_{INH} to become pulled up to V_{IN} potential. It should become apparent that a mechanism may exist for dynamic interaction between how rapidly the output voltage ramps up (depending on TRACK/SS pin usage) versus how rapidly MSP might turn on. We know from item number 2 of this list that on-time should not be arbitrarily large. In general, to avoid any undesirable

APPENDICES

interactions—which might at worst result in excessive output voltage ripple or non-monotonic output voltage ramp-up, a sufficiently slow output voltage ramp-up time can eliminate the danger of V_{INH} and on-time settling interactions influencing output voltage ripple—but properly, this requires investigation and hardware evaluation on a case-by-case basis. Figure 47 shows an example where R_{fSET} connects between f_{SET} and V_{INH}—rather than the input source supply. Because MSP limits the V_{INH} voltage during the input voltage surge, the correct I_{ON} programming current can only be made with a resistor interface to V_{INH}, in that example.

Appendix D. Remote Sensing in Harsh Environments

The rationale for using the symmetrical resistor network is to provide a consistent feedback structure that enables fully differential remote-sense of output voltages between 0.6V and 6V with the flexibility to filter differential and common mode noise in harsh environments. See Figure 64. The use of not greater than 8.2kΩ nominal resistors for R_{SET1A} (and R_{SET1B}) assures that the remote-sense signal is not attenuated at frequencies of interest by the pole formed by the feedback resistors and parasitic capacitances. Furthermore, using an R_{SET1A} (and R_{SET1B}) value of 8.2kΩ for $1.2V_{OUT}$ and larger assures that the common mode range of the remote-sense pins is within their valid range of –0.3V, minimum, to 3V, maximum—even if voltage drop between the module's ground deviates from the POL's ground by as much as ±0.6V.

The differential remote-sense feedback signal is routed from the load as a differential pair on PCB traces (or twisted pair, if wires are used) to R_{SET1A}/R_{SET1B} feedback components. It is very important to place R_{SET1A}/R_{SET1B} and all other components forming the feedback impedance-divider network as close to LTM4641 as is possible. Ground shielding of the differential remote-sense signal is strongly recommended, to prevent stray noise from contaminating the feedback information.

If good shielding of the feedback signals cannot be provided, it is proactive to leave space in one's layout for a small filter capacitor, C_{DM}, placed directly between V_{OSNS}^+ and V_{OSNS}^-, as close to the pins of the module as possible—in anticipation of the possible need to attenuate differential mode noise.

Finally, if the POL is very far from the LTM4641, such as: the output power connection (V_{OUT} and GND) is made

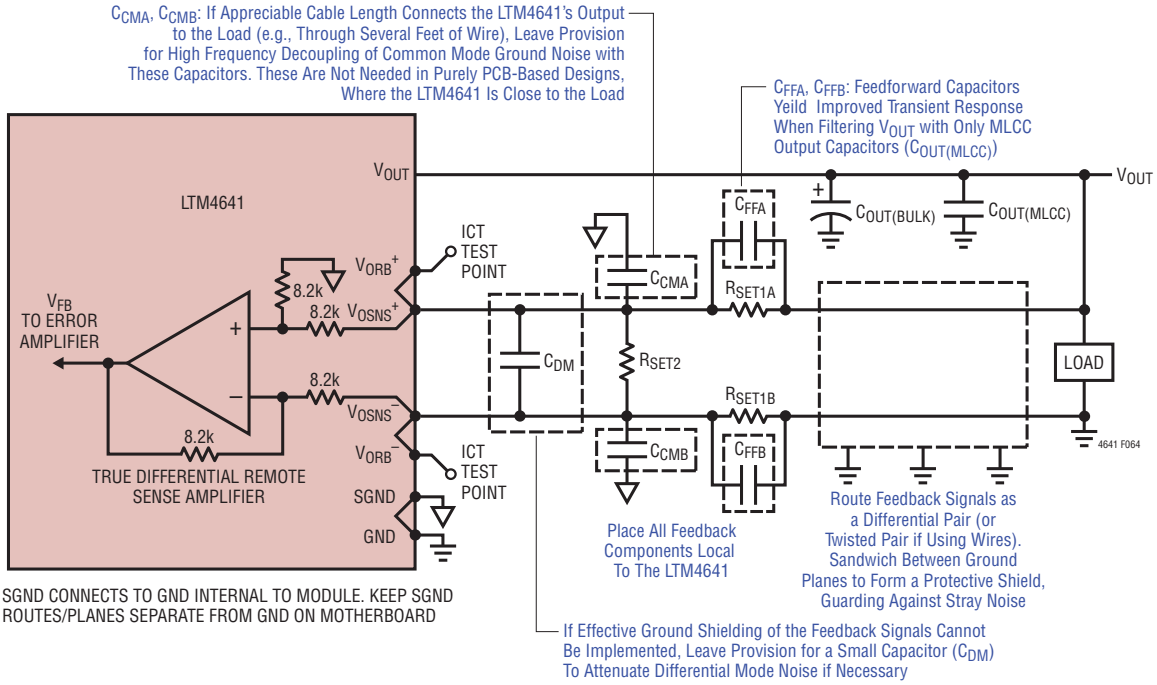


Figure 64. Feedback Remote Sense Connections and Techniques for Harshest Operating Environments

APPENDICES

through a board-to-board connector; an inductive length of cable (say, 50cm in length, or more); or, if the load is highly inductive—then it is proactive to leave provision in one's layout for a pair of small filter capacitors, C_{CMA} and C_{CMB}. C_{CMA} and C_{CMB} should be placed directly from V_{OSNS}^+ to SGND and V_{OSNS}^- to SGND, respectively—as close to the pins of the module as possible. Configured in this manner, C_{CMA} and C_{CMB} can be used to attenuate common mode noise in the remote-sense signal pin pair.

Appendix E. Inspiration For Pulse-Skipping Mode Operation

When M_{TOP} is turned on—for a duration of time proportional to I_{ION} current—inductor current is ramped upwards, and energy is built up in the inductor's B-field. Ultimately, a "packet" of energy is transferred from the input capacitors to the output capacitors. In forced continuous mode operation (FCB logic low), M_{TOP} and M_{BOT} are operated in a purely synchronous fashion, meaning: when M_{TOP} is on, M_{BOT} is off—and vice versa. Observe that when M_{TOP} is turned off, the B-field in the inductor cannot instantaneously vanish: the collapsing B-field forces inductor current to flow through M_{BOT}'s on-die Schottky diode—resulting in unwanted freewheeling diode power loss; M_{BOT} is turned on for lower power loss, instead. With M_{BOT} on, inductor current ramps downward as energy in its B-field wanes.

In steady-state forced continuous mode operation, the inductor ripple current appears as a triangle waveform whose average value equates to the load's current. Forced continuous mode operation (forcing synchronous operation of M_{TOP} and M_{BOT}) provides a mechanism for consistent output voltage ripple, regardless of the load current. However, in this mode of operation, at light load currents (say, less than 2A out), observe that the inductor current is periodically negative—which means some packets of energy that are transferred from the input capacitors to the output are recirculated and transferred back to the input capacitors. This is a source of inefficiency that brings about the motivation for pulse-skipping mode operation, to turn off M_{BOT} when the inductor current ramps down to 0A. This concept is also described in the industry as "diode emulation", because M_{BOT} is made to mimic the behavior of a Schottky rectifier. In pulse-skipping mode operation (FCB logic high), the inductor ripple current at light loads appears as an asymmetrical truncated triangle waveform; inductor current does not go below 0A.

Appendix F. Adjusting the Fast Output Overvoltage Comparator Threshold

The output overvoltage inception threshold (OV_{PGM} voltage) can be adjusted or tightened from its default value. The following guidelines must be followed, however:

- It is not recommended to change the OV_{PGM} voltage dynamically because the fast OOV comparator has no glitch immunity beyond what is provided by OV_{PGM}'s internal 47pF capacitor, and routing of OV_{PGM} can make it vulnerable to electrostatic noise.
- The 15.6µs time constant filter formed by OV_{PGM}'s internal 47pF capacitor and default 499kΩ||1MΩ resistor-divider network should be maintained for practical values of OV_{PGM} voltage: $0.6V < V_{OVPGM} < 0.9V$. Capacitive filtering of OV_{PGM} must not be applied indiscriminately. The OV_{PGM} voltage must come up very rapidly with the $1V_{REF}$ at start-up, to prevent a race condition that would otherwise result in nuisance OOV detection and a faulty latchoff event—so any externally applied capacitance cannot be arbitrarily high. On the other hand, OV_{PGM} must have some filtering from switching noise sources and should be sufficiently insulated from any possible dynamic activity on $1V_{REF}$. (See Figure 9.)
- External resistor(s) applied between OV_{PGM} and $1V_{REF}$/SGND should be relatively high impedance, to minimize loading on the $1V_{REF}$ output. Then, small values of C_{OVPGM} achieve a consistent time constant as OVPGM's resistance-divider network is altered.

Figure 65 shows the optional network one can apply to alter or tighten the OV_{PGM} setpoint.

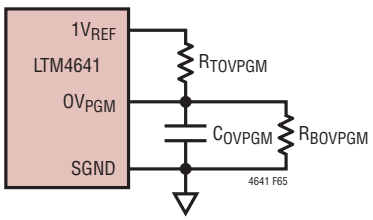


Figure 65. Optional OV_{PGM} Network to Alter or Tighten V_{OVPGM}

APPENDICES

To nudge the OV_{PGM} setpoint downward, to a new OOV inception threshold voltage at $OV_{PGM(NEW)}$—using an R_{BOVPGM} resistor, only—calculate:

$$R_{BOVPGM} = \frac{1}{\frac{1V - OV_{PGM(NEW)}}{OV_{PGM(NEW)} \bullet 499k\Omega} - \frac{1}{1M\Omega}} \quad (37)$$

The new OV_{PGM} threshold can then be double-checked by

$$OV_{PGM(NEW)} = \frac{1V \bullet (1M\Omega \,||\, R_{BOVPGM})}{(499k\Omega + 1M\Omega \,||\, R_{BOVPGM})} \quad (38)$$

When lowering the OV_{PGM} setpoint with application of R_{BOVPGM} only, it is not necessary to apply a C_{OVPGM} capacitor, because: for an extreme OVPGM(NEW) setting of 600mV, which is not practical since that is the voltage of V_{FB} during normal regulation, the time-constant of the OV_{PGM} network would have changed by less than 2µs from its default value.

To nudge the OV_{PGM} trip threshold upward to set a new OOV inception threshold voltage at $OV_{PGM(NEW)}$—using an R_{TOVPGM} resistor only—calculate:

$$R_{TOVPGM} = \frac{1}{\frac{OV_{PGM(NEW)}}{(1V - OV_{PGM(NEW)}) \bullet 1M\Omega} - \frac{1}{499k\Omega}} \quad (39)$$

The new OV_{PGM} setting can then be double-checked by:

$$OV_{PGM(NEW)} = \frac{1V \bullet 1M\Omega}{(499k\Omega \,||\, R_{TOVPGM} + 1M\Omega)} \quad (40)$$

If R_{TOVPGM} is computed in Equation 39 to be smaller than 10kΩ, connect OV_{PGM} to $1V_{REF}$ and do not apply any C_{OVPGM} capacitor; this will yield an OOV setting of 167% of nominal. Otherwise, use the next smallest standard value of C_{OVPGM} available, computed by:

$$C_{OVPGM} = \frac{15.6\mu s}{(499k\Omega \,||\, 1M\Omega \,||\, R_{TOVPGM})} - 47pF \quad (41)$$

The default V_{OVPGM} setpoint is 665mV ±2.26%, over temperature. To tighten the OV_{PGM} setpoint, begin by choosing R_{BOVPGM} to be a commonly available precision 100kΩ, low T.C.R. resistor. Using tolerances of ±0.1% and a T.C.R. of ±25ppm/°C can provide a considerable improvement in accuracy over the default divider network, over temperature. Next, decide the new value of V_{OVPGM} desired—$OV_{PGM(NEW)}$—within a practical window of 0.6V < $OV_{PGM(NEW)}$ < 0.9V. Then, compute R_{TOVPGM} according to:

$$R_{TOVPGM} = \frac{1}{\frac{OV_{PGM(NEW)}}{(1V - OVP_{GM(NEW)}) \bullet (1M\Omega \,||\, R_{BOVPGM})} - \frac{1}{499k\Omega}} \quad (42)$$

The new OV_{PGM} setting can be double-checked by:

$$OV_{PGM(NEW)} = \frac{1V \bullet (1M\Omega \,||\, R_{BOVPGM})}{(499k\Omega \,||\, R_{TOVPGM} + 1M\Omega \,||\, R_{BOVPGM})} \quad (43)$$

Then, use the next smallest standard value of C_{OVPGM} available, computed by:

$$C_{OVPGM(NEW)} = \frac{15.6\mu s}{(499k\Omega \,||\, 1M\Omega \,||\, R_{TOVPGM} \,||\, R_{BOVPGM})} - 47pF \quad (44)$$

For example, the $OV_{PGM(NEW)}$ setpoint can be kept at its nominal value of 666mV—but with better accuracy—by using ±0.1% precision resistors with ±25ppm/°C T.C.R. for R_{BOVPGM} = 100k and R_{TOVPGM} = 49.9k, and bypassing OV_{PGM} to SGND with C_{OVPGM} = 470pF. The resulting V_{OVPGM} OOV setpoint threshold becomes better than ±1.8%, over temperature. The vast majority of the remaining variation in the threshold setting comes variation of the $1V_{REF}$—a ±1.5% reference, over temperature.

The extreme values of the OOV setpoint voltage, plus the OVP_{ERR} term—which is the offset voltage of the fast comparator (±12mV maximum, over temperature)—gives guidance on what the minimum and maximum voltage V_{FB} can be at which the CROWBAR output would swing logic high and invoke latchoff overvoltage protection.

One must take care to set the OV_{PGM} voltage to a practical level and not too aggressively. If OV_{PGM} is set too low, the system will demonstrate nuisance output overvoltage latchoff behavior. The output voltage of any switching

APPENDICES

regulator can witnesses transient excursions above its ideal DC voltage operating point routinely, owing to:

- Control IC bandgap reference accuracy
- Output voltage ripple and noise
- Load current step-down transient events—including recovery from a short-circuit condition
- Steep line voltage step-up
- Start-up overshoot (little or no soft-starting of V_{OUT}), or rail-tracking a fast master rail

The Linear Technology LTpowerCAD design tool can help quantify some of these dynamic values; LTM4641's total DC error (including bandgap reference variation) is better than ±1.5%, over temperature.

If OV_{PGM} has been decreased to its lowest practical level and output voltage overshoot during high side MOSFET short-circuit testing (shorting V_{INH} to SW on evaluation hardware such as DC1543, for example) does not clamp the output voltage to one's satisfaction, be aware that increasing output capacitance can reduce the maximum output voltage excursion. The reason follows: the larger the output capacitance, the longer it takes for the output voltage to be ramped up, even in the extreme case of deliberately short circuiting V_{INH} to SW. The capacitance on V_{OUT} is mainly what prevents the output voltage from shooting up to V_{INH}—until CROWBAR turns on MCB.

Multimodule parallel applications also have better output voltage overshoot during high side MOSFET short-circuit testing, owing to the fact that the sibling modules whose high side MOSFETs are not short circuited are able to help pull the output voltage down by turning on their low side power MOSFETs. Examples of paralleled LTM4641 powering and protecting loads are shown in Figures 56 and 66.

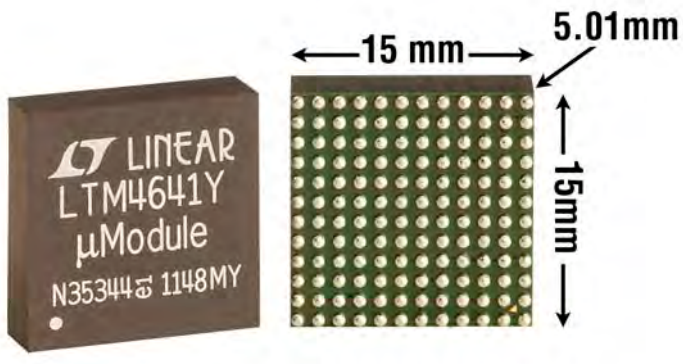
PACKAGE DESCRIPTION

Table 10. LTM4641 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	SGND	B1	SGND	C1	SGND	D1	V_{ORB}^+	E1	GND	F1	GND
A2	SGND	B2	SGND	C2	SGND	D2	V_{ORB}^-	E2	GND	F2	GND
A3	SGND	B3	SGND	C3	SGND	D3	OTBH	E3	GND	F3	GND
A4	HYST	B4	UVLO	C4	SGND	D4	TMR	E4	GND	F4	GND
A5	TEMP	B5	OVLO	C5	$\overline{LATCH}$	D5	RUN	E5	GND	F5	GND
A6	IOVRETRY	B6	GND	C6	$1V_{REF}$	D6	GND	E6	GND	F6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND
A8	GND	B8	GND	C8	GND	D8	GND	E8	GND	F8	GND
A9	GND	B9	CROWBAR	C9	V_{OUT}	D9	V_{OUT}	E9	V_{OUT}	F9	GND
A10	GND	B10	OV_{PGM}	C10	V_{OUT}	D10	V_{OUT}	E10	V_{OUT}	F10	GND
A11	GND	B11	GND	C11	V_{OUT}	D11	V_{OUT}	E11	V_{OUT}	F11	GND
A12	GND	B12	GND	C12	V_{OUT}	D12	V_{OUT}	E12	V_{OUT}	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	V_{OSNS}^+	J1	COMP	K1	SGND	L1	PGOOD	M1	SGND
G2	GND	H2	V_{OSNS}^-	J2	f_{SET}	K2	FCB	L2	TRACK/SS	M2	SGND
G3	GND	H3	GND	J3	V_{INL}	K3	SGND	L3	SGND	M3	SGND
G4	GND	H4	GND	J4	DRV_{CC}	K4	$INTV_{CC}$	L4	GND	M4	GND
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND	M5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND	M6	GND
G7	GND	H7	GND	J7	GND	K7	V_{INH}	L7	V_{INH}	M7	V_{INH}
G8	GND	H8	GND	J8	GND	K8	V_{INH}	L8	V_{INH}	M8	V_{INH}
G9	GND	H9	GND	J9	GND	K9	V_{INH}	L9	V_{INH}	M9	V_{ING}
G10	GND	H10	SW	J10	GND	K10	V_{INH}	L10	V_{INH}	M10	V_{INGP}
G11	GND	H11	GND	J11	GND	K11	GND	L11	V_{INH}	M11	V_{INH}
G12	GND	H12	GND	J12	GND	K12	GND	L12	V_{INH}	M12	V_{INH}

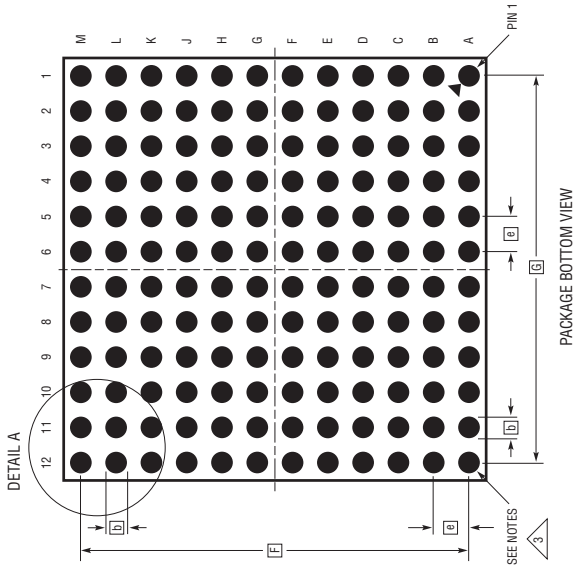
PACKAGE PHOTO



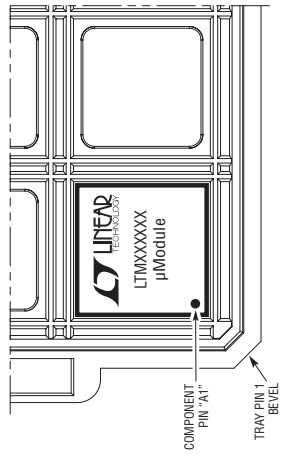
PACKAGE DESCRIPTION

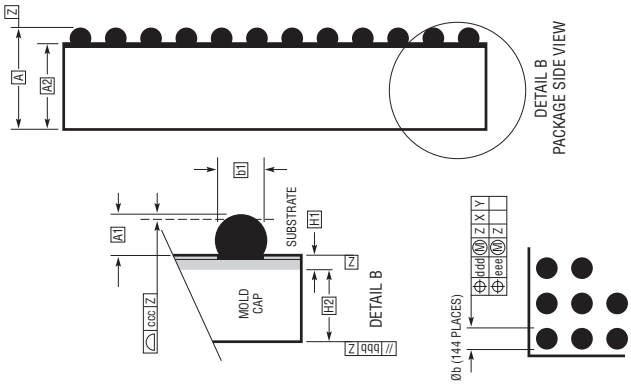
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

BGA Package
144-Lead (15mm × 15mm × 5.01mm)
(Reference LTC DWG # 05-08-1914 Rev Ø)



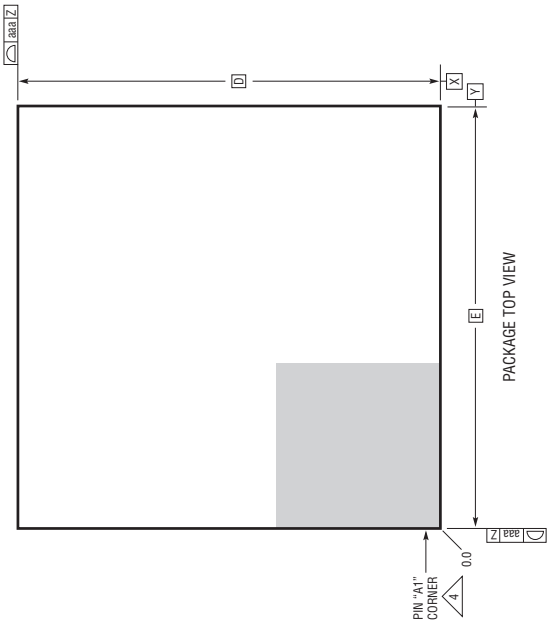
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu

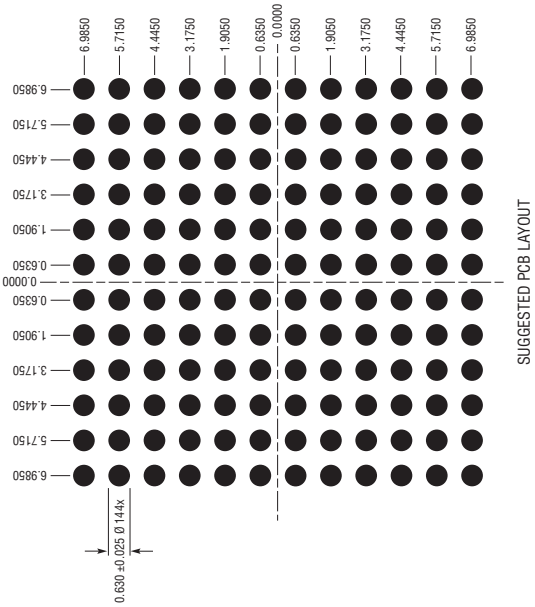




DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 144





REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/13	Updated Figure 1	15

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

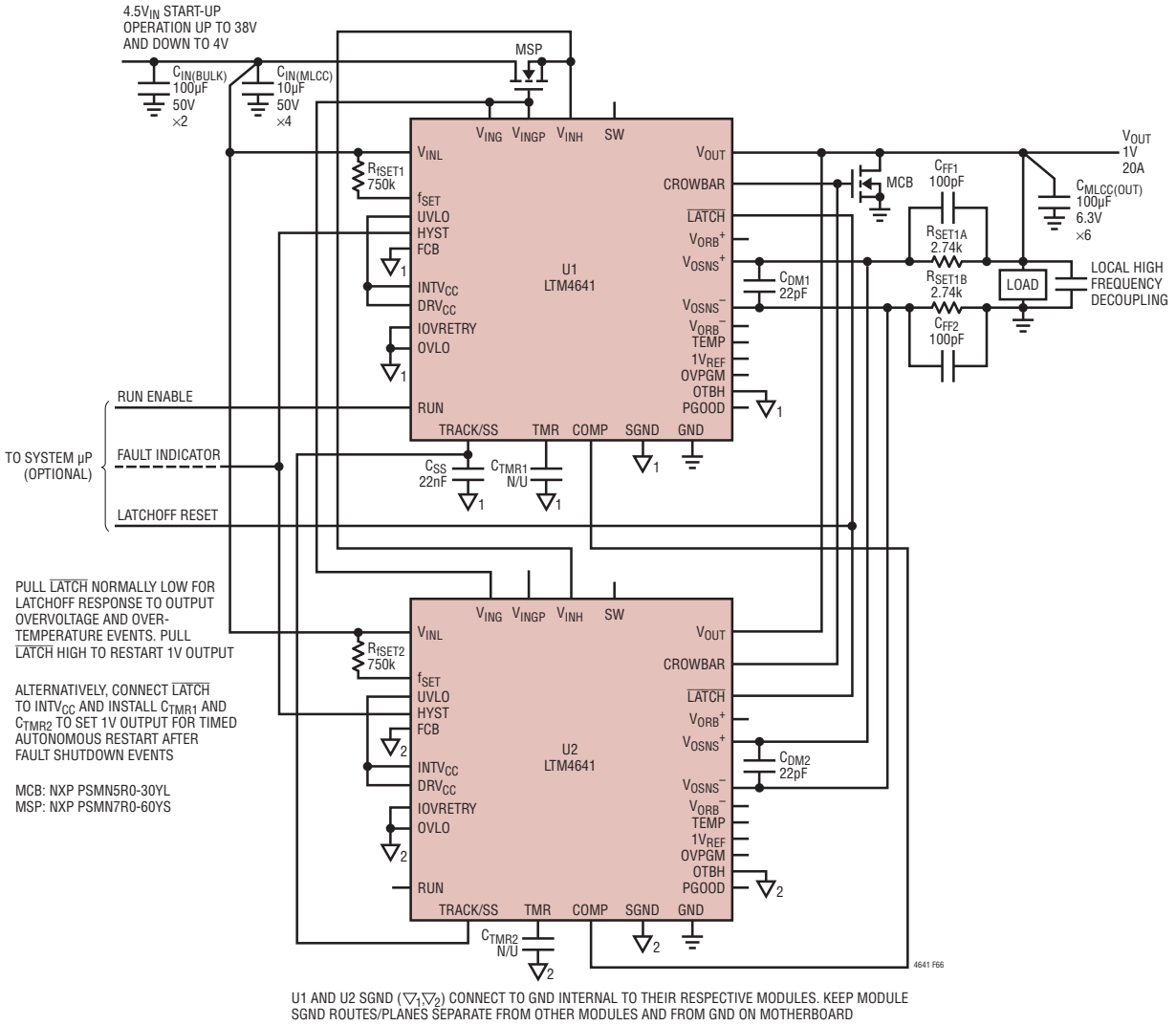


Figure 66. 1V, 20A Fault-Protected Load Powered by Paralleled LTM4641—from Up to 38V_{IN}. cf. Typical Performance Characteristics

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4620	Dual 13A, Single 26A µModule Regulator	Up to 100A with Four Devices; 4.5V ≤ V_{IN} ≤ 16V; 0.6V ≤ V_{OUT} ≤ 2.5V. See LTM4620A for Higher V_{OUT}; 15mm × 15mm × 4.41mm LGA
LTM4613	EN55022B Certified 36V, 8A Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V; 3.3V ≤ V_{OUT} ≤ 15V; Synchronizable, Parallelable, 15mm × 15mm × 4.32mm LGA
LTM4627	20V, 15A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 20V; 0.6V ≤ V_{OUT} ≤ 5V; Synchronizable, Parallelable, Remote Sensing, 15mm × 15mm × 4.32mm LGA or 15mm × 15mm × 4.92mm BGA
LTM8027	60V, 4A Step-Down µModule Regulator	4.5V ≤ V_{IN} ≤ 60V; 2.5V ≤ V_{OUT} ≤ 24V; Synchronizable, 15mm × 15mm × 4.32mm LGA
LTM4609	36V, 4A Buck-Boost µModule Regulator	4.5V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 34V; Synchronizable, Parallelable, Up to 4A in Boost Mode and 10A in Buck Mode, 15mm × 15mm × 2.82mm LGA or 15mm × 15mm × 3.42mm BGA
LT4356	High Voltage Surge Stopper	100V_{IN} Overvoltage and Overcurrent Protection, Latchoff and Auto-Retry Options

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/4641
LT 0213 REV B • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2012